

Bias Resistor Transistor

PNP Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

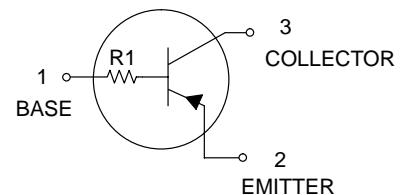
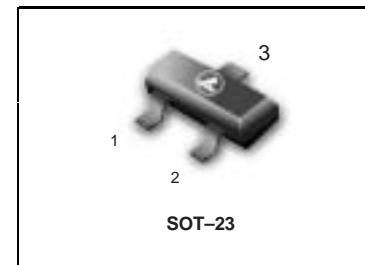
LDTA113TLT1G

- Applications

Inverter, Interface, Driver

- Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
 - 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
 - 3) Only the on/off conditions need to be set for operation, making the device design easy.
- We declare that the material of product compliance with RoHS requirements.



- Absolute maximum ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	-50	V
Collector-emitter voltage	V_{CEO}	-50	V
Emitter-base voltage	V_{EBO}	-5 to +10	V
Collector current	I_c	-100	mA
Collector Power dissipation	P_c	200	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTA113TLT1G	O2	1	-	3000/Tape & Reel
LDTA113TLT3G	O2	1	-	10000/Tape & Reel

- Electrical characteristics ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	-50	-	-	V	$I_c = -50\mu\text{A}$
Collector-emitter breakdown voltage	BV_{CEO}	-50	-	-	V	$I_c = -1\text{mA}$
Emitter-base breakdown voltage	BV_{EBO}	-5	-	-	V	$I_E = -50\mu\text{A}$
Collector cutoff current	I_{CBO}	-	-	-0.5	μA	$V_{CB} = -50\text{V}$
Emitter cutoff current	I_{EBO}	-	-	-0.5	μA	$V_{EB} = -4\text{V}$
Collector-emitter saturation voltage	$V_{CE(\text{sat})}$	-	-	-0.3	V	$I_c/I_b = -5\text{mA} / -0.25\text{mA}$
DC current transfer ratio	h_{FE}	100	250	600	-	$I_c = -1\text{mA}, V_{CE} = -5\text{V}$
Input resistance	R_i	0.7	1	1.3	$\text{k}\Omega$	-
Transition frequency	f_T	*	-	250	-	$V_{CB} = -10\text{V}, I_c = 5\text{mA}, f = 100\text{MHz}$

* Characteristics of built-in transistor

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●Electrical characteristic curves

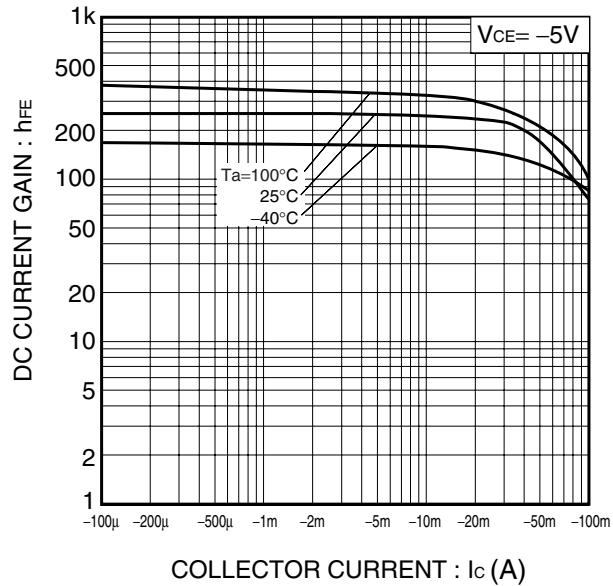


Fig.1 DC Current gain
vs. Collector Current

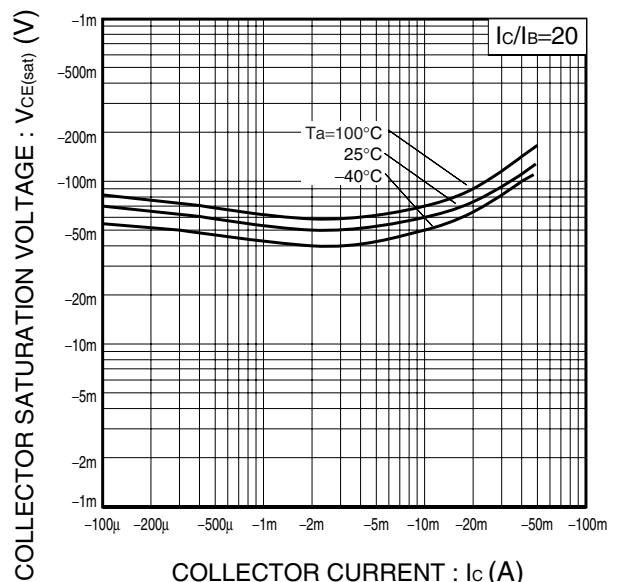
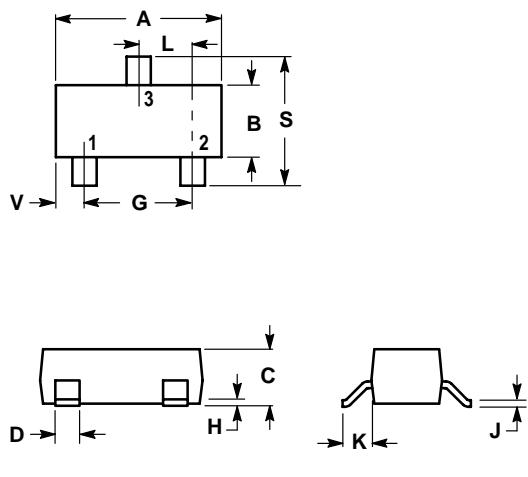


Fig.2 Collector-emitter saturation voltage
vs. Collector Current

LDTA113TLT1G
SOT-23
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

