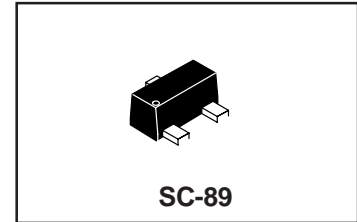


# Bias Resistor Transistors

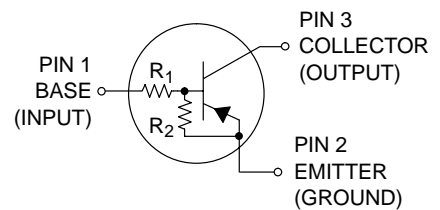
## PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

### LDTA114EET1G Series S-LDTA114EET1G Series



This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-89 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SC-89 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- We declare that the material of product compliance with RoHS requirements.
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CBO}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mAdc

#### THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Total Device Dissipation, FR-4 Board (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.6	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	600	$^\circ\text{C/W}$
Total Device Dissipation, FR-4 Board (Note 2) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	400	$^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-4 @ Minimum Pad.
2. FR-4 @  $1.0 \times 1.0$  Inch Pad.

## LDTA114EET1G Series, S-LDTA114EET1G Series

### ORDERING INFORMATION AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping <sup>†</sup>
LDTA114EET1G	6A	10	10	SC-89	3000 Tape & Reel
LDTA124EET1G	6B	22	22	SC-89	3000 Tape & Reel
LDTA144EET1G	6C	47	47	SC-89	3000 Tape & Reel
LDTA114YET1G	6D	10	47	SC-89	3000 Tape & Reel
LDTA114TET1G	6E	10	∞	SC-89	3000 Tape & Reel
LDTA143TET1G	6F	4.7	∞	SC-89	3000 Tape & Reel
LDTA123EET1G	6H	2.2	2.2	SC-89	3000 Tape & Reel
LDTA143EET1G	43	4.7	4.7	SC-89	3000 Tape & Reel
LDTA143ZET1G	6K	4.7	47	SC-89	3000 Tape & Reel
LDTA124XET1G	6L	22	47	SC-89	3000 Tape & Reel
LDTA123JET1G	6M	2.2	47	SC-89	3000 Tape & Reel
LDTA115EET1G	6N	100	100	SC-89	3000 Tape & Reel
LDTA144WET1G	6P	47	22	SC-89	3000 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	100	nAdc
Collector-Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	500	nAdc
Emitter-Base Cutoff Current (V <sub>EB</sub> = 6.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	0.5	mAdc
	LDTA114EET1G	–	–	0.2	
	LDTA124EET1G	–	–	0.1	
	LDTA144EET1G	–	–	0.2	
	LDTA114YET1G	–	–	0.9	
	LDTA114TET1G	–	–	1.9	
	LDTA143TET1G	–	–	2.3	
	LDTA123EET1G	–	–	1.5	
	LDTA143EET1G	–	–	0.18	
	LDTA143ZET1G	–	–	0.13	
	LDTA124XET1G	–	–	0.2	
	LDTA123JET1G	–	–	0.05	
	LDTA115EET1G	–	–	0.13	
	LDTA144WET1G	–	–		
Collector-Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	–	–	Vdc

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

# LDTA114EET1G Series, S-LDTA114EET1G Series

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>ON CHARACTERISTICS</b> (Note 4)						
DC Current Gain ( $V_{CE} = 10\text{ V}$ , $I_C = 5.0\text{ mA}$ )	LDTA114EET1G LDTA124EET1G LDTA144EET1G LDTA114YET1G LDTA114TET1G LDTA143TET1G LDTA123EET1G LDTA143EET1G LDTA143ZET1G LDTA124XET1G LDTA123JET1G LDTA115EET1G LDTA144WET1G	$h_{FE}$	35 60 80 80 160 160 8.0 15 80 80 80 80 80	60 100 140 140 250 250 15 27 140 130 140 150 140	– – – – – – – – – – – – –	– – – – – – – – – – – – –
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_E = 0.3\text{ mA}$ ) ( $I_C = 10\text{ mA}$ , $I_B = 5\text{ mA}$ ) ( $I_C = 10\text{ mA}$ , $I_B = 1\text{ mA}$ )	LDTA123EET1G LDTA114TET1G/LDTA143TET1G LDTA143ZET1G/LDTA124XET1G LDTA143EET1G	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )  ( $V_{CC} = 5.0\text{ V}$ , $V_B = 3.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 5.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 4.0\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	LDTA114EET1G LDTA124EET1G LDTA114YET1G LDTA114TET1G LDTA143TET1G LDTA123EET1G LDTA143EET1G LDTA143ZET1G LDTA124XET1G LDTA123JET1G LDTA144EET1G LDTA115EET1G LDTA144WET1G	$V_{OL}$	– – – – – – – – – – – – –	– – – – – – – – – – – – –	0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2	Vdc
Output Voltage (off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.25\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	LDTA114TET1G LDTA143TET1G LDTA123EET1G LDTA143EET1G LDTA115EET1G	$V_{OH}$	4.9	–	–	Vdc
Input Resistor	LDTA114EET1G LDTA124EET1G LDTA144EET1G LDTA114YET1G LDTA114TET1G LDTA143TET1G LDTA123EET1G LDTA143EET1G LDTA143ZET1G LDTA124XET1G LDTA123JET1G LDTA115EET1G LDTA144WET1G	R1	7.0 15.4 32.9 7.0 7.0 3.3 1.5 3.3 3.3 15.4 1.54 70 32.9	10 22 47 10 10 4.7 2.2 4.7 4.7 22 2.2 100 47	13 28.6 61.1 13 13 6.1 2.9 6.1 6.1 28.6 2.86 130 61.1	k $\Omega$
Resistor Ratio	LDTA114EET1G/LDTA124EET1G LDTA144EET1G/LDTA115EET1G LDTA114YET1G LDTA114TET1G/LDTA143TET1G LDTA123EET1G/LDTA143EET1G LDTA143ZET1G LDTA124XET1G LDTA123JET1G LDTA144WET1G	$R_1/R_2$	0.8 0.17 – 0.8 0.055 0.38 0.038 1.7	1.0 0.21 – 1.0 0.1 0.47 0.047 2.1	1.2 0.25 – 1.2 0.185 0.56 0.056 2.6	–

4. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%

# LDTA114EET1G Series, S-LDTA114EET1G Series

## TYPICAL ELECTRICAL CHARACTERISTICS – LDTA114EET1G

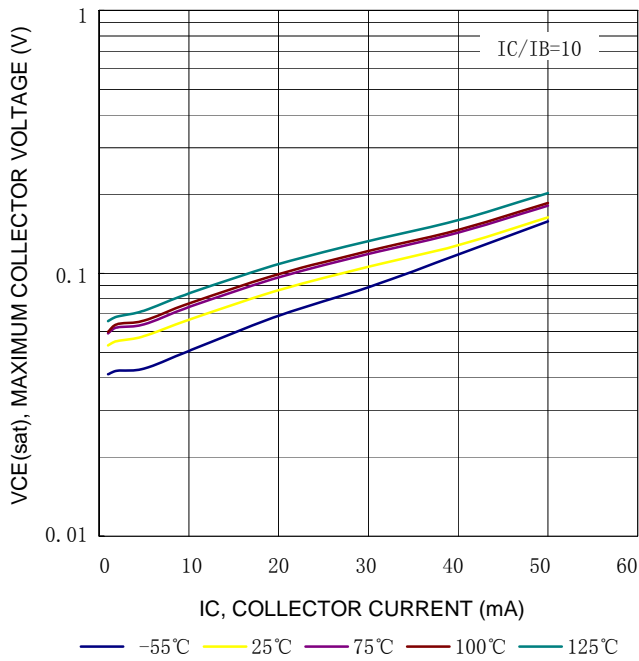


Fig. 1  $V_{CE(sat)}$  VS  $I_C$

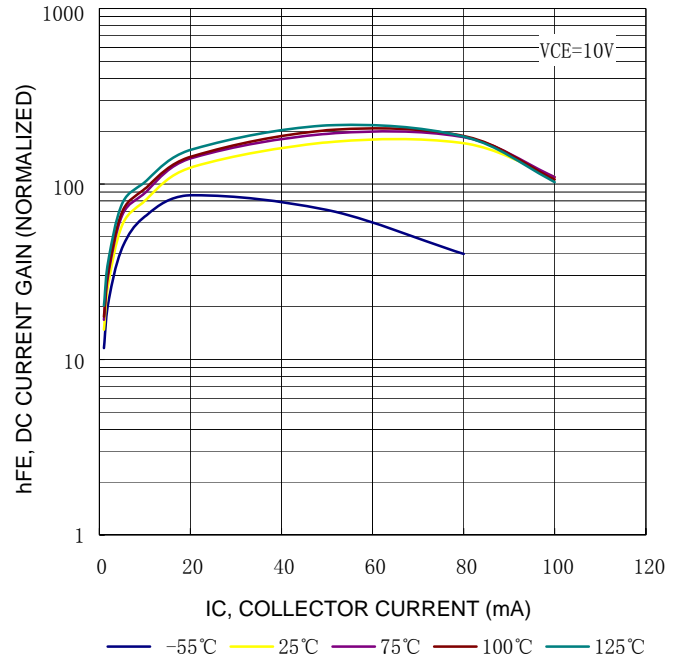


Fig. 2 DC CURRENT GAIN

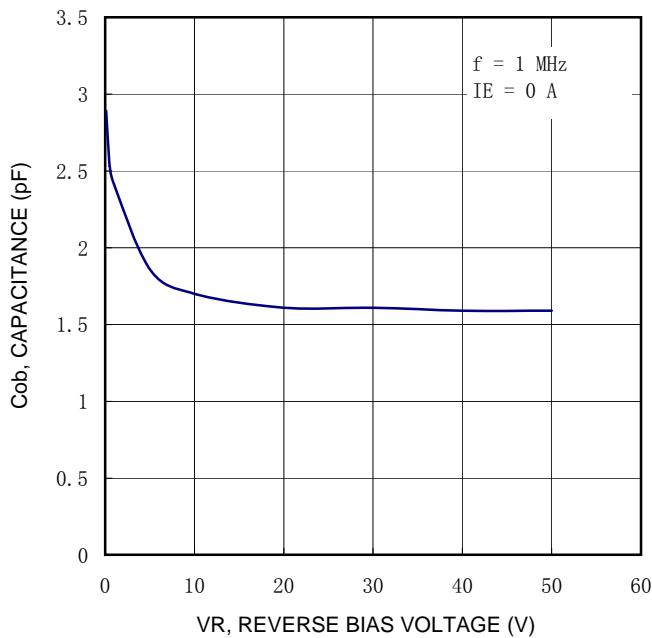


Fig. 3 OUTPUT CAPACITANCE

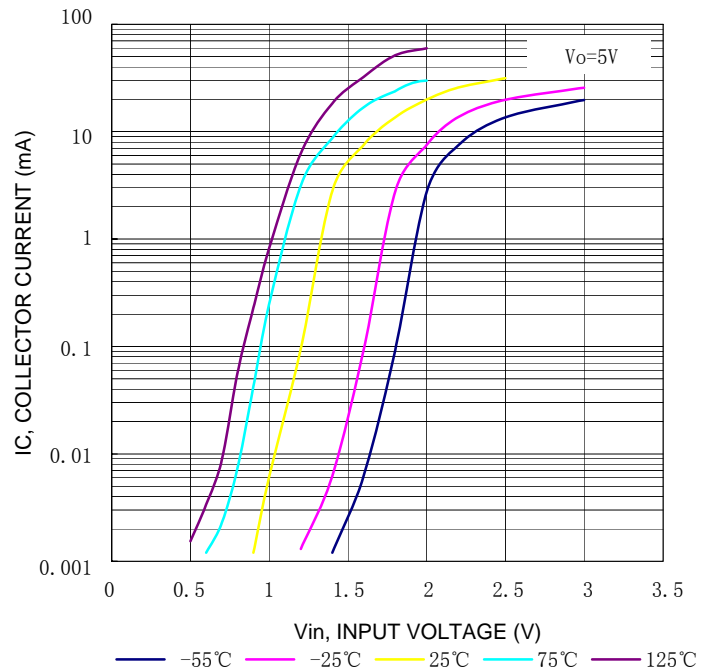
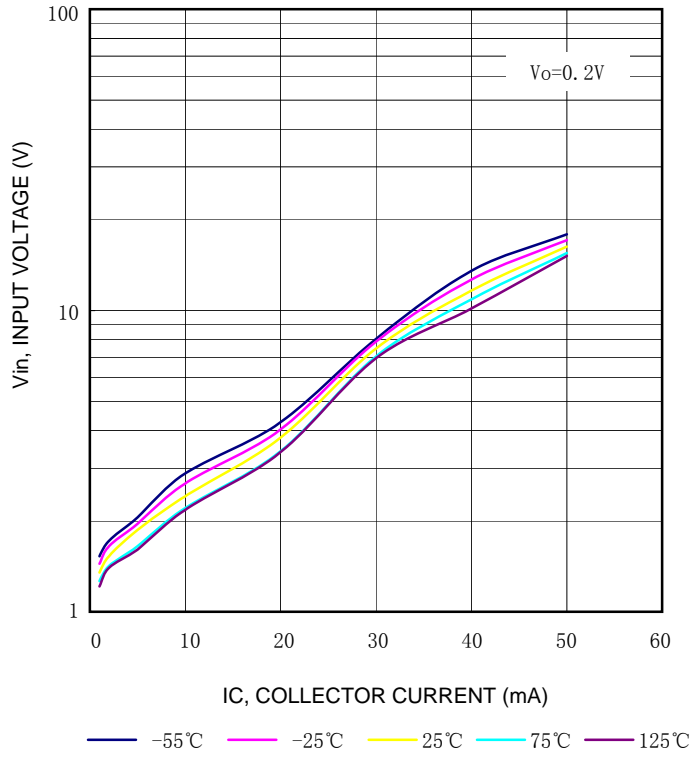
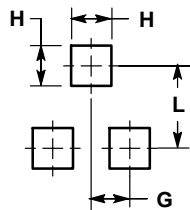
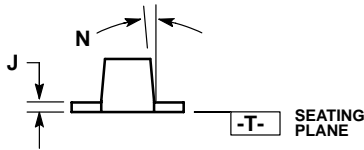
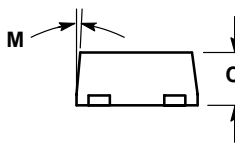
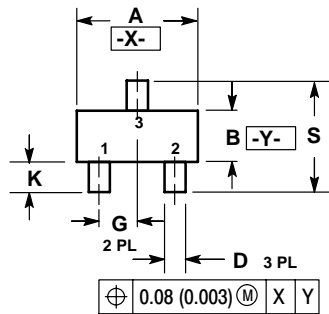


Fig. 3 OUTPUT CURRENT VS INPUT VOLTAGE

**LDTA114EET1G Series, S-LDTA114EET1G Series****TYPICAL ELECTRICAL CHARACTERISTICS – LDTA114EET1G****Fig. 5 INPUT VOLTAGE VS OUTPUT CURRENT**

# LDTA114EET1G Series, S-LDTA114EET1G Series

SC-89



RECOMMENDED PATTERN OF SOLDER PADS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067