

Bias Resistor Transistor

PNP Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

LDTA115TWT1G

● **Applications**

Inverter, Interface, Driver

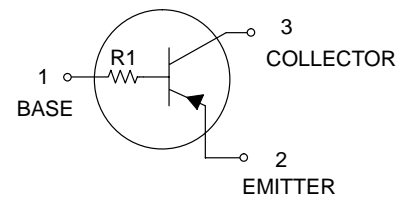
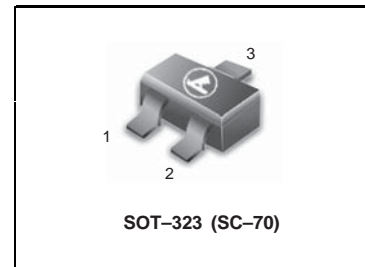
● **Features**

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making the device design easy.

- We declare that the material of product compliance with RoHS requirements.

● **Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V _{CB0}	-50	V
Collector-emitter voltage	V _{CEO}	-50	V
Emitter-base voltage	V _{EBO}	-5	V
Collector current	I _c	-100	mA
Collector Power dissipation	P _c	200	mW
Junction temperature	T _j	150	°C
Storage temperature	T _{stg}	-55 to +150	°C



DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTA115TWT1G	6U	100	-	3000/Tape & Reel
LDTA115TWT3G	6U	100	-	10000/Tape & Reel

● **Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV _{CB0}	-50	-	-	V	I _c = -50μA
Collector-emitter breakdown voltage	BV _{CEO}	-50	-	-	V	I _c = -1mA
Emitter-base breakdown voltage	BV _{EBO}	-5	-	-	V	I _E = -50μA
Collector cutoff current	I _{cBO}	-	-	-0.5	μA	V _{CB} = -50V
Emitter cutoff current	I _{EBO}	-	-	-0.5	μA	V _{EB} = -4V
Collector-emitter saturation voltage	V _{CE(sat)}	-	-	-0.3	V	I _c /I _B = -1mA/-0.1mA
DC current transfer ratio	h _{FE}	100	250	600	-	I _c = -1mA , V _{CE} = -5V
Input resistance	R ₁	70	100	130	kΩ	-
Transition frequency	f _T *	-	250	-	MHz	V _{CE} = -10V , I _E =5mA , f=100MHz

*Characteristics of built-in transistor

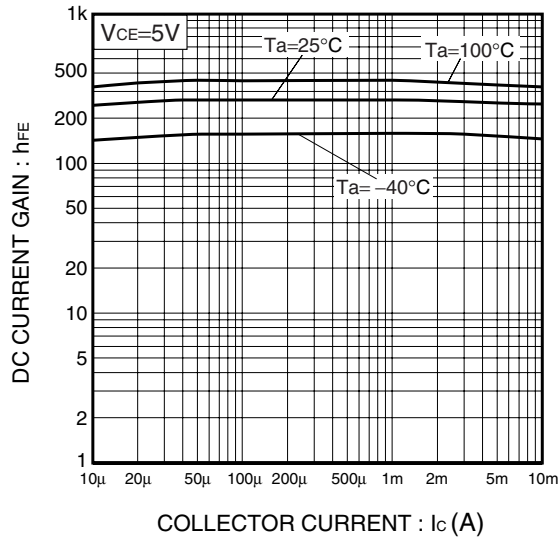
LDTA115TWT1G
●Electrical characteristic curves


Fig.1 DC current gain vs. Collector current

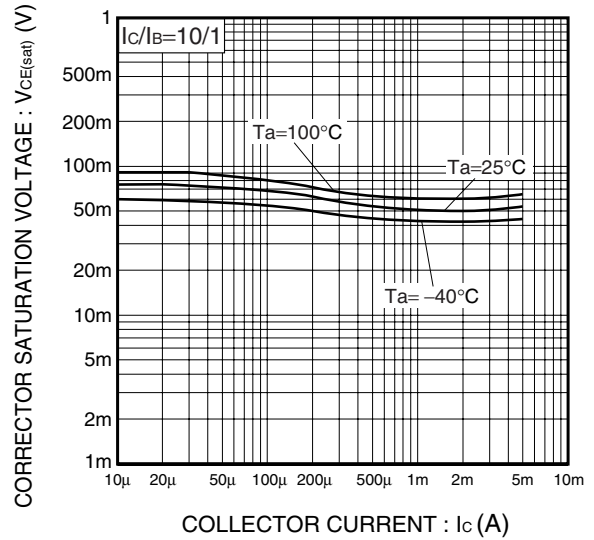
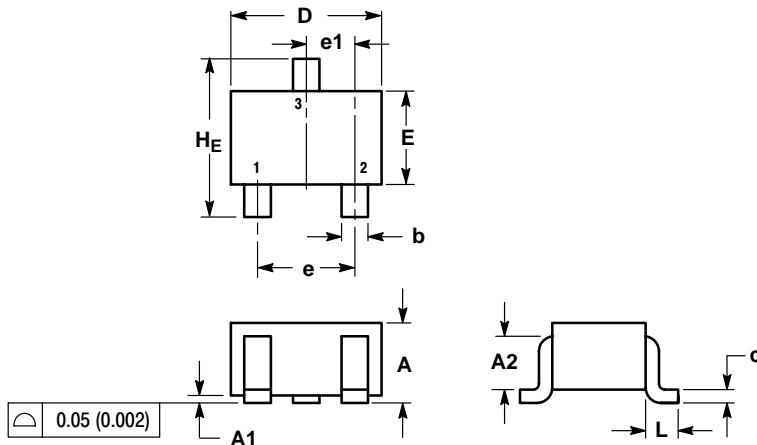


Fig.2 Collector-Emmitter saturation voltage vs. Collector current

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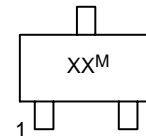
SC-70 (SOT-323)



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.7 REF			0.028 REF		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.425 REF			0.017 REF		
HE	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC MARKING DIAGRAM



XX = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*

