

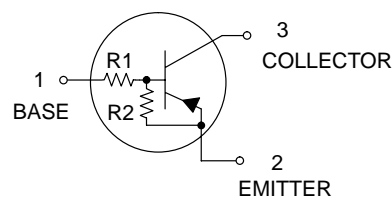
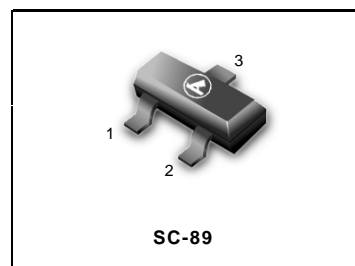
# Bias Resistor Transistor

## PNP Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

This new digital transistor is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-89 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count

**LDTA124EET1**



### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CBO}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mA <sub>dc</sub>

### DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTA124EET1	6B	22	22	3000/Tape & Reel

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, FR-4 Board (Note 1.) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200	mW mW/ $^\circ\text{C}$
		1.6	
Thermal Resistance, Junction to Ambient (Note 1.)	$R_{\theta JA}$	600	$^\circ\text{C}/\text{W}$
Total Device Dissipation, FR-4 Board (Note 2.) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300	mW mW/ $^\circ\text{C}$
		2.4	
Thermal Resistance, Junction to Ambient (Note 2.)	$R_{\theta JA}$	400	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

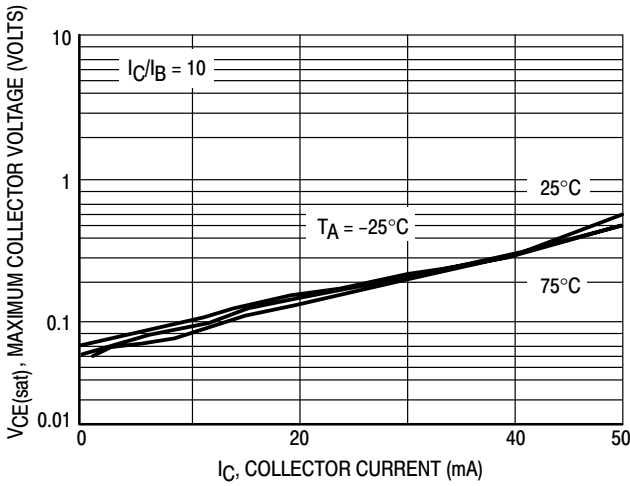
1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 Inch Pad

**LDTA124EET1****ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

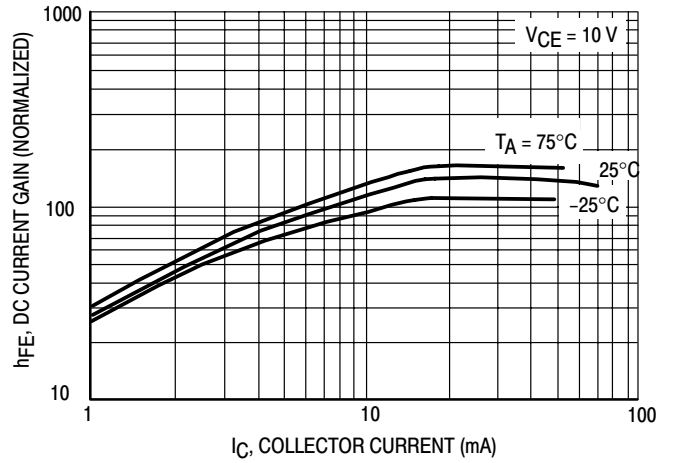
Characteristic	Symbol	Min	Typ	Max	Unit
Collector–Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	–	–	100	nAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	–	–	500	nAdc
Emitter–Base Cutoff Current ( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	–	–	0.2	mAdc
Collector–Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	Vdc
DC Current Gain ( $V_{CE} = 10\text{ V}$ , $I_C = 5.0\text{ mA}$ )	$h_{FE}$	60	100	–	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_B = 1\text{ mA}$ , $I_E = 0.3\text{ mA}$ )	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}$ )	$V_{OL}$	–	–	0.2	Vdc
Input Resistor	R1	15.4	22	28.6	k $\Omega$
Resistor Ratio	R1/R2	0.8	1.0	1.2	

**LDTA124EET1**

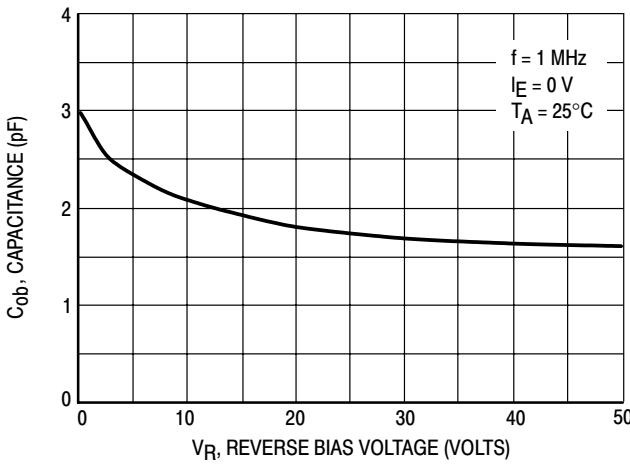
ELECTRICAL CHARACTERISTIC CURVES



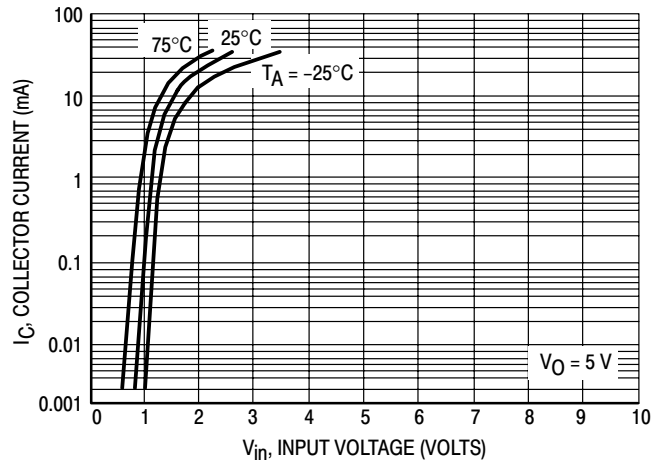
**Figure 1. VCE(sat) versus IC**



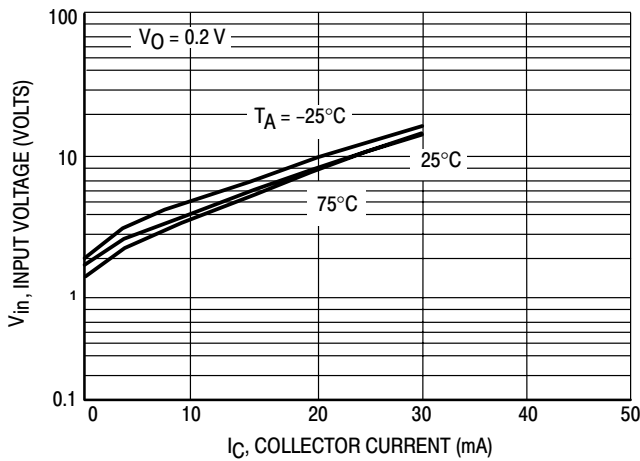
**Figure 2. DC Current Gain**



**Figure 3. Output Capacitance**



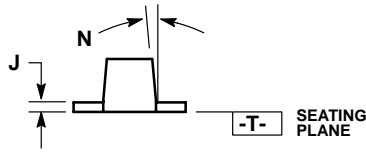
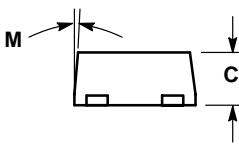
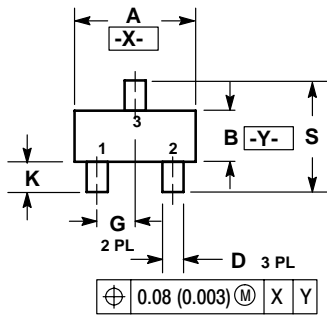
**Figure 4. Output Current versus Input Voltage**



**Figure 5. Input Voltage versus Output Current**

**LDTA124EET1**

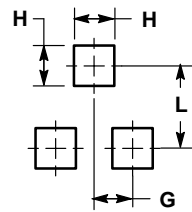
SC-89



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067



RECOMMENDED PATTERN OF SOLDER PADS