

# Bias Resistor Transistor

## NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

**LDTDG12GPT1G**

### ●Applications

Driver

### ●Features

- 1) High  $h_{FE}$ .  
300 (Min.) ( $V_{CE} / I_C = 2V / 0.5A$ )
  - 2) Low saturation voltage,  
( $V_{CE(sat)} = 0.4V$  at  $I_C / I_B = 500mA / 5mA$ )
  - 3) Built-in zener diode gives strong protection against reverse surge by L- load (an inductive load).
- We declare that the material of product compliance with RoHS requirements.

### ●Structure

 NPN epitaxial planar silicon transistor  
(with built-in resistor and zener diode)

### ●Absolute maximum ratings ( $T_a = 25^\circ C$ )

Parameter	Symbol	Limits	Unit
Collector-base voltage	$V_{CBO}$	$60 \pm 10$	V
Collector-emitter voltage	$V_{CEO}$	$60 \pm 10$	V
Emitter-base voltage	$V_{EBO}$	5	V
Collector current	$I_C$	1	A
	$I_{CP}$	2 *1	A
Collector power dissipation	$P_C$	0.5	W
		2 *2	
Junction temperature	$T_j$	150	$^\circ C$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ C$

 \*1  $P_w \leq 10ms$ , Duty cycle  $\leq 1/2$ 

 \*2 When mounted on a  $40 \times 40 \times 0.7$  mm ceramic board.

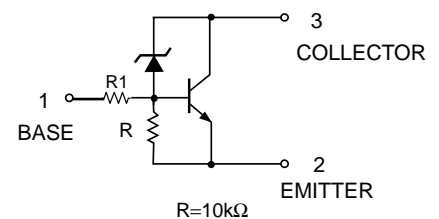
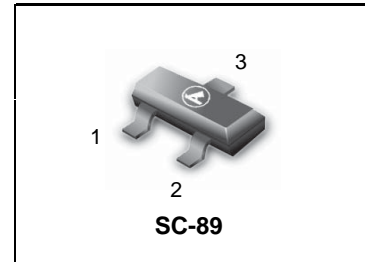
### DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTDG12GPT1G	Q7	1	22	3000/Tape & Reel
LDTDG12GPT3G	Q7	1	22	10000/Tape & Reel

### ●Electrical characteristics ( $T_a = 25^\circ C$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	$BV_{CBO}$	50	-	70	V	$I_C = 50\mu A$
Collector-emitter breakdown voltage	$BV_{CEO}$	50	-	70	V	$I_C = 1mA$
Emitter-base breakdown voltage	$BV_{EBO}$	5	-	-	V	$I_E = 720\mu A$
Collector cutoff current	$I_{CBO}$	-	-	0.5	$\mu A$	$V_{CB} = 40V$
Emitter cutoff current	$I_{EBO}$	300	-	580	$\mu A$	$V_{EB} = 4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	-	-	0.4	V	$I_C / I_B = 500mA / 5mA$
DC current transfer ratio	$h_{FE}$	300	-	-	-	$V_{CE} = 2V, I_C = 500mA$
Emitter-base resistance	R	7	10	13	$k\Omega$	-
Transition frequency	$f_t$ *	-	80	-	MHz	$V_{CE} = 5V, I_E = -0.1A, f = 30MHz$

\* Characteristics of built-in transistor



LDTDG12GPT1G

●Electrical characteristic curves

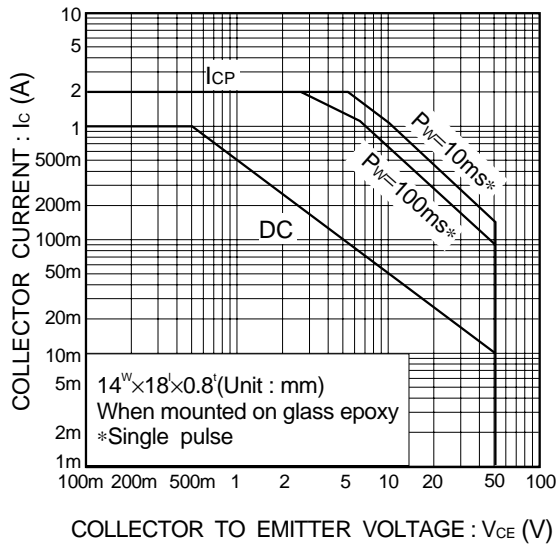


Fig.1 Safe operating area

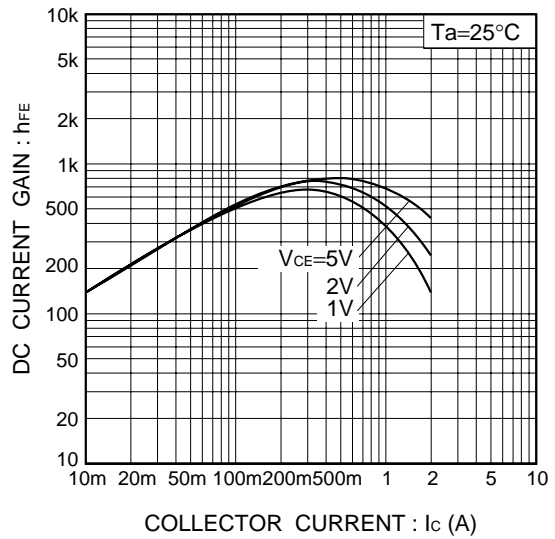


Fig.2 DC current gain vs. collector current

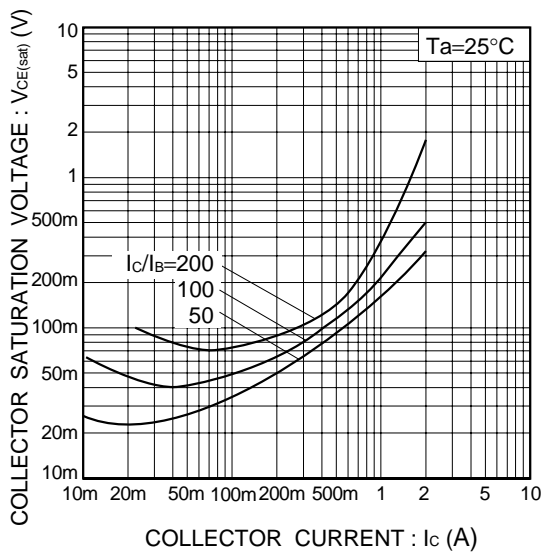
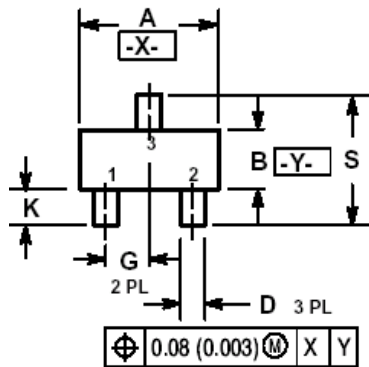
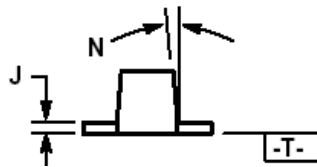
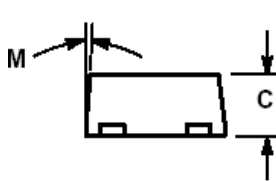


Fig.3 Collector-emitter saturation voltage vs. collector current

**LDTDG12GPT1G**
**SC-89**


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067

