Ordering number : ENA1887

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

CMOS IC

LE24CB1283 — Two Wire Serial Interface EEPROM (128K EEPROM)

Overview

The LE24CB1283 (hereinafter referred to as 'this device') is two-wire serial interface EEPROM (Electrically Erasable and Programmable ROM). This device realizes high speed and a high level reliability by SANYO's high performance CMOS EEPROM technology. This device is compatible with I^2C memory protocol, therefore it is best suited for application that requires re-writable nonvolatile parameter memory.

Functions

- Capacity : 128K bits (16k × 8 bits)
- Single supply voltage : 2.7V to 5.5V.
- Interface : Two wire serial interface (I^2C Bus*)
- Operating clock frequency : 400kHz
- Low power consumption : Standby: 2μA (max), Active(read): 1mA (max.)
- Automatic page write mode: 64 bytes
- Read mode : Sequential read and random read
- Erase/Write cycles : 10^6 cycles
- Data Retention : 20 years
- High reliability : Adopts SANYO's proprietary symmetric memory array configuration (USP6947325)
  Noise filters connected to SCL and SDA pins
  Incorporates a feature to prohibit write operations under low voltage conditions.
- Package : LE24CB1283M MFP8 (225mil)

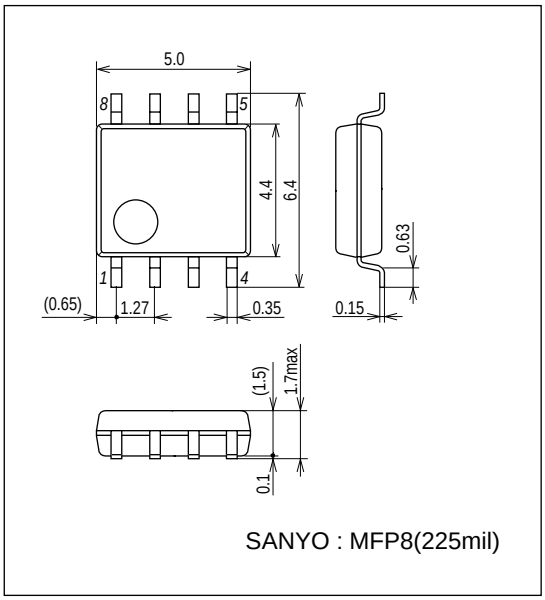
* : I^2C Bus is a trademark of Philips Corporation.

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

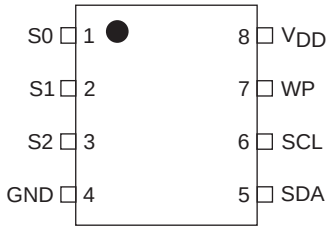
Package Dimensions

unit:mm (typ)

3032D [LE24CB1283M]



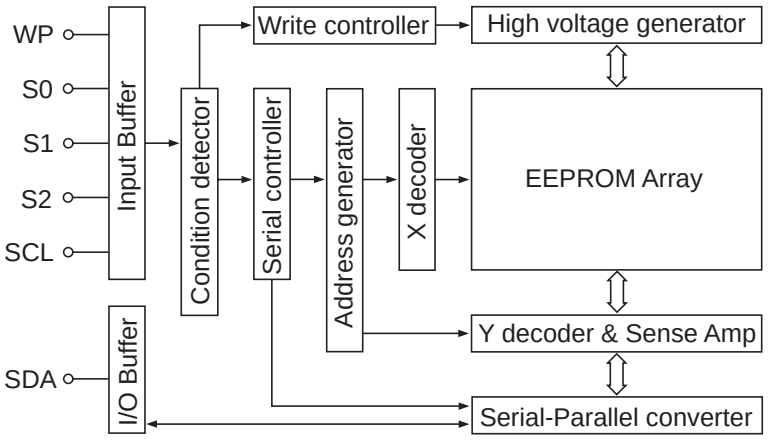
Pin Assignment



Pin Descriptions

PIN.1	S0	Slave Device Address 0
PIN.2	S1	Slave Device Address 1
PIN.3	S2	Slave Device Address 2
PIN.4	GND	Ground
PIN.5	SDA	Serial data input/output
PIN.6	SCL	Serial clock input
PIN.7	WP	Write protect
PIN.8	V_{DD}	Power supply

Block Diagram



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage			-0.5 to +6.5	V
DC input voltage			-0.5 to +5.5	V
Over-shoot voltage		Below 20ns	-1.0 to +6.5	V
Storage temperature	Tstg		-65 to +150	°C

Operating Conditions

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage			2.7 to 5.5	V
Operating temperature			-40 to +85	°C

DC Electrical Characteristics

Parameter	Symbol	Conditions	typ.	min.	max	Unit
Power supply current at reading	$I_{CC}1$	f=400kHz, V_{DD}=V_{DD} max			1	mA
Power supply current at writing	$I_{CC}2$	f=400kHz, t_{WC}=5ms, V_{DD}=V_{DD} max			5	mA
CMOS standby current	I_{SB}	V_{IN}=V_{DD} or GND, (V_{DD}= 2.7V)			2	μA
		V_{IN}=V_{DD} or GND, (V_{DD}= 5.5V)			5	μA
Input leakage current	I_{LI}	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} max	-2.0		+2.0	μA
Output leakage current	I_{LO}	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} max	-2.0		+2.0	μA
Input low voltage	V_{IL}				V_{DD}*0.3	V
Input high voltage	V_{IH}		V_{DD}*0.7			V
Output low voltage	V_{OL}	I_{OL}=0.7mA, V_{DD}1=2.7V			0.2	V
		I_{OL}=2.0mA, V_{DD}1=2.7V			0.4	V
		I_{OL}=3.0mA, V_{DD}1=5.5V			0.4	V

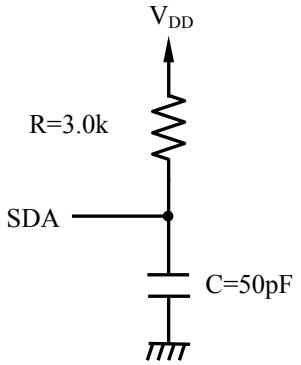
Capacitance/Ta=25°C, f=1.0MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
In/Output capacitance	$C_{I/O}$	$V_{I/O}$=0V (SDA)			10	pF
Input capacitance	C_I	V_{IN}=0V			10	pF

Note: This parameter is sampled and not 100% tested.

AC Electric Characteristics

Input pulse level	0.1*V_{DD} to 0.9*V_{DD}
Input rise / fall time	20ns
Input / output timing level	0.5*V_{DD}
Output load	50pF + Pull up resistor 3.0kΩ



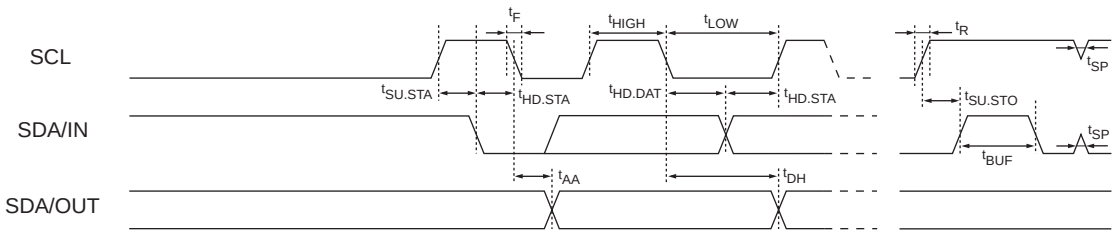
Fast Mode

Parameter	Symbol	Spec			unit
		min	typ	max	
SCL clock frequency	f_{SCLS}	0		400	kHz
SCL pulse with Low	t_{LOW}	1200			ns
SCL pulse with High	t_{HIGH}	600			ns
Access time	t_{AA}	100		900	ns
Data output hold time	t_{DH}	100			ns
Start condition setup time	$t_{SU.STA}$	600			ns
Start condition hold time	$t_{HD.STA}$	600			ns
Data in setup time	$t_{SU.DAT}$	100			ns
Data in hold time	$t_{HD.DAT}$	0			ns
Stop condition setup time	$t_{SU.STO}$	600			ns
SCL, SDA rise time	t_R			300	ns
SCL, SDA fall time	t_F			300	ns
Bus free time for next mode	t_{BUF}	1200			ns
Noise suppression time	t_{SP}			100	ns
Write time	t_{WC}			5	ms

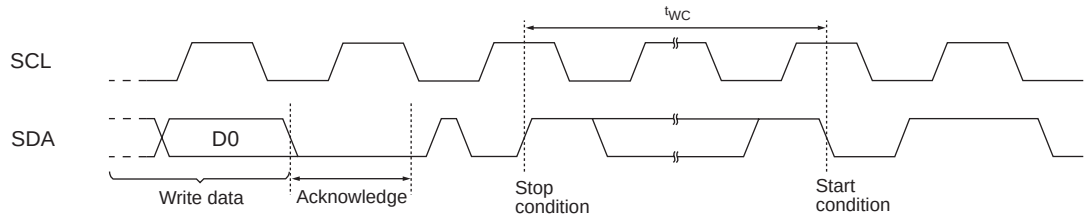
Standard Mode

Parameter	Symbol	Spec			unit
		min	typ	max	
SCL clock frequency	f_{SCLS}	0		100	kHz
SCL pulse with Low	t_{LOW}	4700			ns
SCL pulse with High	t_{HIGH}	4000			ns
Access time	t_{AA}	100		3500	ns
Data output hold time	t_{DH}	100			ns
Start condition setup time	$t_{SU.STA}$	4700			ns
Start condition hold time	$t_{HD.STA}$	4000			ns
Data in setup time	$t_{SU.DAT}$	250			ns
Data in hold time	$t_{HD.DAT}$	0			ns
Stop condition setup time	$t_{SU.STO}$	4000			ns
SCL, SDA rise time	t_R			1000	ns
SCL, SDA fall time	t_F			300	ns
Bus free time for next mode	t_{BUF}	4700			ns
Noise suppression time	t_{SP}			100	ns
Write time	t_{WC}			5	ms

Bus Timing



Write Timing



Pin Functions

SCL (serial clock)

The SCL signal is used to control serial input data timing. The SCL is used to latch input data synchronously at the rising edge and read output data synchronously at the falling edge.

SDA (serial input/output data)

The SDA pin is bidirectional for serial data transfer. It is an open-drain structure that needs to be pulled up by resistor.

WP (Write protect)

When the WP signal is high, write protections are enabled. When this signal is low, write operation for all memory arrays are allowed. The read operation is always activated irrespective of the WP pin status.

S0/S1/S2 (Slave address)

When many devices are connected on the same bus, the S0/S1/S2 are used to select the device. The S0/S1/S2 must be tied to V_{DD} or GND.

Functional Description

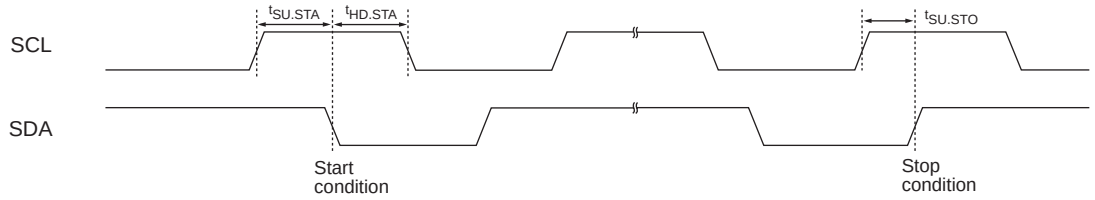
The device supports the I^2C protocol. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device.

1. Start condition

A Start condition is needs to start the EEPROM operation, it is to set falling edge of the SDA while the SCL is stable in the high status.

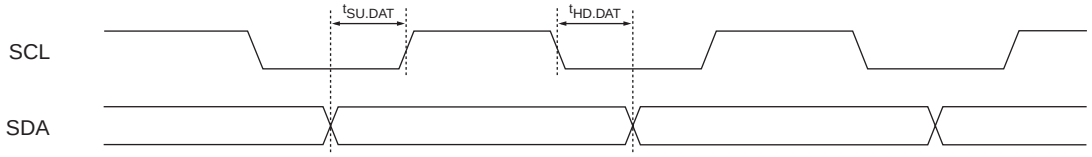
2. Stop condition

A Start condition is identified by rising edge of the SDA signal while the SCL is stable in the high status. The device becomes the standby mode from a Read operation by a Stop condition. In a write sequence, a stop condition is trigger to start the internal write cycle. After the internally write cycle time which is specified as t_{WC}, the device enters a standby mode.



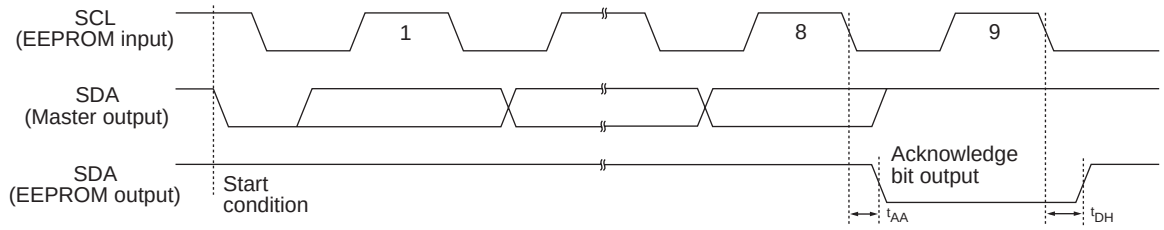
3. Data Input

During data input, the device latches the SDA on the rising edge of the SCL. For correct the operation, the SDA must be stable during the rising edge of the SCL.



4. Acknowledge

The Acknowledge Bit is used to indicate a successful byte data transfer. The receiver sends a zero to acknowledge that it has received each word (Device Code, Slave Address etc) from the transmitter.

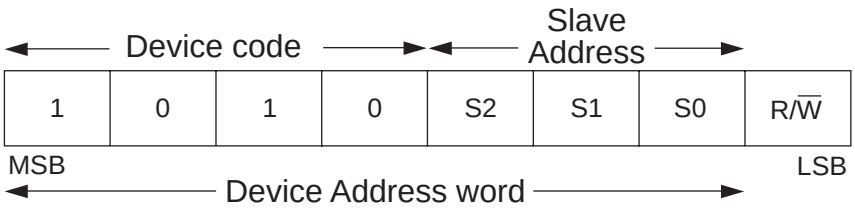


5. Device addressing

To transmit between the bus master and slave device (EEPROM), the master must send a Start condition to the EEPROM. The device address word of the EEPROM consists of 4-bit Device Code, 3-bit Slave Device address code and 1-bit read/write code. By sending these, it becomes possible to communicate between the bus master and the EEPROM.

The upper 4-bit of the device address word are called the Device Code, the Device Code of the EEPROM uses 1010b fixed code. This device has the 3-bit of the Slave Device address as the Slave address (S0, S1, S2), so it can connect up to eight device on the bus.

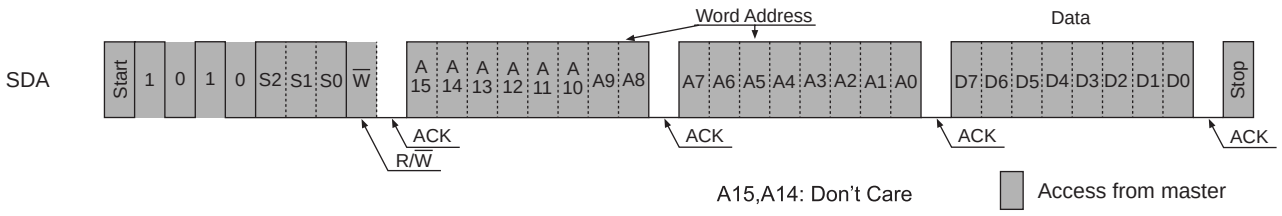
When the Device Code is received on the SDA, the device only responds if Slave address pin tied to V_{DD} or GND is the same as the Slave address signal input. The 8th bit is the read/write bit. The bit is set to 1 for Read operation and 0 for Write operation. If a match occurs on the Device Code, the corresponding device gives an acknowledgement on SDA during the 9th bit time. If device does not match the Device Code, it deselects itself from the bus, and goes into the Standby mode. Use the Random Read command when you execute reading after the slave device was switched.



6 EEPROM write operation

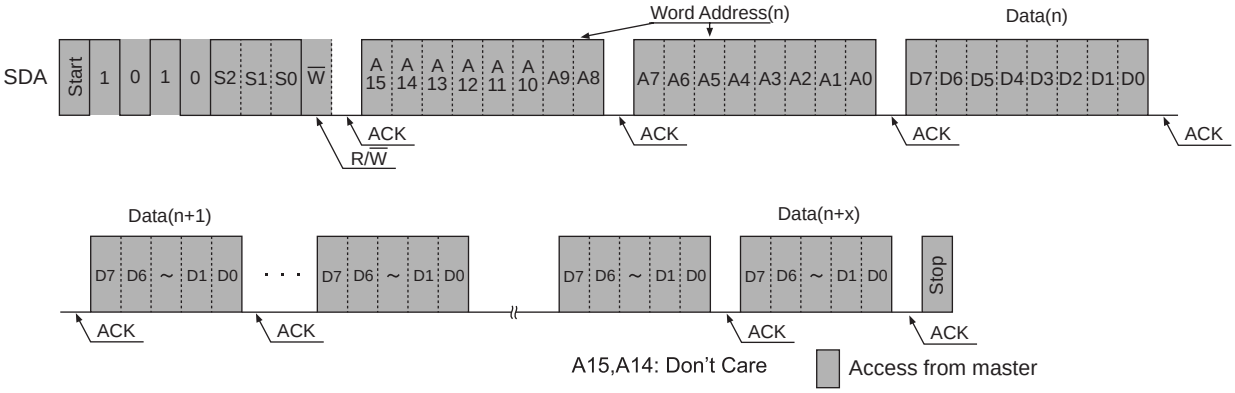
6-1. Byte writes

The write operation requires a 7-bit device address word with the 8th bit = 0(write). Then the EEPROM sends acknowledgement 0 at the 9th clock cycle. After these, the EEPROM receives word address (A15 to A8), and the EEPROM outputs acknowledgement 0. And then, the EEPROM receives word address (A7 to A0), and the EEPROM outputs acknowledgement 0. Then the EEPROM receives 8-bit write data, the EEPROM outputs acknowledgement 0 after receipt of write data. If the EEPROM receives a stop condition, the EEPROM enters an internally timed (t_{WC}) write cycle and terminates receipt of inputs until completion of the write cycle.



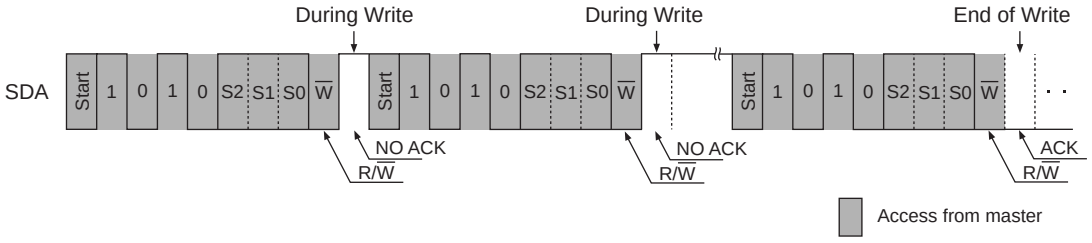
6-2. Page writes

The Page write allows up to 64 bytes to be written in a single write cycle. The page write is the same sequence as the byte writes except for inputting the more write data. The page write is initiated by a start condition, device code, device address, memory address (n) and write data (n) with every 9th bit acknowledgement. The device enters the page write operation if this device receives more write data (n+1) instead of receiving a stop condition. The page address (A0 to A5) bits are automatically incremented on receiving write data (n+1). The device can continue to receive write data up to 64 bytes. If the page address bits reach the last address of the page, the page address bits will roll over to the first address of the same page and previous write data will be overwritten. After these, if the device receives a stop condition, the device enters an internally timed ($t_{WC} \times (n+x)$) write cycle and terminates receipt of inputs until completion of the write cycle.



6-3. Acknowledge polling

The Acknowledge polling operation is used to show if the EEPROM is in an internally timed write cycle or not. This operation is initiated by the stop condition after inputting write data. This requires the 8-bit device address word with the 8th bit = 0 (write) following the start condition during an internally timed write cycle. If the EEPROM is busy with the internal write cycle, no acknowledge will be returned. If the EEPROM has terminated the internal write cycle, it responds with an acknowledge. The terminated write cycle of the EEPROM can be known by this operation.

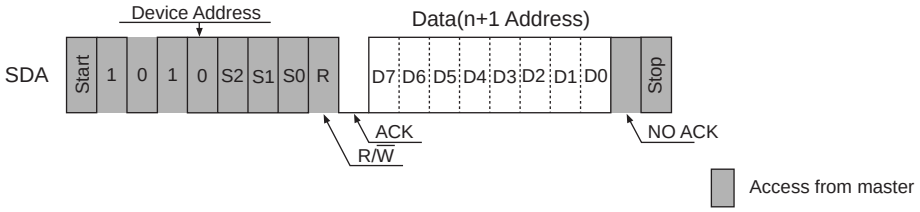


7 EEPROM read operations

7-1. Current address reading

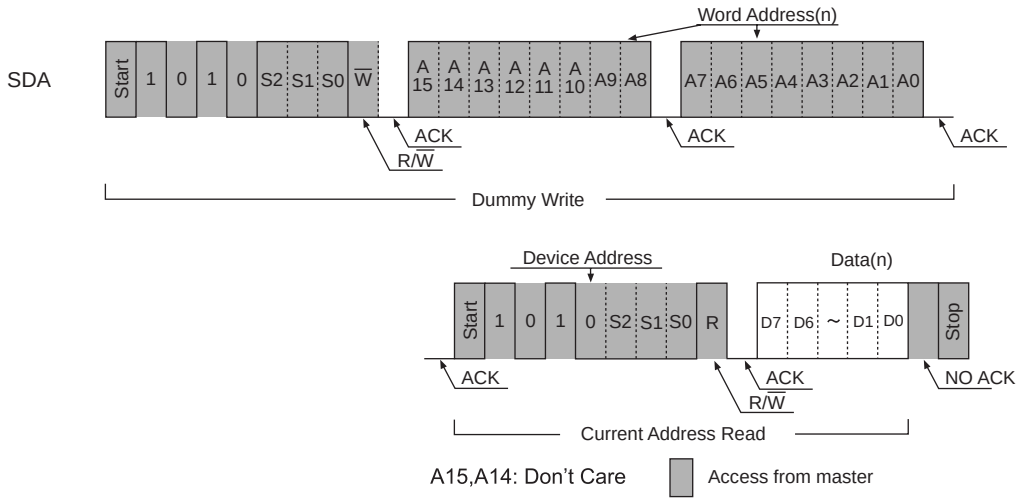
The device has an internal address counter. It maintains that last address during the last read or write operation, with incremented by one. The current address read accesses the address kept by the internal address counter. After receiving a start condition and the device address word with the 8th bit = 1 (read), the EEPROM outputs the 8-bit current address data from following acknowledgement 0. If the EEPROM receives acknowledgement 1 and a following stop condition, the EEPROM stops the read operation and is returned to a standby mode. In case the EEPROM has accessed the last address of the last page at previous read operation, the current address will roll over and returns to zero address. In case EEPROM has accessed the last address of the last page at previous write operation, the current address roll over within page addressing and returns to the first address in the same page.
The current address is valid while power is ON. After power on, the current address will be reset (all 0).

Note: After the page writes operation, the current address is the specified memory address in the last page write. If the write data is more than 64-bytes.



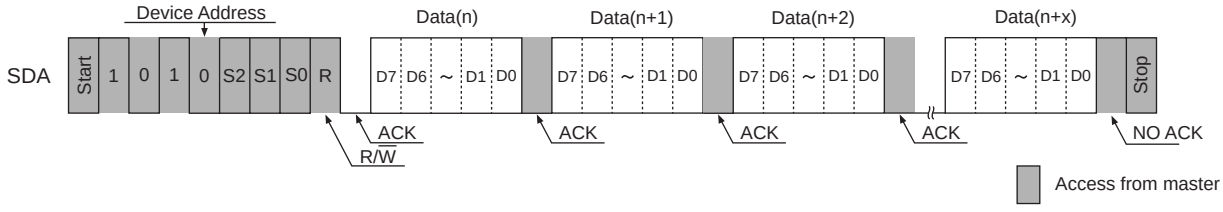
7-2. Random read

The random read requires a dummy write to set read address. The EEPROM receives a start condition and the device address word with the 8th bit = 0 (write), the memory address. The EEPROM outputs acknowledgement 0 after receiving memory address then enters a current address read with receiving a start condition. The EEPROM outputs the read data of the address which was defined in the dummy write operation. After receiving no acknowledgement and a following stop condition, the EEPROM stop the random read operation and returns to standby mode.



7-3. Sequential read

The sequential read operation is initiated by either a current address read or random read. If the EEPROM receives acknowledgement 0 after 8-bit read data, the read address is incremented and the next 8-bit read data outputs. The current address will roll over and returns address zero if it reaches the last address of the last page. The sequential read can be continued after roll over. The sequential read is terminated if the EEPROM receives no acknowledgement and a following stop condition.

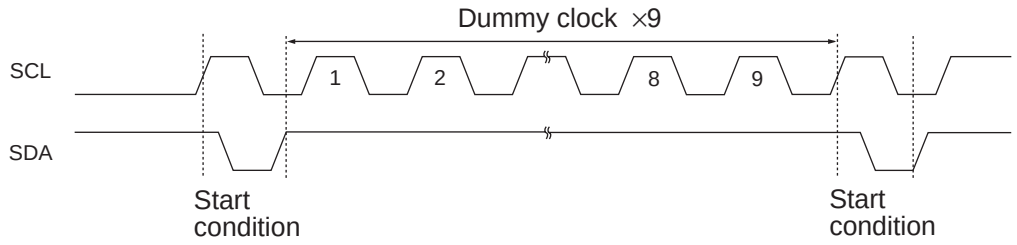


Application Notes

1) Software reset function

Software reset (start condition + 9 dummy clock cycles + start condition), shown in the figure below, is executed in order to avoid erroneous operation after power-on and to reset while the command input sequence. During the dummy clock input period, the SDA bus must be opened (set to high by a pull-up resistor). Since it is possible for the ACK output and read data to be output from the EEPROM during the dummy clock period, forcibly entering H will result in an overcurrent flow.

Note that this software reset function does not work during the internal write cycle.



2) Pull-up resistor of SDA pin

Due to the demands of the I^2C bus protocol function, the SDA pin must be connected to a pull-up resistor (with a resistance from several kΩ to several tens of kΩ) without fail. The appropriate value must be selected for this resistance (R_{PU}) on the basis of the V_{IL} and I_{IL} of the microcontroller and other devices controlling this product as well as the V_{OL}–I_{OL} characteristics of the product. Generally, when the resistance is too high, the operating frequency will be restricted; conversely, when it is too low, the operating current consumption will increase.

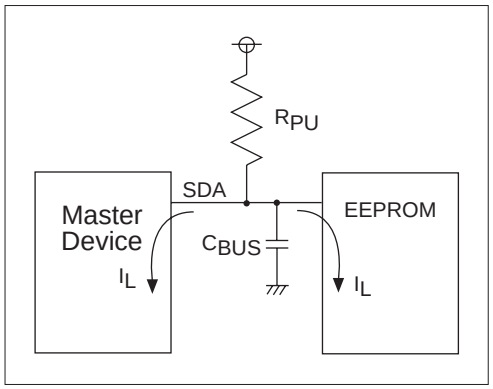
R_{PU} maximum resistance

The maximum resistance must be set in such a way that the bus potential, which is determined by the sum total (I_L) of the input leaks of the devices connected to the SDA bus and by R_{PU}, can completely satisfy the input high level (V_{IH} min) of the microcontroller and EEPROM. However, a resistance value that satisfies SDA rise time t_R and fall time t_F must be set.

R_{PU} maximum value = $(V_{DD} - V_{IH})/I_L$

Example: When V_{DD}=3.0V and I_L= 2μA

R_{PU} maximum value = (3.0V – 3.0V × 0.8)/2μA = 300kΩ



R_{PU} minimum value

A resistance corresponding to the low-level output voltage (V_{OL} max) of SANYO's EEPROM must be set.

R_{PU} minimum value = $(V_{DD} - V_{OL})/I_{OL}$

Example: When V_{DD}=3.0V, V_{OL} = 0.4V and I_{OL} = 1mA

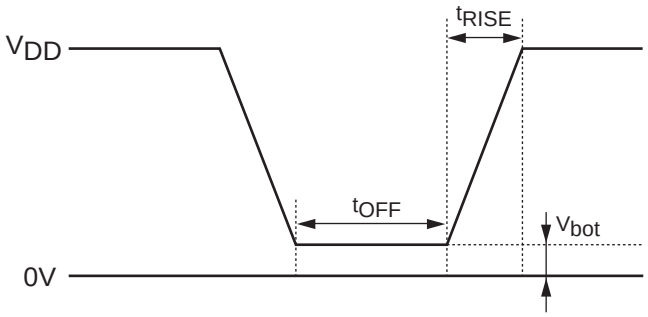
R_{PU} minimum value = (3.0V – 0.4)/1mA = 2.6kΩ

Recommended R_{PU} setting

R_{PU} is set to strike a good balance between the operating frequency requirements and power consumption. If it is assumed that the SDA load capacitance is 50pF and the SDA output data strobe time is 500ns, R_{PU} will be about R_{PU} = 500ns/50pF = 10kΩ.

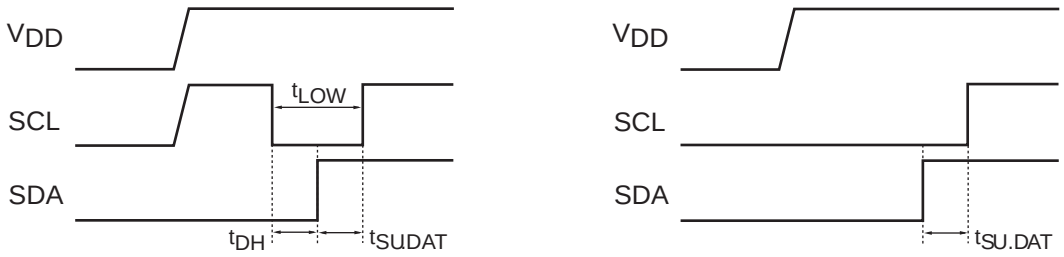
3) Precautions when turning on the power
This product contains a power-on reset circuit for preventing the inadvertent writing of data when the power is turned on. The following conditions must be met in order to ensure stable operation of this circuit. No data guarantees are given in the event of an instantaneous power failure during the internal write operation.

Item	Symbol	min	typ	max	unit
Power rise time	t_{RISE}			100	ms
Power off time	t_{OFF}	10			ms
Power bottom voltage	V_{bot}			0.2	V



Notes:
1) The SDA pin must be set to high and the SCL pin to low or high.
2) Steps must be taken to ensure that the SDA and SCL pins are not placed in a high-impedance state.

A. If it is not possible to satisfy the instruction 1 in Note above, and SDA is set to low during power rise
After the power has stabilized, the SCL and SDA pins must be controlled as shown below, with both pins set to high.



B. If it is not possible to satisfy the instruction 2 in Note above
After the power has stabilized, software reset must be executed.

C. If it is not possible to satisfy the instructions both 1 and 2 in Note above
After the power has stabilized, the steps in A must be executed, then software reset must be executed.

4) Noise filter for the SCL and SDA pins
This product contains a filter circuit for eliminating noise at the SCL and SDA pins. Pulses of 100ns or less are not recognized because of this function.

5) Function to inhibit writing when supply voltage is low
This product contains a supply voltage monitoring circuit that inhibits inadvertent writing below the guaranteed operating supply voltage range. The data is protected by ensuring that write operations are not started at voltages (typ.) of 1.3V and below.

6) Notes on write protect operation

This product prohibits all memory arrays writing when the WL pin is high. To ensure full write protection, the WP is set high for all periods from the start condition to the stop condition, and the conditions below must be satisfied.

symbol	Parameter	spec			Unit
		min	typ	max	
$t_{SU.WP}$	WP Setup time	600			ns
$t_{HD.WP}$	WP Hold time	600			ns