



SANYO Semiconductors

DATA SHEET

LE25LB643 — Serial SPI EEPROM (SPI Bus) (64Kbit)

Overview

The LE25LB643 is a 64Kbit EEPROM that supports serial peripheral interface (SPI). It realizes high speed operation and high level reliability by incorporating SANYO's high performance CMOS EEPROM technology. The interface is compatible with SPI bus protocol, therefore, it is best suited for applications that require small-scale rewritable nonvolatile parameter memory. Moreover, the LE25LB643 has a 32 bytes page rewrite function that provides rapid data rewriting.

Features

- Capacity : 64Kbits (8K×8bits)
- Single supply voltage : 1.8V to 3.6V
- Serial interface : SPI Mode0, Mode3 supported
- Operating clock frequency : 5MHz (2.5V to 3.6V), 3MHz (1.8V to 3.6V)
- Low current dissipation : Standby : 3μA (max.)
: Active (Read) : 1mA (max.)
: Active (Rewrite) : 3mA (max.)
- Page write function : 32bytes
- Rewrite time : 10ms
- Number of rewrite times : 10⁶ times/Address
- Data retention period : 20years
- High reliability : Adopts SANYO's proprietary symmetric memory array configuration (USP6947325)
Incorporates a feature to prohibit write operations under low voltage conditions.

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

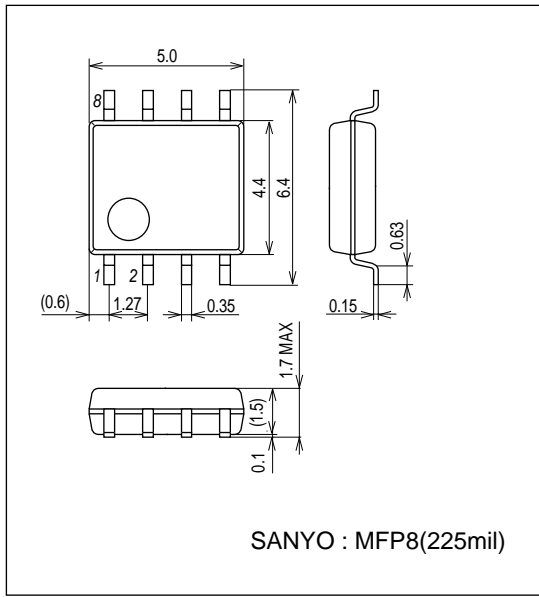
SANYO Semiconductor Co., Ltd.

<http://semicon.sanyo.com/en/network>

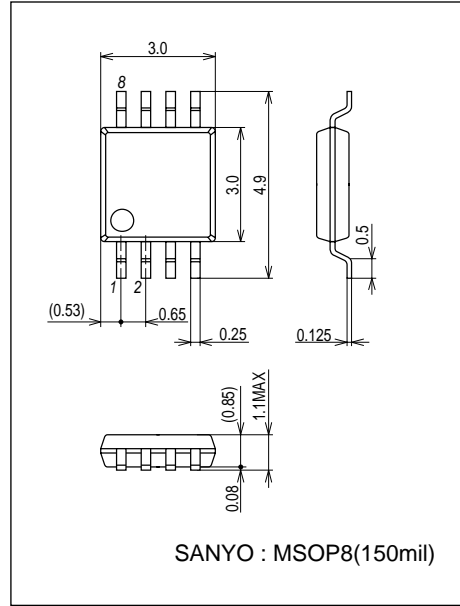
LE25LB643

Package Dimensions

unit : mm (typ)
3032E [LE25LB643M]



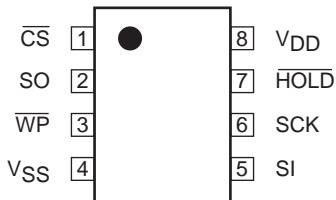
unit : mm (typ)
3245B [LE25LB643TT]



Packages

MFP8 (225mil) : LE25LB643M
MSOP8 (150mil) : LE25LB643TT

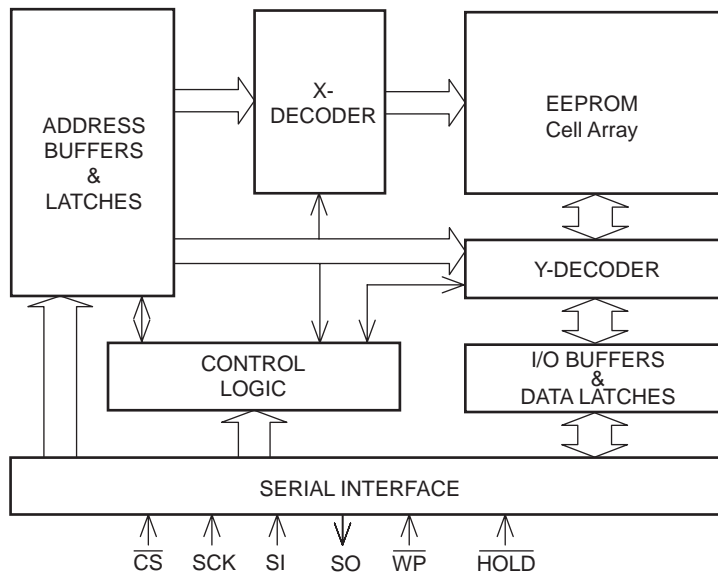
Pin Assignment



Pin Descriptions

PIN.1	\overline{CS}	Chip select
PIN.2	SO	Serial data output
PIN.3	\overline{WP}	Write protect
PIN.4	V_{SS}	Ground
PIN.5	SI	Serial data input
PIN.6	SCK	Serial clock
PIN.7	\overline{HOLD}	Hold
PIN.8	V_{DD}	Power supply

Block Diagram



LE25LB643

Specifications

Absolute Maximum Rating/If an electrical stress exceeding the maximum rating is applied, the device may be damaged.

Parameter	Symbol	Conditions	Ratings	Unit
Storage temperature			-65 to +150	°C
Supply voltage			-0.5 to 4.6	V
DC input voltage			-0.5 to $V_{DD}+0.5$	V
Overshoot voltage (below 20ns)			-1.0 to $V_{DD}+0.5$	V

Operating Conditions

Parameter	Symbol	Conditions	Ratings	Unit
Operating temperature			-40 to +85	°C
Operating supply voltage			1.8 to 3.6	V

DC Electrical Characteristics

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current when reading	I_{CCR}	$\overline{CS} = 0.1V_{DD}$, $\overline{HOLD} = \overline{WP} = 0.9V_{DD}$ $SI = 0.1V_{DD}/0.9V_{DD}$, $SO = \text{Open}$ Operating frequency = 5MHz, $V_{DD} = 3.6V$			1	mA
		$\overline{CS} = 0.1V_{DD}$, $\overline{HOLD} = \overline{WP} = 0.9V_{DD}$ $SI = 0.1V_{DD}/0.9V_{DD}$, $SO = \text{Open}$ Operating frequency = 5MHz, $V_{DD} = 2.5V$			0.5	mA
		$\overline{CS} = 0.1V_{DD}$, $\overline{HOLD} = \overline{WP} = 0.9V_{DD}$ $SI = 0.1V_{DD}/0.9V_{DD}$, $SO = \text{Open}$ Operating frequency = 3MHz, $V_{DD} = 1.8V$			0.3	mA
Supply current when writing	I_{CCW}	$V_{DD} = 3.6V$, $V_{IN} = 0.1V_{DD}/0.9V_{DD}$			3	mA
CMOS standby current	I_{SB}	$\overline{CS} = V_{DD}$, $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 3.6V$			3	μA
		$\overline{CS} = V_{DD}$, $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 2.5V$			2	μA
Input leakage current	I_{LI}	$V_{IN} = V_{SS}$ to V_{DD} , $V_{DD} = V_{DD} \text{ max.}$	-2		2	μA
Output leakage current	I_{LO}	$V_{IN} = V_{SS}$ to V_{DD} , $V_{DD} = V_{DD} \text{ max.}$	-2		2	μA
Input low voltage	V_{IL}	$V_{DD} = V_{DD} \text{ max.}$	-0.3		$0.3V_{DD}$	V
Input high voltage	V_{IH}	$V_{DD} = V_{DD} \text{ min.}$	$0.7V_{DD}$		$V_{DD}+0.3$	V
Output low voltage	V_{OL1}	$I_{OL} = 3.0mA$, $V_{DD} = 2.5V$ to $3.6V$			0.4	V
	V_{OL2}	$I_{OL} = 0.7mA$, $V_{DD} = 1.8V$ to $3.6V$			0.2	V
Output high voltage	V_{OH1}	$I_{OH} = -0.4mA$, $V_{DD} = 2.5V$ to $3.6V$	$0.8V_{DD}$			V
	V_{OH2}	$I_{OH} = -0.1mA$, $V_{DD} = 1.8V$ to $3.6V$	$0.8V_{DD}$			V

Capacitance at $T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Output pin capacitance	C_{DQ}	$V_{DQ} = 0V$			12	pF
Input pin capacitance	C_{IN}	$V_{IN} = 0V$			6	pF

Note : These parameters are sampled and not 100% tested.

AC Electrical Characteristics

Input pulse level	$0.2 \times V_{DD}$ to $0.8 \times V_{DD}$
Input pulse rise/fall time	10ns
Output detection voltage	$0.5 \times V_{DD}$
Output load	30pF

LE25LB643

AC Characteristics (at FCLK = 5MHz)/V_{DD} = 2.5V to 3.6V

Parameter	Symbol	Conditions	min	typ	max	Unit
Clock frequency	FCLK				5	MHz
SCK logic high level pulse width	t _{CLHI}		90			ns
SCK logic low level pulse width	t _{CLLO}		90			ns
Input signal rise/fall time	t _{RF}				1	us
$\overline{\text{CS}}$ setup time	t _{CSS}		90			ns
SCK setup time	t _{CLS}		90			ns
Data setup time	t _{DS}		20			ns
Data hold time	t _{DH}		30			ns
$\overline{\text{CS}}$ hold time	t _{CSH}		90			ns
SCK hold time	t _{CLH}		90			ns
$\overline{\text{CS}}$ standby pulse width	t _{CPH}		90			ns
$\overline{\text{CS}}$ output high impedance time	t _{CHZ}				150	ns
SCK output data time	t _v				80	ns
Output data hold time	t _{HO}		0			ns
$\overline{\text{WP}}$ setup time	t _{WPS}		30			ns
$\overline{\text{WP}}$ hold time	t _{WPH}		30			ns
$\overline{\text{HOLD}}$ setup time	t _{HS}		30			ns
$\overline{\text{HOLD}}$ hold time	t _{HH}		30			ns
$\overline{\text{HOLD}}$ output low impedance time	t _{HLz}				50	ns
$\overline{\text{HOLD}}$ output high impedance time	t _{HHz}				100	ns
Write cycle time	t _{WC}				5	ms
SCK output low impedance time	t _{CLZ}		0			ns

AC Characteristics (at FCLK = 3MHz)/V_{DD} = 1.8V to 3.6V

Parameter	Symbol	Conditions	min	typ	max	Unit
Clock frequency	FCLK				3	MHz
SCK logic high level pulse width	t _{CLHI}		120			ns
SCK logic low level pulse width	t _{CLLO}		120			ns
Input signal rise/fall time	t _{RF}				1	us
$\overline{\text{CS}}$ setup time	t _{CSS}		100			ns
SCK setup time	t _{CLS}		100			ns
Data setup time	t _{DS}		30			ns
Data hold time	t _{DH}		50			ns
$\overline{\text{CS}}$ hold time	t _{CSH}		100			ns
SCK hold time	t _{CLH}		150			ns
$\overline{\text{CS}}$ standby pulse width	t _{CPH}		120			ns
$\overline{\text{CS}}$ output high impedance time	t _{CHZ}				200	ns
SCK output data time	t _v				150	ns
Output data hold time	t _{HO}		0			ns
$\overline{\text{WP}}$ setup time	t _{WPS}		30			ns
$\overline{\text{WP}}$ hold time	t _{WPH}		30			ns
$\overline{\text{HOLD}}$ setup time	t _{HS}		30			ns
$\overline{\text{HOLD}}$ hold time	t _{HH}		30			ns
$\overline{\text{HOLD}}$ output low impedance time	t _{HLz}				120	ns
$\overline{\text{HOLD}}$ output high impedance time	t _{HHz}				120	ns
Write cycle time	t _{WC}				10	ms
SCK output low impedance time	t _{CLZ}		0			ns

Table 1 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	nth bus cycle
Write enable (WREN)	06h						
Write disable (WRDI)	04h						
Status register read (RDSR)	05h						
Status register write (WRSR)	01h	DATA					
Read (READ)	03h	A15-A8	A7-A0				
Write (WRITE)	02h	A15-A8	A7-A0	PD *1	PD *1	PD *1	PD *1

Explanatory notes for Table 1

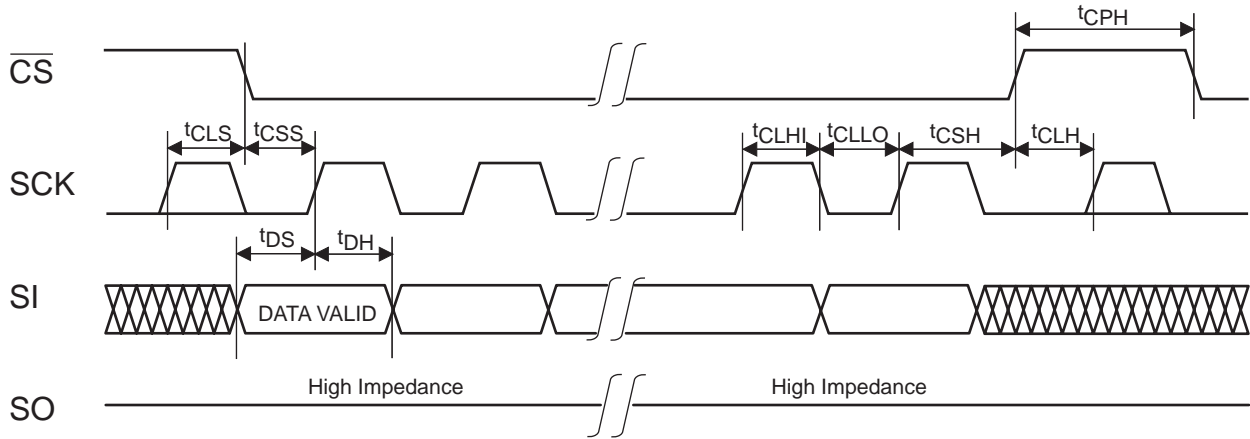
The "h" following each code indicates that the number given is in hexadecimal notation.

Addresses A15 - A13 for all commands are "don't care."

*1: "PD" stands for page program data. Any amount of data from 1 to 32 bytes is input.

Figure 2 Serial Input Timing

(SPI Mode 0)



(SPI Mode 3)

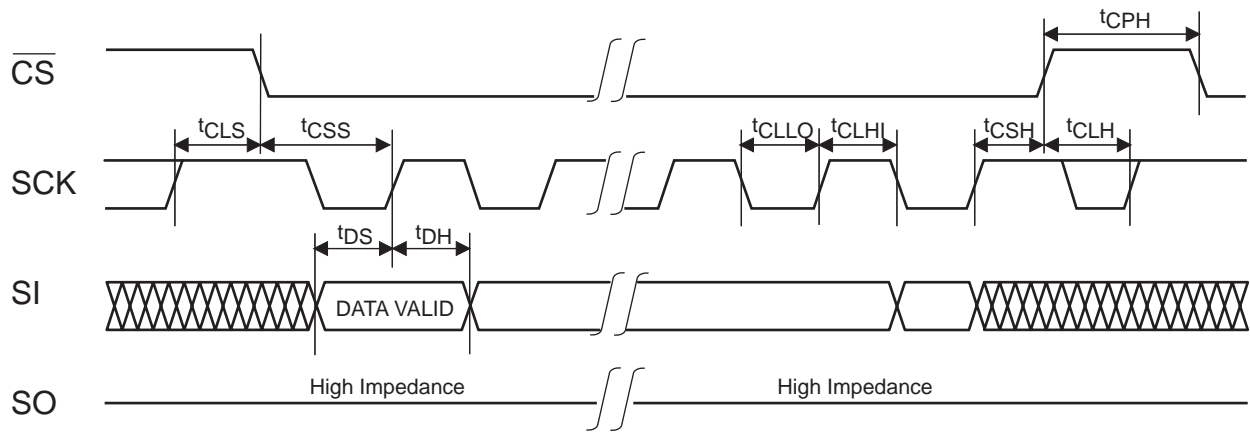
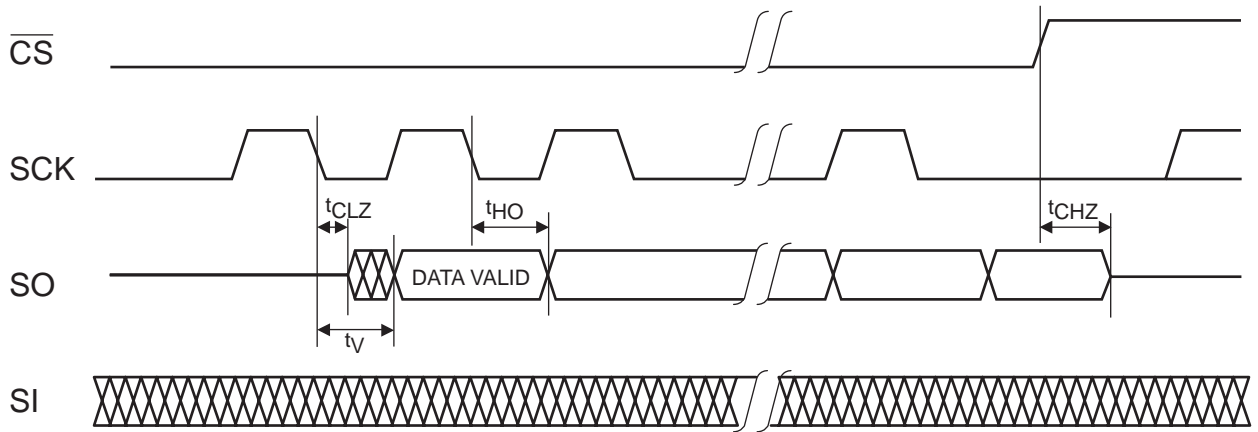
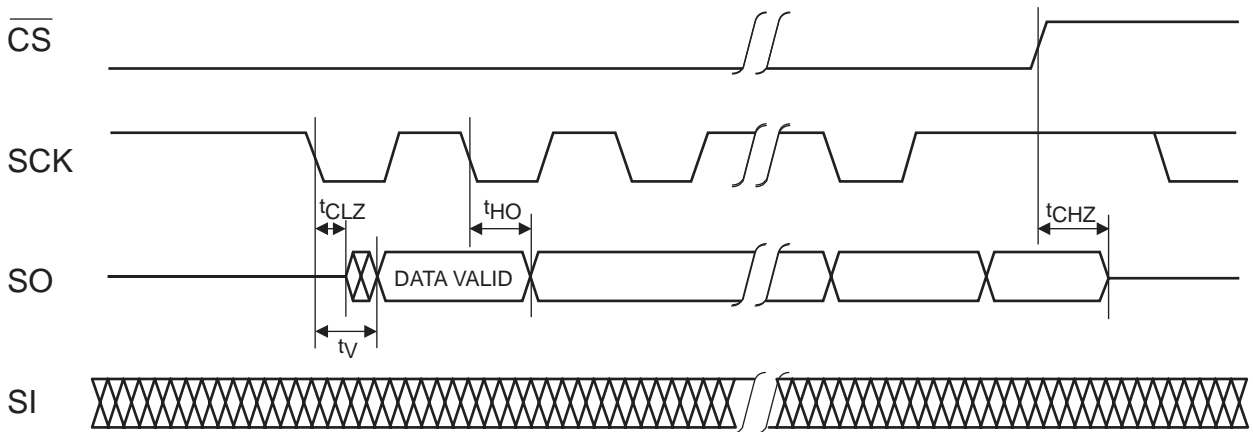


Figure 3 Serial Output Timing

(SPI Mode 0)



(SPI Mode 3)



Description of Commands and Their Operations

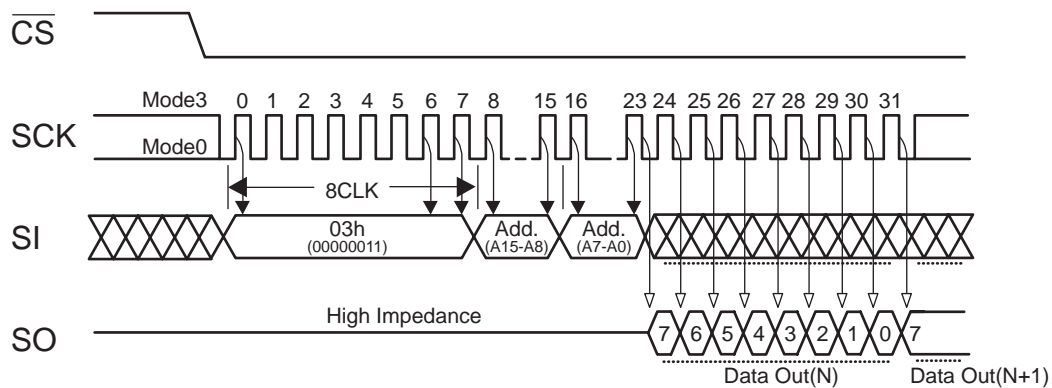
“Table 1 Command Settings” provides a list and overview of the commands. A detailed description of the functions and operations corresponding to each command is presented below.

1. Read (READ)

Consisting of the first through third bus cycles, the read command inputs the 16-bit addresses following (03h), and the data in the designated addresses is output synchronized to SCK. The data is output from SO on the falling edge of third bus cycle bit0 as a reference. “Figure 4 READ” shows the timing waveforms.

When SCK is input continuously after the read command has been input and the data in the designated addresses has been output, the address is automatically incremented inside the device while SCK is being input, and the corresponding data is output in sequence. If the SCK input is continued after the internal address arrives at the highest address, the internal address returns to the lowest address (0000h), and data output is continued. By setting the logic level of \overline{CS} to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 4 READ



- Addresses A15 - A13 are “don’t care.”
- In synchronization with the rising edges of 0 to 23 clock signals, the command is identified and the addresses are taken in through SI.
- In synchronization with the falling edges of 23 clock signal or later, the data is output to SO.

2. Status Registers

The status registers read the operating and setting statuses inside the device from outside (status register read) and set the protect information (status register write). There are 8 bits in total, and “Table 2 Status Registers” gives the significance of each bit.

Table 2 Status Registers

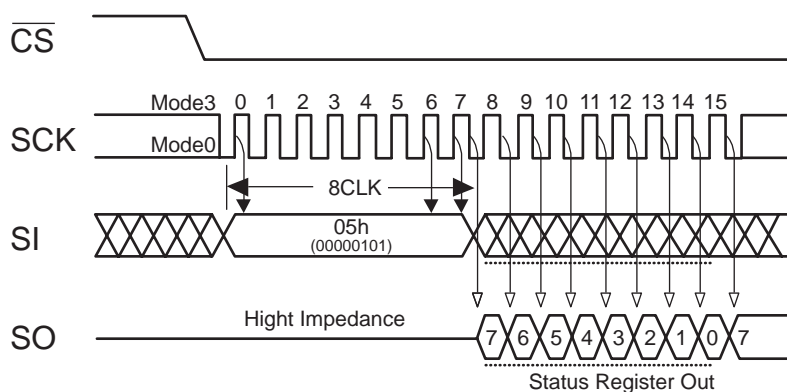
Bit	Name	Logic	Function	Power-on time Information	
Bit0	RDY	0	Ready	0	
		1	Busy (in write operation)		
Bit1	WEN	0	Write disabled	0	
		1	Write enabled		
Bit2	BP0	0	Block protect information See status register description on BP0 and BP1	Nonvolatile information	
		1			
Bit3	BP1	0			Nonvolatile information
		1			
Bit4	x	0	Reserved bit	0	
Bit5	x	0	Reserved bit	0	
Bit6	x	0	Reserved bit	0	
Bit7	SRWP	0	Status register write enabled	Nonvolatile information	
		1	Status register write disabled		

2-1. Status Register Read (RDSR)

The contents of the status registers can be read using the status register read command. This command can be executed even during write operation.

“Figure 5 Status Register READ” shows the timing waveforms of status register read. Consisting only of the first bus cycle, the status register command outputs the contents of the status registers synchronized to the falling edge of the clock (SCK) with which the eighth bit of (05h) has been input. In terms of the output sequence, SRWP (bit7) is the first to be output, and each time one clock is input, all the other bits up to RDY (bit0) are output in sequence, synchronized to the falling clock edge. If the clock input is continued after RDY (bit0) has been output, the data is output by returning to the bit (SRWP) that was first output, after which the output is repeated as long as the clock input is continued. The data can be read by the status register read command at any time.

Figure 5 Status Register Read

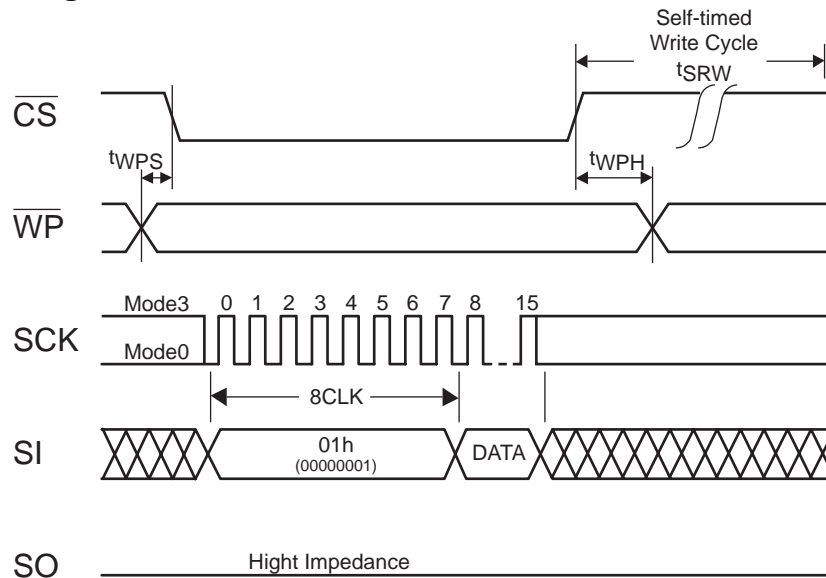


2-2. Status Register Write (WRSR)

The information in status registers BP0, BP1, and SRWP can be rewritten using the status register write command. \overline{RDY} , WEN, bit4, bit5, and bit6 are read-only bits and cannot be rewritten. The information in bits BP0, BP1, and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down.

“Figure 6 Status Register Write” shows the timing waveforms of status register write, and Figure 11 shows a status register write flowchart. Consisting of the first and second bus cycles, the status register write command initiates the internal write operation at the rising \overline{CS} edge after the data has been input following (01h). By the operation of this command, the information in bits BP0, BP1, and SRWP can be rewritten. Since bits \overline{RDY} (bit0), WEN (bit1), bit4, bit5, and bit6 of the status register cannot be written, no problem will arise if an attempt is made to set them to any value when rewriting the status register. Status register write ends can be detected by \overline{RDY} of status register read. Information in the status register can be rewritten 1,000 times (min.). To initiate status register write, the logic level of the \overline{WP} pin must be set high and the status register WEN must be set to “1”.

Figure 6 Status Register Write



2-3. Contents of Each Status Register

\overline{RDY} (bit0) Ready/Busy detection

The \overline{RDY} register is for detecting the write end. When it is “1”, the device is in a busy state, and when it is “0”, it means that the write operation is completed.

WEN (bit1) Write enable

The WEN register is for detecting whether the device can perform write operations. If it is set to “0”, the device will not perform the write operation even if the write command is input. If it is set to “1”, the device can perform write operation in any area that is not block-protected.

WEN can be controlled using the write enable and write disable commands. By inputting the write enable command (06h), WEN can be set to “1”, and by inputting the write disable command (04h), it can be set to “0”. In the following states, WEN is automatically set to “0” in order to protect against unintentional writing.

- At power-on
- Upon completion of write
- Upon completion of status register write

* If a write operation has not been performed inside the device because, for instance, the command input for any of the write operations has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

BP0, BP1 (bits 2, 3)

Block Protect Settings

Block protect BP0 and BP1 are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to “Table 3 Protect Level Setting Conditions.”

Table 3 Protect Level Setting Conditions

Protection Block (Level)	Status Register Bits		Protected Area
	BP1	BP0	
0 (Whole area unprotected)	0	0	None
1 (Upper 1/4 area protected)	0	1	1800h to 1FFFh
2 (Upper 1/2 area protected)	1	0	1000h to 1FFFh
3 (Whole area protected)	1	1	0000h to 1FFFh

SRWP (bit7)

Status Register Write Protect Settings

Status register write protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is “1” and the logic level of the \overline{WP} pin is low, the status register write command is ignored, and status registers BP0, BP1, BP2, and SRWP are protected. When the logic level of the \overline{WP} pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in “Table 4 SRWP Setting Conditions.”

Table 4 SRWP Setting Conditions

\overline{WP} Pin	SRWP	Mode	Status Register	Protected Area	Unprotected Area
1	0	Software protected (SPM)	Unprotected	Protected	Unprotected
0	0				
1	1	Hardware protected (HPM)	Protected	Protected	Unprotected
0	1				

Bit4, bit5, and bit6 are reserved bits, and have no significance.

3. Write Enable (WREN)

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to “1”, and the state is enabled by inputting the write enable command. “Figure 7 Write Enable” shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

- Write (WRITE)
- Status register write (WRSR)

4. Write Disable (WRDI)

The write disable command sets status register WEN to “0” to prohibit unintentional writing. “Figure 8 Write Disable” shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h).

The write disable state (WEN “0”) is exited by setting WEN to “1” using the write enable command (06h).

Figure 7 Write Enable

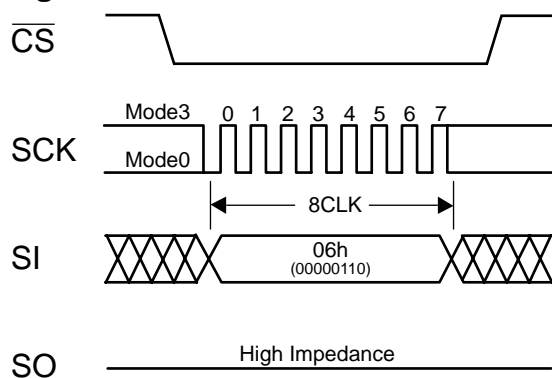
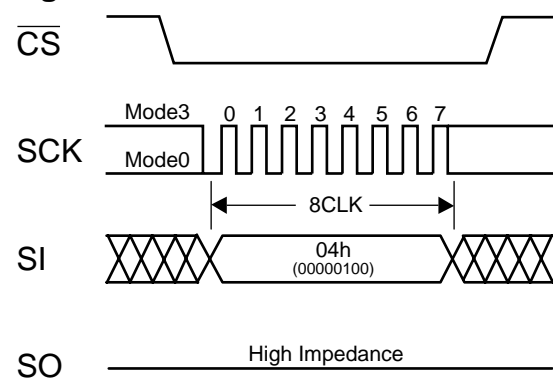


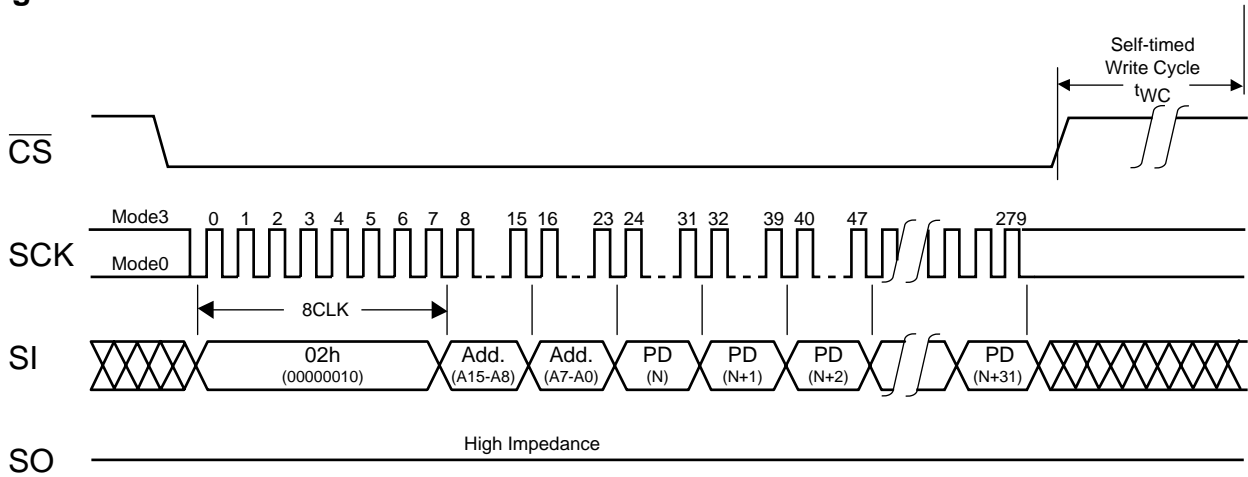
Figure 8 Write Disable



5. Write (WRITE)

The LE25LB643 enables pages with up to 32bytes to be written. Any number of bytes from 1 to 32bytes can be written within the same sector page (page addresses : A15 to A5). “Figure 9 Write” shows the write timing waveforms, and Figure 12 shows a write flowchart. After the falling CS edge, the command (02H) is input followed by the 16-bit addresses (Add). The write data is then loaded until the rising CS edge, and the internal addresses (A4 to A0) are incremented (Add+1) every time the data is loaded in 1-byte increments. The data loading continues until the rising CS edge. If the data loaded has exceeded 32bytes, the 32bytes loaded last are written. The write data must be loaded in 1-byte increments, and the write operation is not performed at the rising CS edge occurring at any other timing. The write time is 10ms (max.) when 32bytes (1page) are written at one time.

Figure 9 Write

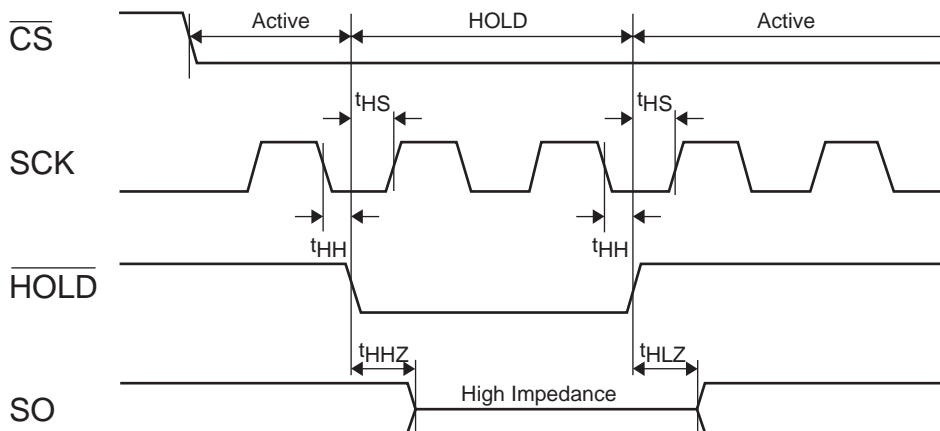


- Addresses A15 - A13 are “don’t care.”

6. Hold Function

Using HOLD pin, the hold function suspends serial communication (it places it in the hold status). “Figure 10 \overline{HOLD} ” shows the timing waveforms. The device is placed in the hold status at the falling \overline{HOLD} edge while the logic level of \overline{SCK} is low, and it exits from the hold status at the rising \overline{HOLD} edge. When the logic level of \overline{SCK} is high, \overline{HOLD} must not rise or fall. The hold function takes effect when the logic of \overline{CS} is low, and the hold status is exited and serial communication is reset at the rising \overline{CS} edge. In the hold status, the \overline{SO} output is in the high-impedance state, and \overline{SI} and \overline{SCK} are “don’t care.”

Figure 10 \overline{HOLD}



7. Hardware Data Protection

In order to protect against unintentional writing at power-on, the LE25LB643 incorporates a power-on reset function.

8. Software Data Protection

This product eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

- When a write command is input and the rising \overline{CS} edge timing is not in a bus cycle (8CLK units of SCK).
- When the write data is not in 1-byte increments.
- When the status register write command is input for 2bus cycles or more.

9. Power-on

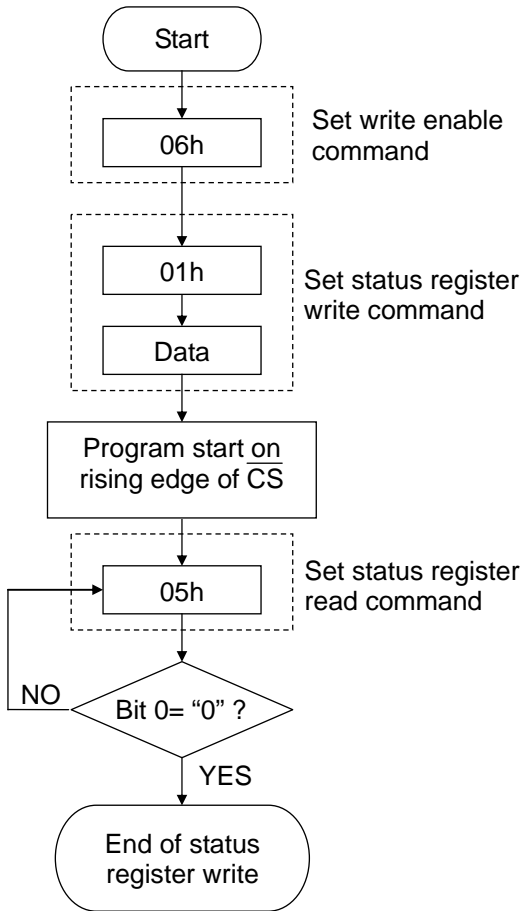
In order to protect against unintentional writing, \overline{CS} must be kept at V_{DD} at power-on. After power-on, the supply voltage has stabilized at 1.8V or higher, wait for 10 μ s (t_{PJ_READ}) before inputting the command to start a read operation. Similarly, wait for 10ms (t_{PJ_WRITE}) after the supply voltage has stabilized at 1.8V or higher before inputting the command to start a write operation.

10. Decoupling Capacitor

A0.1 μ F ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

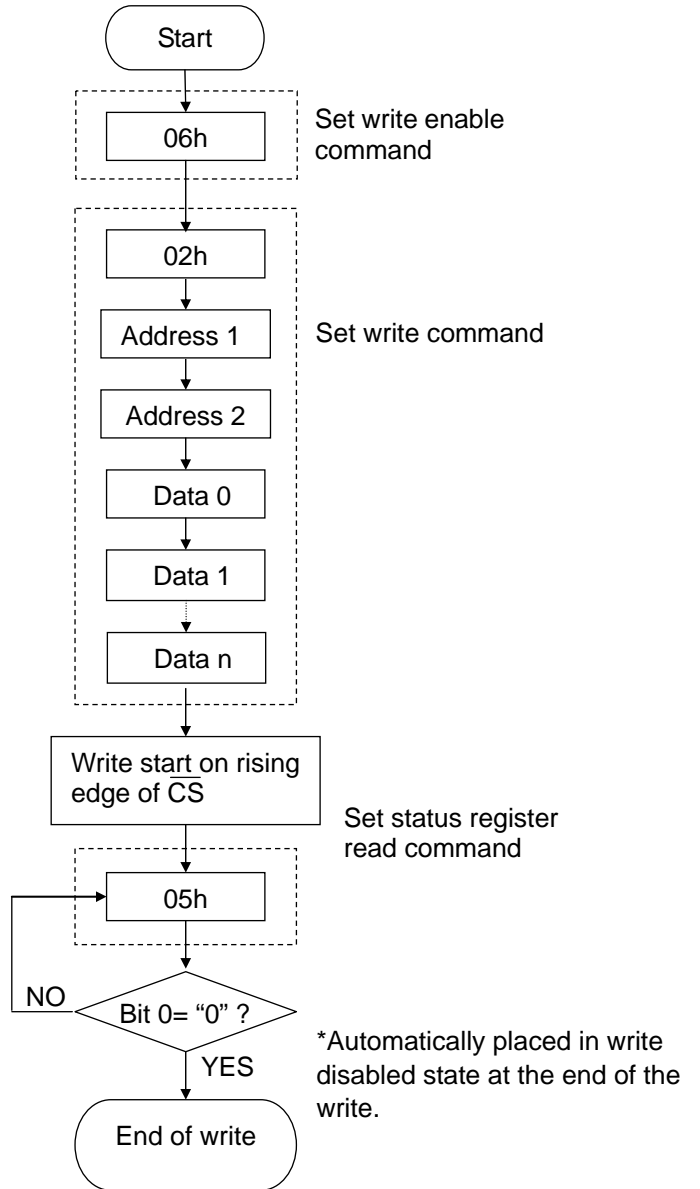
Figure 11 Status Register Write Flowchart Figure 12 Write Flowchart

Status register write



*Automatically placed in write disabled state at the end of the status register write.

Write



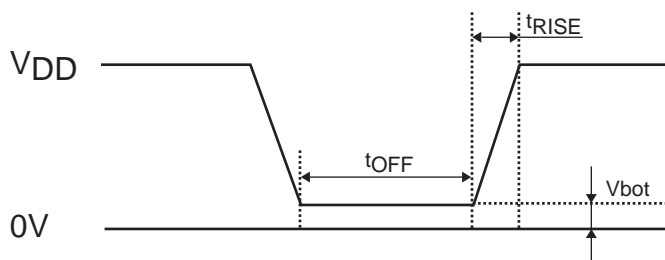
*Automatically placed in write disabled state at the end of the write.

Application Note

1) Precautions at Power-on

In order to protect against unintentional writing, the LE25LB643 incorporates a power-on rest circuit. The following conditions must be met in order to ensure that the power-on reset circuit will operate stably. No guarantees are given for data in the event of an instantaneous power failure occurring during the write operation.

Symbol	Item	$V_{DD} = 1.8 \text{ to } 3.6\text{V}$			Unit
		min	typ	max	
t_{RISE}	Power rise time			100	ms
t_{OFF}	Power off time	10			ms
V_{bot}	Power bottom voltage			0.2	V



Note:

- 1). The \overline{CS} pin must be set high.

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of January, 2011. Specifications and information herein are subject to change without notice.