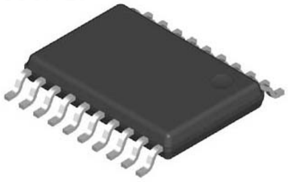
LEOAC08

Datasheet

Rad-hard plastic Quad two-input AND gate

TSSOP-20



Maturity status link
LEOAC08

Features

- AND gate
- 6 V max. operating
- 7 V max. rating
- 8.5 ns propagation delay
- Nickel/Palladium/Gold-lead-finished (NiPdAu), whisker-free
- Gold-wires
- RML <1% and CVCM <0.1% guaranteed outgassing
- 50 krad (Si) Total Ionizing Dose
- SEL-free up to 62.5 MeV.cm²/mg
- Mass: 80 mg
- Compliant with ST-LEO-specification

Applications

- Low earth orbit (LEO) applications

Description

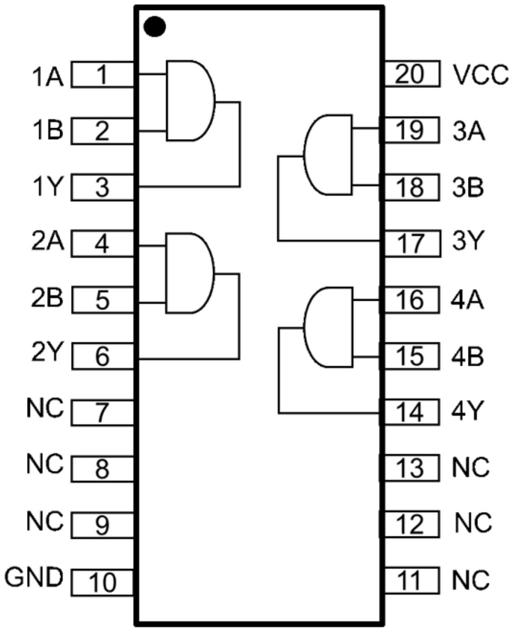
The LEOAC08 is a CMOS low power quad 2-input AND gate qualified for use in aerospace environments. It operates from 2 V to 6 V power supply (7 V absolute maximum rating).

The LEOAC08 can operate over a large temperature range of -40 °C to +125 °C and it is housed in plastic TSSOP-20, Thin-Shrink Small Outline Package, 20 leads, using golden bonding and Nickel/Palladium/Golden-lead-finishing to prevent whiskers.

The LEOAC08 is compliant with ST-LEO-specification, dedicated specification for space-ready rad-hard plastic products. This AEC-Q100-based specification offers a specific trade-off between footprint size savings, cost of ownership and quality assurance together with radiation hardness and large quantity capability.

1 Functional description

Figure 1. **Pin connections (top view)**



NC: not internally connected.

The pin can be externally connected to any potential.

Table 1. **Truth table**

Each gate		
INPUT (A)	INPUT (B)	OUTPUT (Y)
L	L	L
L	H	L
H	L	L
H	H	H

with: L = low level, H = high Level.
For all inputs, V_{IN} = V_{IH} minimum or V_{IL} maximum, verify output V_{OUT}.

2 Maximum ratings and operating conditions

Table 2. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{CC} (1)	Maximum power supply between V_{CC} and GND	-0.5 to 7	V
V_{IN}	DC input voltage range	-0.5 to V_{CC} +0.5 (and 7 V max.)	V
V_{OUT}	DC output voltage range	-0.5 to V_{CC} + 0.5 (and 7 V max.)	V
I_K	I/O clamp diode current	+/-20	mA
T_{stg}	Maximum temperature storage	-65 to +150	°C
T_j (2)	Maximum junction temperature	+150	°C
R_{th} (3)	Junction to ambient thermal resistance (Θ_{ja})	80	°C/W
	Junction to case thermal resistance (Θ_{jc})	17	°C/W
ESD	HBM (human body model)	2k	V
	CDM (charged device model)	1k	V

1. *All voltages, except differential I/O bus voltage, are with respect to the network ground terminal .*
2. *Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions as per the method 5004 of MIL-STD-883.*
3. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.*

Table 3. **Operating conditions**

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Analog supply voltage	2	6	V
V_{IN}	Input voltage range	0	V_{CC}	V
V_{OUT}	Output voltage range	0	V_{CC}	V
Ta	Ambient temperature range	-40	+125	°C

Note: All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

3 Electrical characteristics

V_{CC} = 3 V to 5.5 V, typical values are at ambient Ta = +25 °C, min. and max. values are at Ta = -40 °C and +125 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	VCC (V)	Min.	Typ.	Max.	Unit
V_{OH} (1)	High level output voltage	For all inputs affecting output under test, V_{IN} = V_{IH} minimum or V_{IL} maximum. For all other inputs, V_{IN} = V_{CC} or GND, I_{OH} = -50 µA	3	2.9			V
			4.5	4.4			
			5.5	5.4			
		For all inputs affecting output under test, V_{IN} = V_{IH} minimum or V_{IL} maximum. For all other inputs, V_{IN} = V_{CC} or GND, I_{OH} = -12 mA	3	2.4			
		For all inputs affecting output under test, V_{IN} = V_{IH} minimum or V_{IL} maximum. For all other inputs, V_{IN} = V_{CC} or GND, I_{OH} = -24 mA	4.5	3.7			
			5.5	4.7			
		For all inputs affecting output under test, V_{IN} = V_{IH} minimum or V_{IL} maximum. For all other inputs, V_{IN} = V_{CC} or GND I_{OH} = -50 mA	5.5	3.85			
V_{OL} (1)	Low level output voltage	For all inputs affecting output under test, V_{IN} = V_{IH} minimum or V_{IL} maximum. For all other inputs, V_{IN} = V_{CC} or GND, I_{OL} = +50 µA	3		0.1		V
			4.5		0.1		
			5.5		0.1		
		For all inputs affecting output under test, V_{IN} = V_{IH} minimum or V_{IL} maximum. For all other inputs, V_{IN} = V_{CC} or GND, I_{OL} = +12 mA	3		0.5		
		For all inputs affecting output under test, V_{IN} = V_{IH} minimum or V_{IL} maximum. For all other inputs, V_{IN} = V_{CC} or GND, I_{OL} = +24 mA	4.5		0.5		
			5.5		0.5		
		For all inputs affecting output under test, V_{IN} = V_{IH} minimum or V_{IL} maximum. For all other inputs, V_{IN} = V_{CC} or GND, I_{OL} = +50 mA	5.5		1.65		
I_{OH}	High level output current		3	-12			mA
			4.5	-24			
			5.5	-24			
I_{OL}	Low level output current		3			12	
			4.5			24	
			5.5			24	
V_{IH} (2)	High level input voltage		3	2.1			mA
			4.5	3.15			
			5.5	3.85			
V_{IL} (2)	Low level input voltage		3			0.9	V
			4.5			1.35	
			5.5			1.65	
V_{IC+}	Positive input clamp voltage	For input under test, I_{IN} = -1.0 mA	0	0.4		1.5	V

Symbol	Parameter	Test condition	VCC (V)	Min.	Typ.	Max.	Unit
V_{IC-}	Negative input clamp voltage	For input under test, I_{IN} = -1.0 mA	Open	0.4		1.5	V
I_{IH}	Input current high	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND	5.5			1	µA
I_{IL}	Input current low	For input under test, V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND	5			-1	µA
I_{CCH}	Quiescent supply current, output high	For all inputs, $V_{IN} = V_{CC}$ or GND I_{OUT} = 0 A	5.5			40	µA
I_{CCL}	Quiescent supply current, output low	For all inputs, $V_{IN} = V_{CC}$ or GND I_{OUT} = 0 A	5.5			40	µA
C_{IN} (3)	Input capacitance	Ta = +25 °C	5			10	pF
C_{PD} (4) (3)	Power dissipation capacitance	Ta = +25 °C, F = 1 MHz	5			88	pF
T_r, T_f	Output rise time and fall time	C_L = 2 pF, R_L = 500 ohm (see Figure 2)	3		3.3		ns
			4.5		2.7		
		C_L = 50 pF, R_L = 500 ohm (see Figure 2)	3		4.6		
			4.5		3.3		
T_{PHL} (5)	Propagation delay time An to Yn, high to low	C_L = 50 pF, R_L = 500 ohm (see Figure 2)	3	1		11.5	ns
			4.5	1		8.5	
T_{PLH}(5)	Propagation delay time An to Yn, low to high	C_L = 50 pF, R_L = 500 ohm (see Figure 2)	3	1		12.5	
			4.5	1		9	

1. *The V_{OH} and V_{OL} tests shall be tested at V_{CC} = 3.0 V and 4.5 V. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for other values of V_{CC}. Limits shown apply to operation at V_{CC} = 3.3 V, ±0.3 V and V_{CC} = 5.0 V ±0.5 V. Tests with input current at +50 mA and –50 mA are performed on only one input at a time with duration not to exceed 10 ms. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = V_{IH}$ minimum and V_{IL} maximum.*
2. *The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.*
3. *C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard JESD20 and table IA herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.*
4. *Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and dynamic current consumption (IS). Where: $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC}) f + (I_{CC} \times V_{CC})$ and $IS = (C_{PD} + C_L) V_{CC} \times f + I_{CC}$, and f is the frequency of the input signal and C_L is the external output load capacitance.*
5. *For propagation delay tests, all paths are tested. The AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. The AC limits at V_{CC} = 3.6 V are equal to the limits at V_{CC} = 3.0 V and guaranteed by testing at V_{CC} = 3.0 V. Minimum AC limits for V_{CC} = 5.5 V and V_{CC} = 3.6 V are 1.0 ns and guaranteed by guard banding the V_{CC} = 4.5 V and V_{CC} = 3.0 V minimum limits, respectively, to 1.5 ns. For propagation delay tests, all paths must be tested.*

4 Waveform and test circuit

Figure 2. Waveform

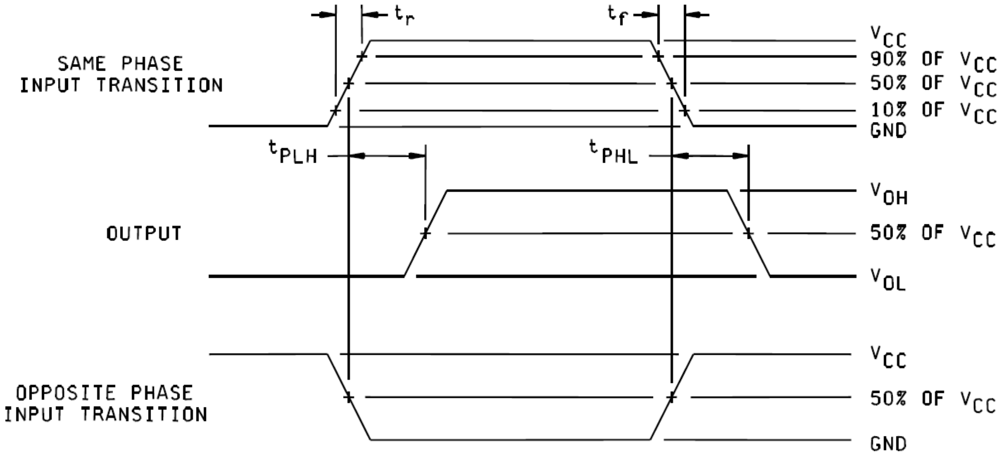
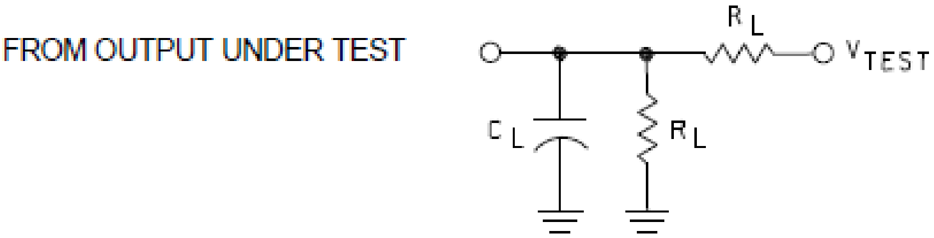


Figure 3. Test circuit



Note:

- *V_{TEST} = open for t_{PLH} and t_{PHL}.*
- *C_L = 50 pF or equivalent (includes probe and jig capacitance).*
- *R_L = 500-ohm or equivalent.*
- *Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; P_{RR} < 1 MHz; ZO = 50-ohm; tr < 3.0 ns; tf < 3.0 ns; tr and tf shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC}, respectively; duty cycle = 50 percent.*
- *Timing parameters shall be tested at a minimum input frequency of 1 MHz.*
- *The outputs are measured one at a time with one transition per measurement.*

5 Radiations

Total ionizing dose (TID):

For the qualification, the product is characterized in TID as per MIL-STD-883 TM 1019 up to 50 krad (Si) on 5 biased parts at high dose rate, such a rate being the worst condition for a pure CMOS technology.

All parameters provided in Table 1 apply to both pre- and post-irradiation.

Each new production lot is tested at high dose rate as per MIL-STD-883 TM 1019 on 5 parts.

Heavy-ions:

Single Event Latchup (SEL) is characterized at 125 °C at a LET of 62.5 MeV.cm2/mg. The test shows the product is immune to heavy ions at this LET. Heavy-ion trials are performed on qualification lots only.

The results in radiation are summarized in Table 5 as follows.

Table 5. Radiations

Type	Conditions	Results
TID (1)	• High-dose rate (40 krad (Si) / h) • Temperature: 25 °C • Performed on 5 biased parts	WithinTable 1 up to 50 krad(Si)
SEL (2)	• LET: 62.5 MeV.cm2/mg (Xenon ions) • Temperature: 125 °C • Fluence: 1 x 10^7 ions/cm^2 (10 Million of particles per cm²) • Normal incidence	Immune to SEL up to 62.5 MeV.cm^2/mg (extracted from the LEOAC00, by similarity of architecture)

1. *A total ionizing dose (TID) of 50 krad(Si) is equivalent to 500 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latch-up*

6 Outgassing

Specification (tested per ASTM E 595)	Value	Unit
Recovered mass loss (RML) (1)	0.06	%
Collected volatile condensable material (CVCM) (2)	0.00	%

1. *RML < 1%*
2. *CVCM < 0.1%*

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 TSSOP-20 package information

Figure 4. TSSOP-20 package outline

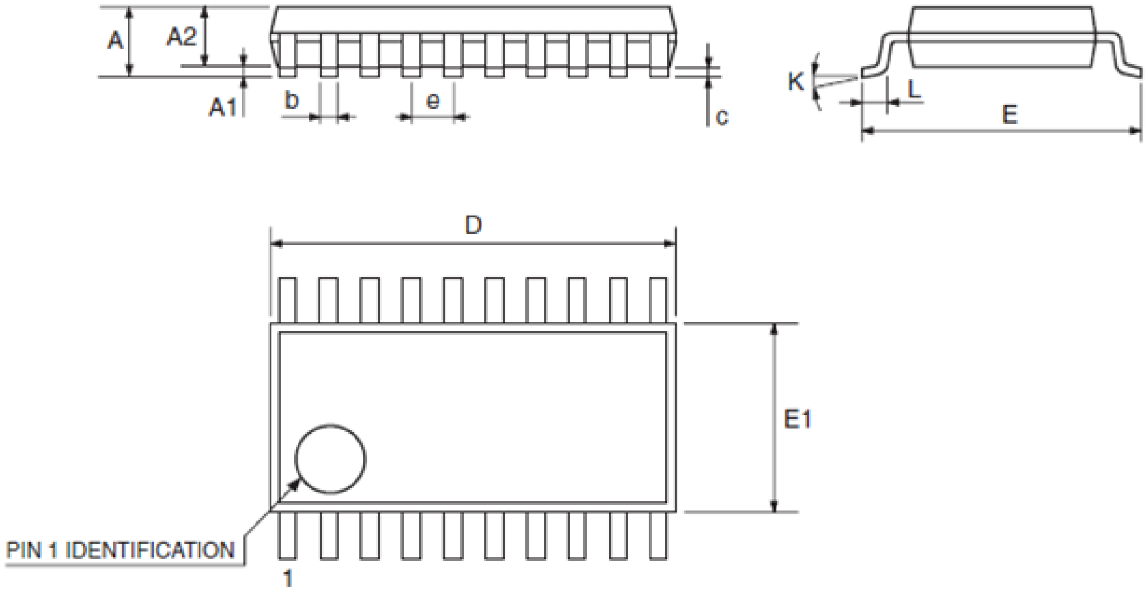


Table 6. TSSOP-20 package mechanical data

Symbol	Milimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		
c	0.09		0.20	0.004		
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Note: *TSSOP: Thin-Shrink Small Outline Package, using golden bonding and Nickel/Palladium/Golden-lead-finishing.*

7.2 TSSOP-20 packing information

Figure 5. TSSOP-20 Carrier tape (dimensions in mm) outline

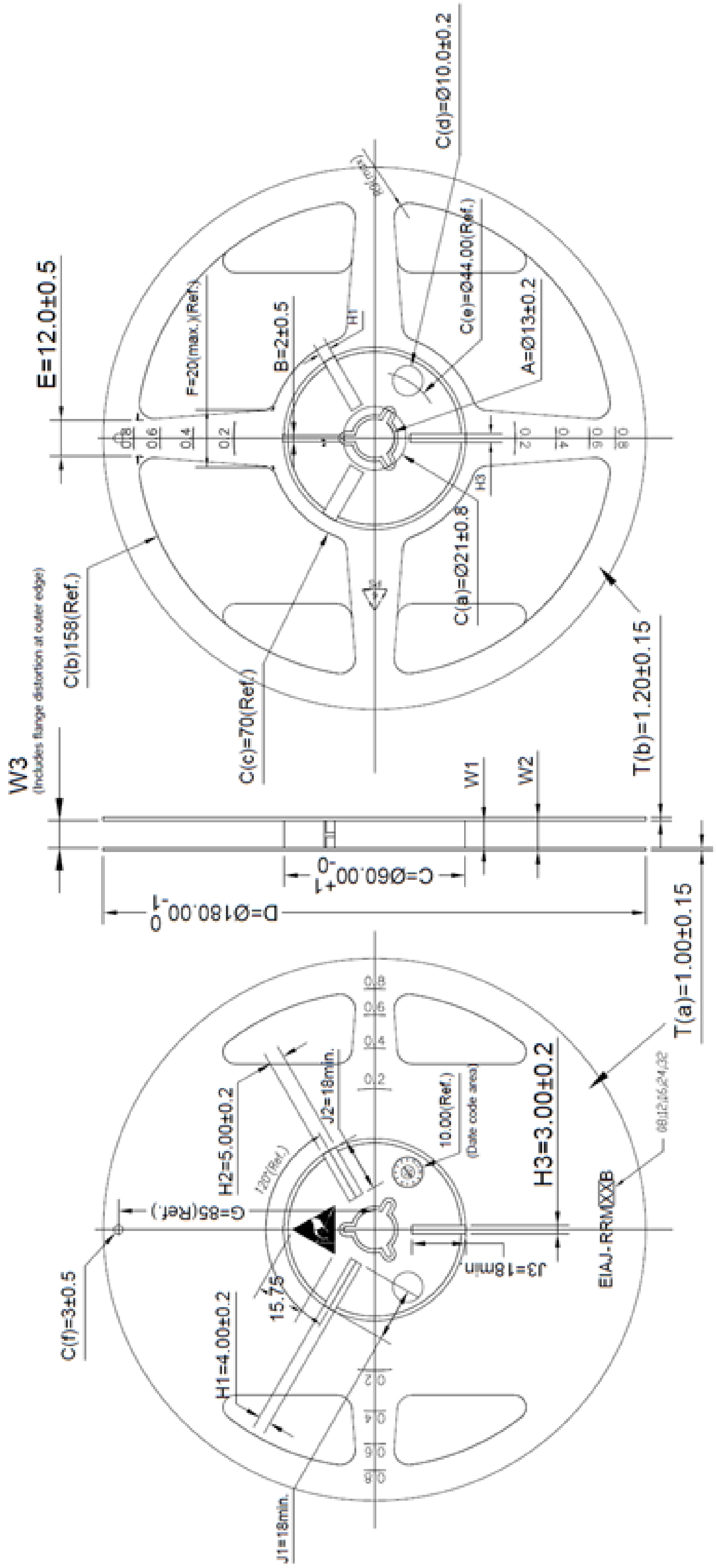
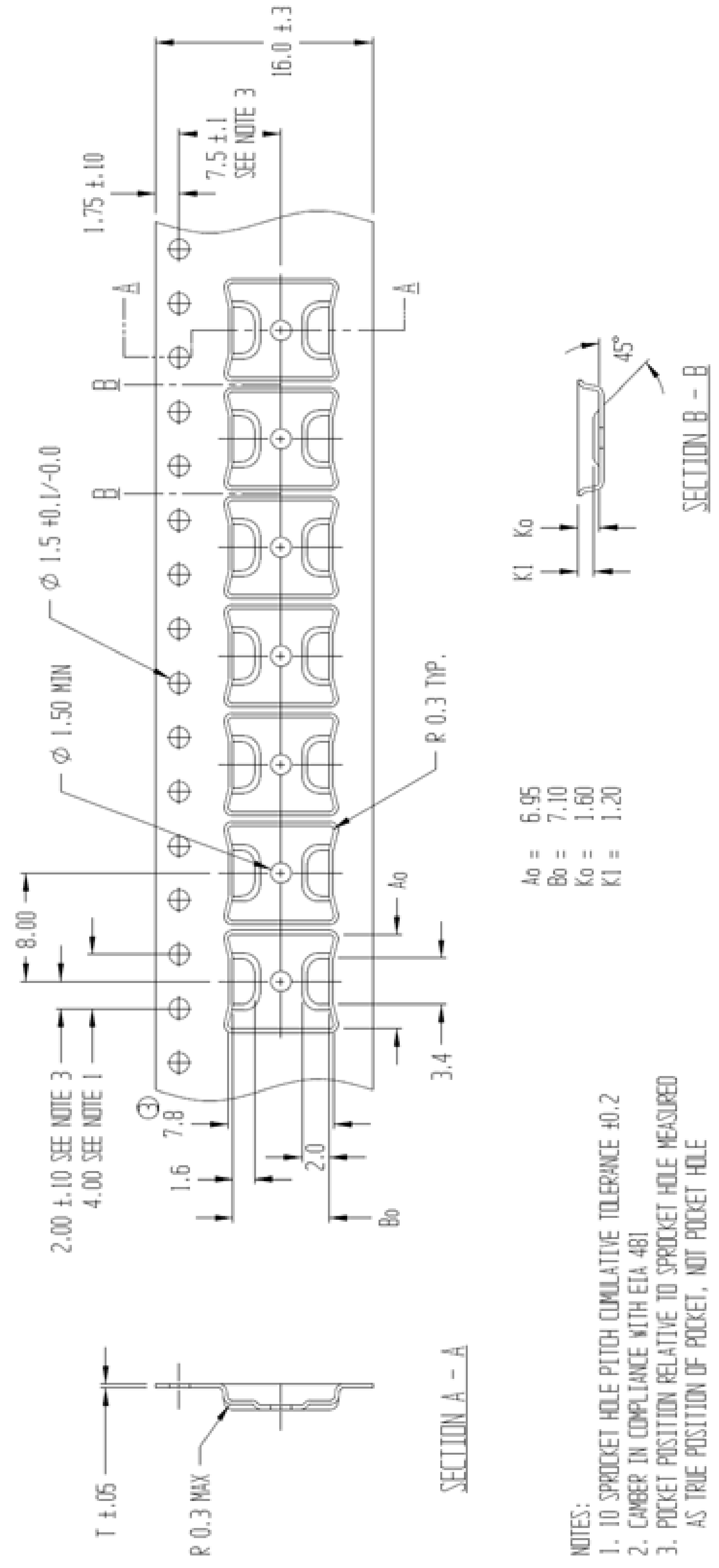


Figure 6. **TSSOP-20 tape (dimensions in mm) outline**



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

8 Ordering information

Table 7. **Ordering information**

Order code	Quality level	Package	Lead-finish	Marking	Packing
LEOAC08PT-D	Development sample	TSSOP-20	NiPdAu	DLEOAC08	Tape and reel
LEOAC08PT	Flight model	TSSOP-20	NiPdAu	LEOAC08	Tape and reel

Table 8. **Order code**

LEO	AC08	P	T
LEO qualification	Name	TSSOP-20 package	Tape and reel

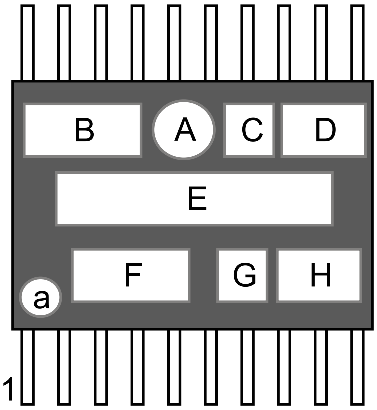


Figure 7. **TSSOP-20 marking**

a: pin-1 reference
A : Second Level of interconnexion (type of lead-finishing)
B: ST logo
C: Assy plant
D: Lot code
E: Marking area
F: Country of origin
G: Assy year
H: Assy week

Revision history

Table 9. **Document revision history**

Date	Version	Changes
10-Jan-2022	1	First release.
01-Feb-2022	2	Removed footnote in Table 7. Ordering information.

Contents

1 Functional description 2
2 Maximum ratings and operating conditions 3
3 Electrical characteristics 4
4 Waveform and test circuit 6
5 Radiations 7
6 Outgassing 8
7 Package information 9
  7.1 TSSOP-20 package information 9
  7.2 TSSOP-20 packing information 10
8 Ordering information 12
Revision history 13

List of tables

Table 1. Truth table . . . 2
Table 2. Absolute maximum ratings . . . 3
Table 3. Operating conditions . . . 3
Table 4. Electrical characteristics . . . 4
Table 5. Radiations . . . 7
Table 6. TSSOP-20 package mechanical data . . . 9
Table 7. Ordering information. . . . 12
Table 8. Order code . . . 12
Table 9. Document revision history . . . 13

List of figures

Figure 1. Pin connections (top view) . . . 2
Figure 2. Waveform . . . 6
Figure 3. Test circuit . . . 6
Figure 4. TSSOP-20 package outline . . . 9
Figure 5. TSSOP-20 Carrier tape (dimensions in mm) outline . . . 10
Figure 6. TSSOP-20 tape (dimensions in mm) outline . . . 11
Figure 7. TSSOP-20 marking . . . 12

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved