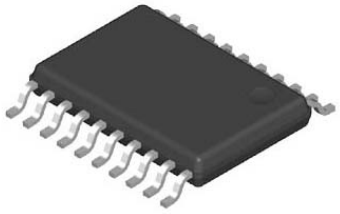
LEOLVDSRD

Datasheet

Rad-hard plastic LVDS driver-receiver

TSSOP-20



Product status link
LEOLVDSRD

Features

- LVDS single driver and single receiver
- 400 Mbps (200 MHz)
- 3 V to 3.6 V operating power supply
- 4.8 V absolute maximum ratings
- Individual enable/disable function with high impedance
- Cold spare on all pins
- Fail-safe function
- RML < 1% and CVCM <0.1% guaranteed outgassing
- Nickel/palladium/gold-lead-finished (NiPdAu), whisker-free
- Gold wires
- 50 krad (Si) total ionizing dose
- SEL-free up to 62.5 MeV.cm²/mg
- Mass: 80 mg
- Compliant with ST-LEO-specification

Applications

- Low earth orbit (LEO) satellites, high speed interface systems

Description

The LEOLVDSRD is a 3 V to 3.6 V power supply (4.8 V absolute maximum ratings) low voltage differential signaling (LVDS) driver and receiver qualified for use in aerospace environments. It operates over a controlled impedance of 100 ohm transmission media that may be printed circuit board traces, back planes, or cables.

The circuit features an internal fail-safe function to ensure a known state in case of an input short-circuit or floating input. All pins have cold spare buffers to ensure they are in high impedance when VCC is tied to GND.

The LEOLVDSRD can operate over a large temperature range of -40 °C to +125 °C and it is housed in plastic TSSOP-20, thin-shrink small outline package, 20 leads, using gold-wires and nickel/palladium/golden-lead-finishing to prevent from whiskers.

The LEOLVDSRD is compliant with ST-LEO-specification, dedicated specification for space-ready rad-hard plastic products. This AEC-Q100-based specification offers a specific trade-off among footprint size savings, cost of ownership and quality assurance together with radiation hardness and a large quantity capability.

1 Functional description

Figure 1. **Pin connections (top view)**

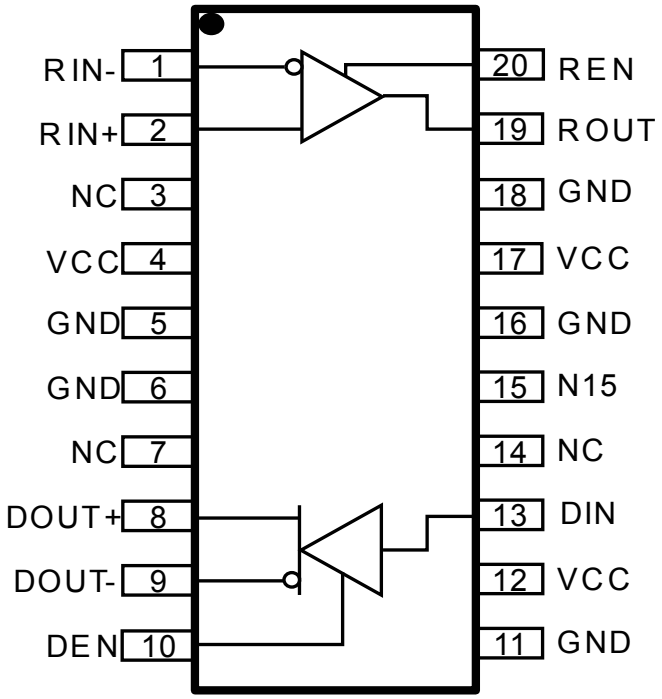


Table 1. **Pin descriptions**

Pin #	Name	Description on the pin
1, 2	RIN+, RIN-	LVDS input of the receiver.
8, 9	DOU+, DOUT-	LVDS output of the driver.
4, 12, 17	VCC	Power supply pins.
5, 6, 11, 16, 18	GND	Ground pins, must be all connected together to the ground of the PCB. Any ground pin cannot be left floating.
3, 7, 14	NC	Not internally connected. These pins can be externally connected to any potential.
10, 20	DEN, REN	LVCMOS input, enable/disable input of the driver and the receiver.
13, 19	DIN, ROUT	LVCMOS input of the driver, LVCMOS output of the receiver.
15	N15	Must be connected to ground.

Figure 2. **Equivalent schematic of the pins**

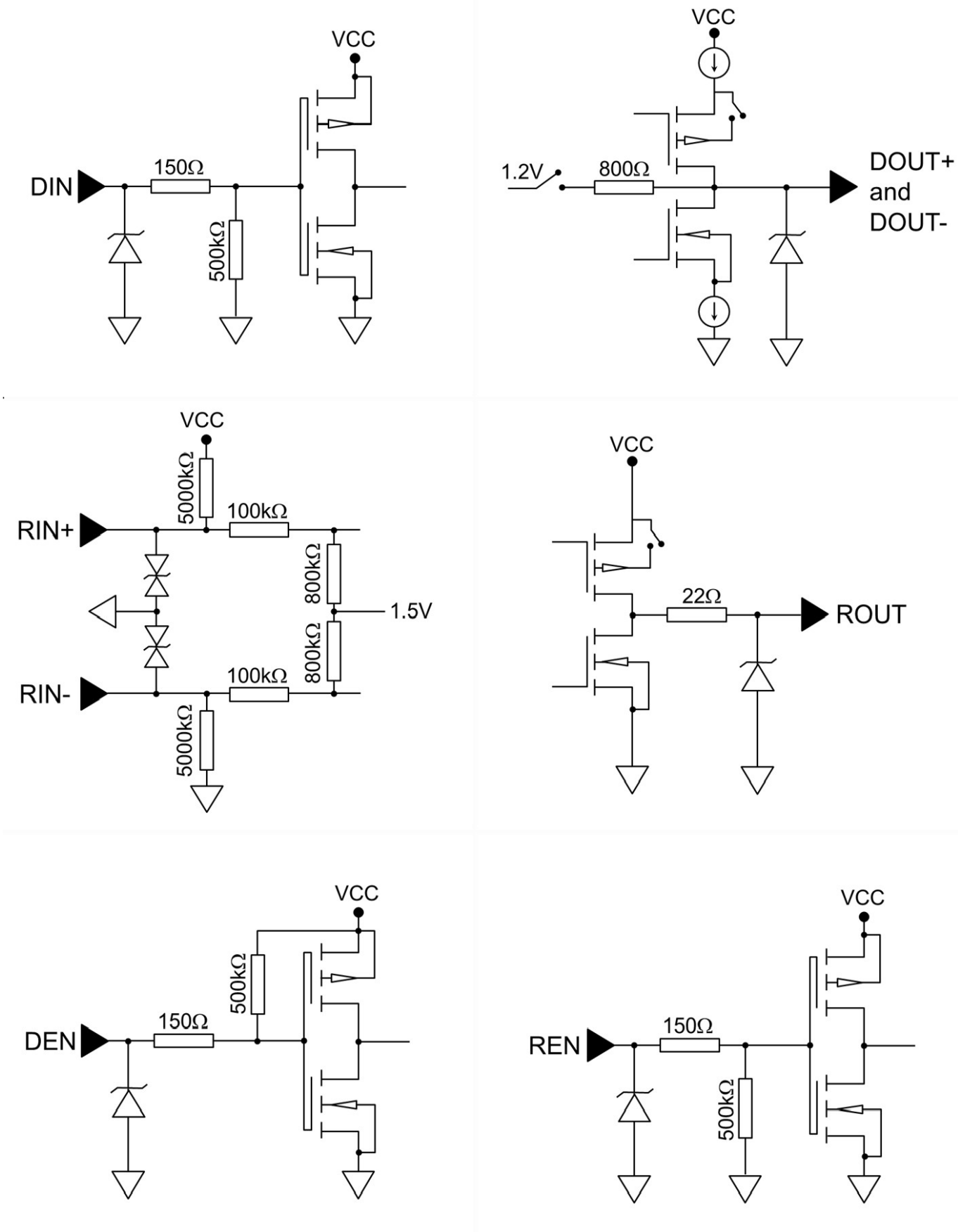


Table 2. Driver truth table (DIN)

Enables	Input	Output	
DEN	DIN	DOUT+	DOUT-
L	X	Z	Z
H or floating (internal pull-up)	L	L	H
	H	H	L
	Open	L	H

Table 3. Receiver truth table

Enables	Input	Output
REN	RIN+ - RIN-	ROUT
L	X	Z
H or floating (internal pull-up)	VID > 0.1 V	H
	VID < -0.1 V	L
	-0.1 V < VID < +0.1 V	?
	Full fail-safe open/short or terminated	H

Note: Vid = (VIN+) - (VIN-), L = low level, H = high Level, X = do not care, Z = high impedance (off).

2 Maximum ratings and operating conditions

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC(1)	Maximum analog power supply between VCC and GND	-0.3 to 4.8	V
Vi	LVCMOS inputs (operating or cold-spare)	-0.3 to 4.8	V
VOUT	LVDS outputs and LVCMOS outputs (operating or cold-spare)	-0.3 to 4.8	V
VCM	LVDS common mode (operating or cold-spare)	-5 to +6	V
T_{stg}	Maximum temperature storage	-65 to +150	°C
T_j(2)	Maximum junction temperature	+150	°C
R_{th}(3)	Junction-to-ambient thermal resistance (Θja)	80	°C/W
	Junction-to-case thermal resistance (Θjc)	17	°C/W
ESD	HBM (human body model), LVDS inputs and outputs vs pin 5, 6, 11, 16	8 k	V
	HBM on all pins except LVDS inputs and outputs	2 k	
	CDM (charged device model)	1 k	

1. *All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.*
2. *Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions as per the method 5004 of MIL-STD-883.*
3. *Short-circuits can cause excessive heating.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 5. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply voltage	3	3.6	V
VCM	Static common mode on the receiver	-4	+4	V
VIN	Driver DC input voltage (LVCMOS inputs)	0	3.6	V
T_a	Ambient temperature range	-40	+125	°C

Note: All unused inputs must be held at VCC or GND to ensure proper device operation.

3 Electrical characteristics

VCC = 3 V to 3.6 V, capa-load (CL) = 10 pF, typical values are at ambient Ta = +25 °C, min. and max. values are at T_a = - 40 °C and + 125 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Whole circuit						
ICC	Total enabled supply current, drivers and receivers enabled, not switching	Driver: VIN = 0 V or VCC, load = 100 ohm, receiver: VID = 400 mV		8	10	mA
ICCZ	Total disabled supply current, loaded or not loaded, drivers and receivers disabled	REN and DEN = GND Driver: VIN = 0 V or VCC receiver: VID = 400 mV			4	mA
VIH	Input voltage high	REN, DEN, and LVCMOS inputs	2		VCC	V
VIL	Input voltage low		GND		0.8	V
IIH	High level input current	REN, DEN, and LVCMOS inputs, VCC = 3.6 V, VIN = VCC	-10		10	µA
IIL	Low level input current	REN, DEN, and LVCMOS inputs, VCC = 3.6 V, VIN = 0	-10		10	
IOFF	LVDS output power-off leakage current	VCC = 0 V, VOUT = 3.6 V	-50		+50	
	LVDS input power-off leakage current	VCC = 0 V, VIN = -4 V to +4 V	-60		60	
	LVCMOS I/Os power off leakage current	VCC = 0 V VIN, REN, and DEN = 3.6 V VOUT = 3.6 V	-10		10	
Driver						
VOH	Output voltage high	RL= 100 ohm			1.65	V
VOL	Output voltage low		0.925			V
VOD	Differential output voltage		250		400	mV
DVOD	Change of magnitude of VOD1 for complementary output states				10	mV
VOS	Offset voltage		1.125		1.375	V
DVOS	Change of magnitude of VOS for complementary output states				15	mV
IOS	Output short-circuit current	VIN= 0 V and VOUT- = 0 V or VIN = VCC and VOUT+ = 0 V	-9			mA
IOZ	High impedance output current	Disabled, VOUT = 3.6 V or GND	-10		10	uA
CIN	Input capacitance			3		pF
TPHLD	Propagation delay time, high to low output	Load: refer to Figure 4. Test circuit, timing and voltage definitions for differential output signal for the driver	0.5		1.5	ns

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
TPLHD	Propagation delay time, low to high output	Load: refer to Figure 4. Test circuit, timing and voltage definitions for differential output signal for the driver	0.5		1.5	
T_r	Differential output signal rise time			0.8		
T_f	Differential output signal fall time			0.8		
TSK	Chip-to-chip skew(1) (2)				0.7	ns
TSKD	Differential skew (TPHLD-TPLHD)(3)				0.3	
TPHZ	Propagation delay time, high level to high impedance output	Load: refer to Figure 5. Enable and disable waveforms for the driver			2.8	
TPLZ	Propagation delay time, low level to high impedance output				2.8	
TPZH	Propagation delay time, high impedance to high level output				2.5	
TPZL	Propagation delay time, high impedance to low level output				2.5	
Receiver						
VTL	Differential input low threshold	VCM = 1.2 V			-100	mV
		-4 V < VCM < +4 V			-130	
VTH	Differential input high threshold	VCM = 1.2 V	+100			
		-4 V < VCM < +4 V	+130			
VCL	LVCMOS input clamp voltage	ICL = 18 mA			1.5	V
VCMREJ	Common mode rejection(2)	F = 10 MHz			300	mVpp
IID	Differential input current	VID = 400 mVp-p	-10		+10	µA
IICM	Common mode input current	VCM = - 4 V to + 4 V	-70		+70	µA
VOH	Output voltage high	IOH = -0.4 mA, VCC = 3 V	2.7			V
VOL	Output voltage low	IOL = 2 mA, VCC = 3 V			0.25	V
IOS	Output short-circuit current	VOUT = 0 V	-90		-30	mA
IOZ	Output tri-state current	Disabled, VOUT = 0 V or VCC	-10		+10	µA
CIN	Input capacitance	IN+ or IN- to GND		3		pF
ROUT	Output resistance			45		ohm
TPHLD	Propagation delay time, high-to-low output	VID = 200 mVp-p, input pulse from 1.1 V to 1.3 V, VCM = 1.2 V Load: refer to Figure 6. Timing test circuit and waveforms for the receiver	1		2.5	ns
TPLHD	Propagation delay time, low-to-high output		1		2.5	
T_r	Output signal rise time	Load: refer to Figure 6. Timing test circuit and waveforms for the receiver		0.9		ns
T_f	Output signal fall time			0.9		
TSK	Chip-to-chip skew(1),(2)				0.7	
TSKD	Differential skew (TPHLD-TPLHD) (3)				0.3	
TPHZ	Propagation delay time, high level to high impedance output	Load: refer to Figure 7. Enable and disable waveforms for the receiver			3.8	ns
TPLZ	Propagation delay time, low level to high impedance output				3.8	

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
TPZH	Propagation delay time, high impedance to high level output	Load: refer to Figure 7. Enable and disable waveforms for the receiver			3.8	ns
TPZL	Propagation delay time, high impedance to low level output				3.8	
TD1	Fail-safe to active time			1		µs
TD2	Active to fail-safe time			1		µs

1. *TSK is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.*
2. *Guaranteed by design and characterization*
3. *TSKD is the maximum delay time difference between TPHLD and TPLHD.*

Cold sparing:

The LEOLVDSRD features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (VCC = GND) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and VCC. ESD protection is ensured through a non-conventional dedicated structure.

Fail-safe:

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of an LVDS input short-circuit or floating input, the LVCMOS output remains in stable logic-high state.

4 Wave forms and test circuits

Figure 3. Voltage and current definition for the driver

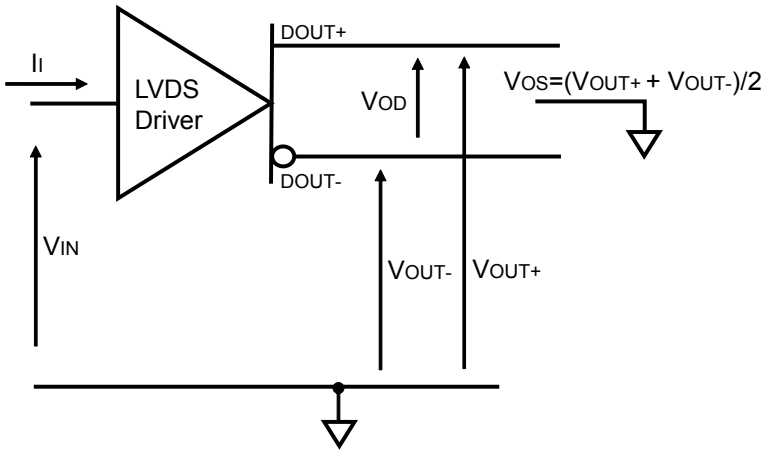
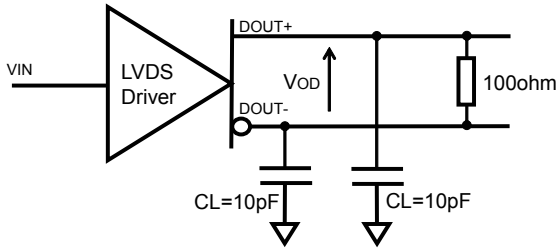
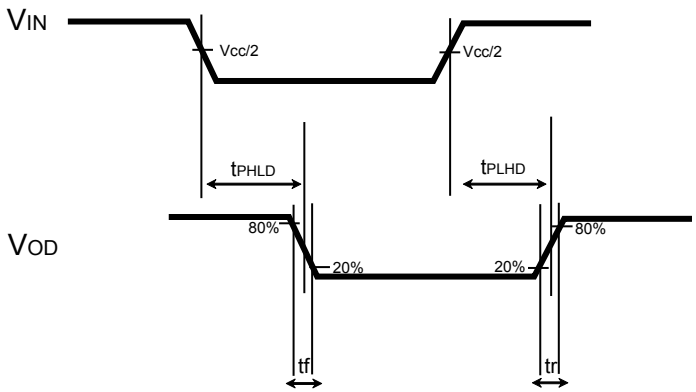


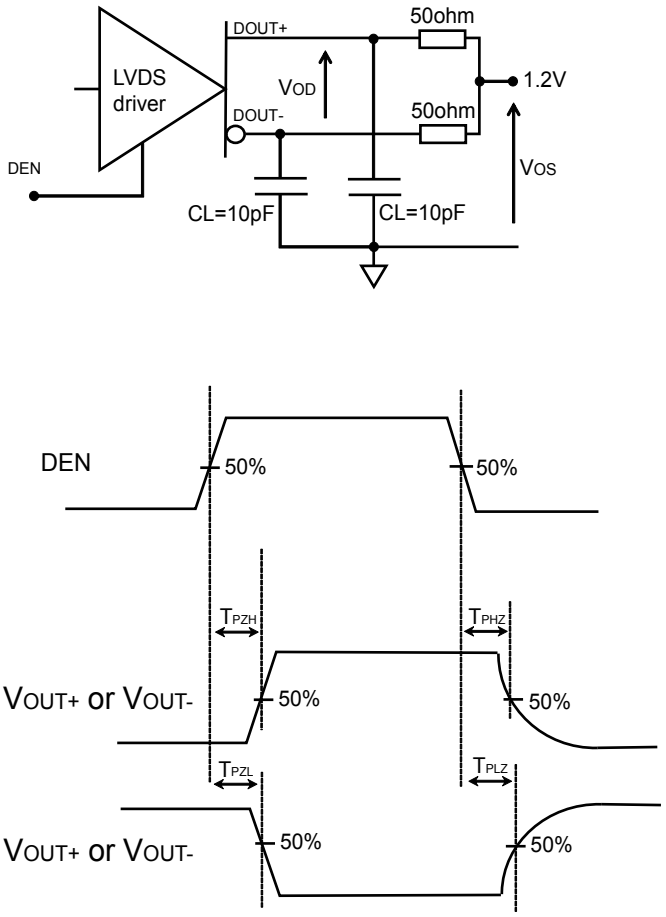
Figure 4. Test circuit, timing and voltage definitions for differential output signal for the driver





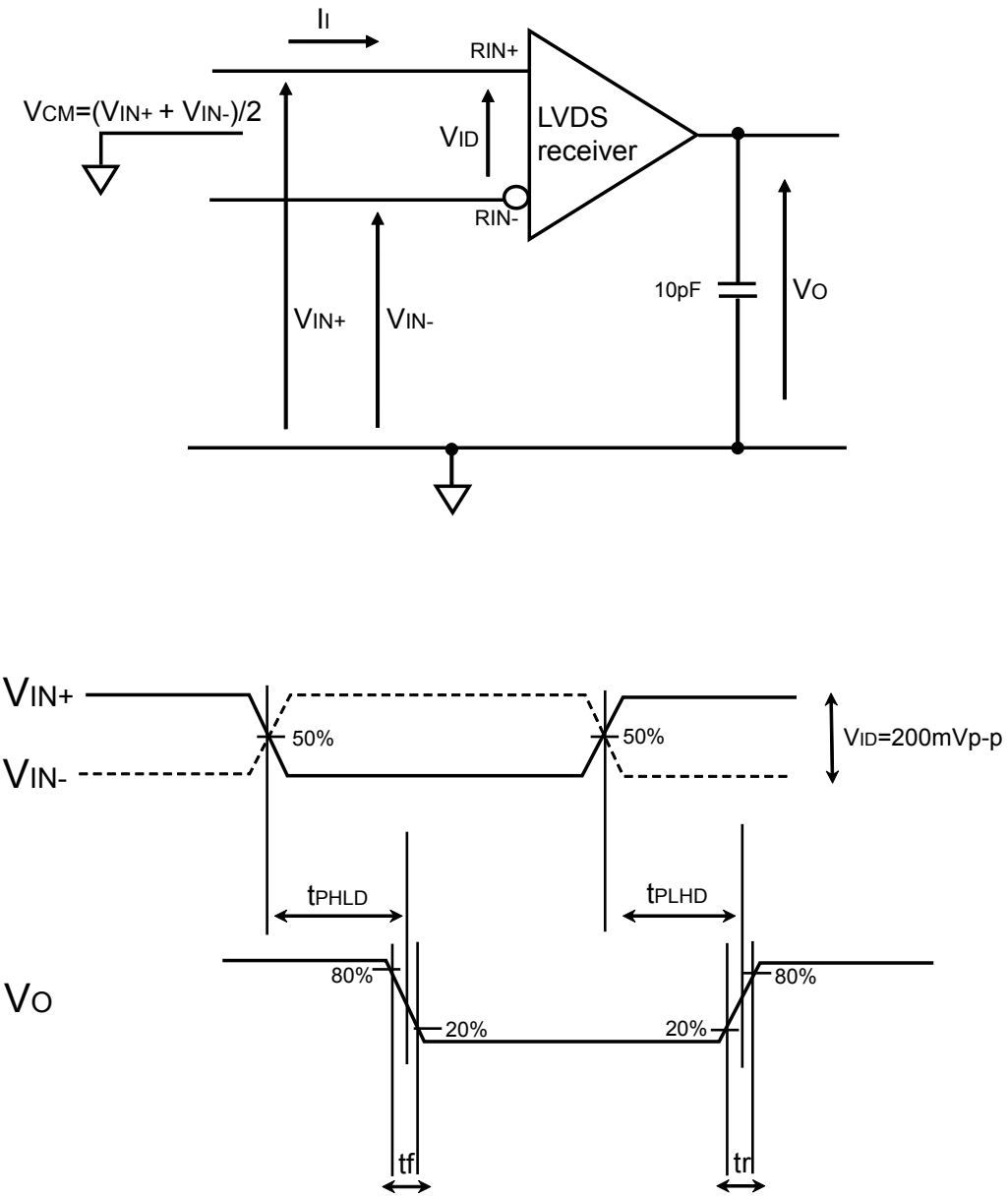
- All input pulses are supplied by a generator with the following characteristics:
  Tr or Tf ≤ 1 ns, f = 1 MHz, ZO = 50 Ω, and duty cycle = 50%.
- The product is guaranteed in test with CL = 10 pF.

Figure 5. Enable and disable waveforms for the driver



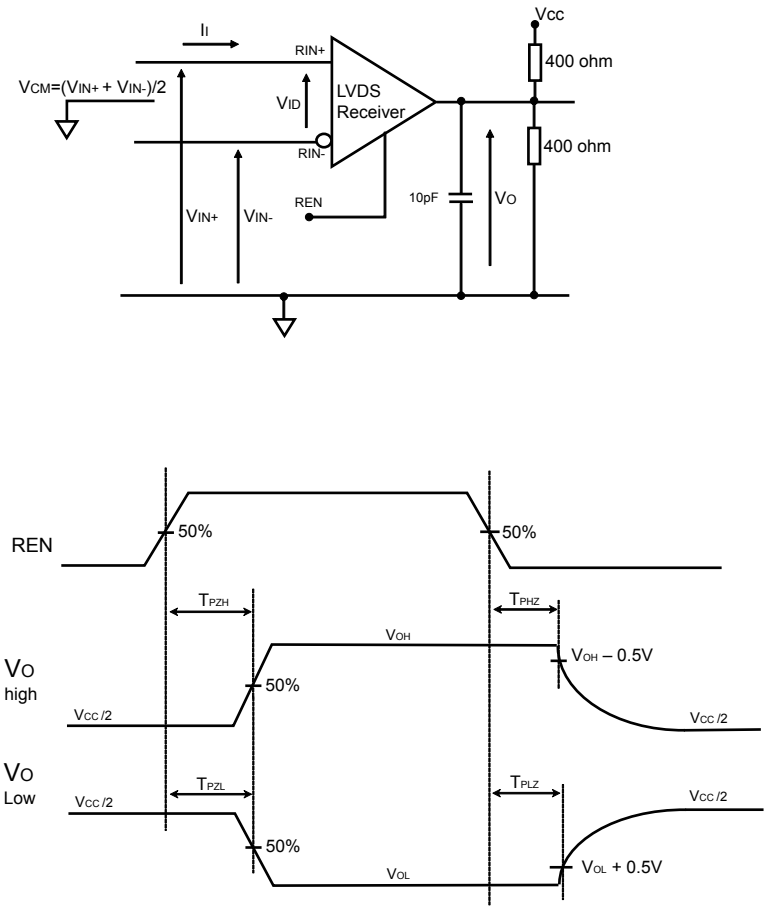
- All input pulses are supplied by a generator with the following characteristics: Tr or Tf ≤ 1 ns, f_{DEN} = 500 kHz, and pulse width on DEN = 500 ns.
- The product is guaranteed in test with CL = 10 pF.

Figure 6. Timing test circuit and waveforms for the receiver



- All input pulses are supplied by a generator with the following characteristics: Tr or Tf ≤ 1 ns, f = 1 MHz, ZO = 50 Ω, and duty cycle = 50%.
- The product is guaranteed in test with CL = 10 pF.

Figure 7. Enable and disable waveforms for the receiver



- All input pulses are supplied by a generator with the following characteristics: Tr or Tf ≤ 1 ns, f_{REN} = 500 kHz, and pulse width on REN = 500 ns.
- The product is guaranteed in test with CL = 10 pF.

5 Radiations

Total ionizing dose (TID):

For the qualification, the product is characterized in TID as per MIL-STD-883 TM 1019 up to 50 krad(Si) on 5 biased parts at high dose rate, such a rate being the worst condition for a pure CMOS technology.

All parameters provided in Table 6. Electrical characteristics apply to both pre- and post-irradiation.

Each new production lot is tested at high dose rate as per MIL-STD-883 TM 1019 on 5 parts.

Heavy-ions:

Single event latchup (SEL) is characterized at 125 °C at a LET of 62.5 MeV.cm2/mg. The test shows the product is immune to heavy ions at this LET. Heavy-ion trials are performed on qualification lots only.

The results in radiation are summarized in Table 7. Radiations as follows:

Table 7. Radiations

Symbol	Characteristics	Value
TID (1)	• High-dose rate (40 krad (Si) / h) • Temperature: 25 °C • Performed on 5 biased parts	Within Table 6. Electrical characteristics up to 50 krad(Si)
SEL(2)	• LET: 62.5 MeV.cm2/mg (Xenon ions) • Temperature: 125 °C • Fluence: 1 x 10^7 ions/cm^2 (10 million of particles per cm^2) • Normal incidence	Immune to SEL up to 62.5 MeV.cm^2/mg

1. *A total ionizing dose (TID) of 50 krad(Si) is equivalent to 500 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latchup.*

6 Outgassing

Specification (tested per ASTM E 595)	Value	Unit
Recovered mass loss (RML)[1]	0.06	%
Collected volatile condensable material (CVCM)[2]	0.00	%

1. *RML < 1%.*
2. *CVCM < 0.1%.*

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 TSSOP-20 package information

Figure 8. TSSOP-20 package outline

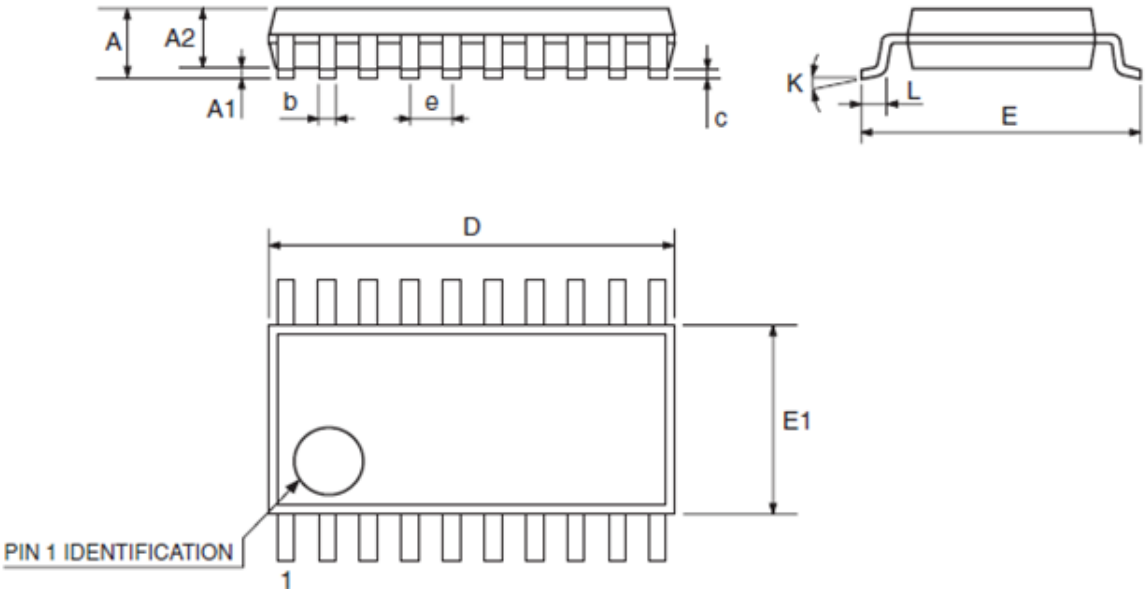


Table 8. TSSOP-20 package mechanical data

Symbol	Milimeters			Inches[1]		
	Min.	Typ.	Max.	Min	Typ	Max
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		
c	0.09		0.20	0.004		
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

7.2 TSSOP-20 packing information

Figure 9. **TSSOP-20 Carrier tape (dimensions in mm) outline**

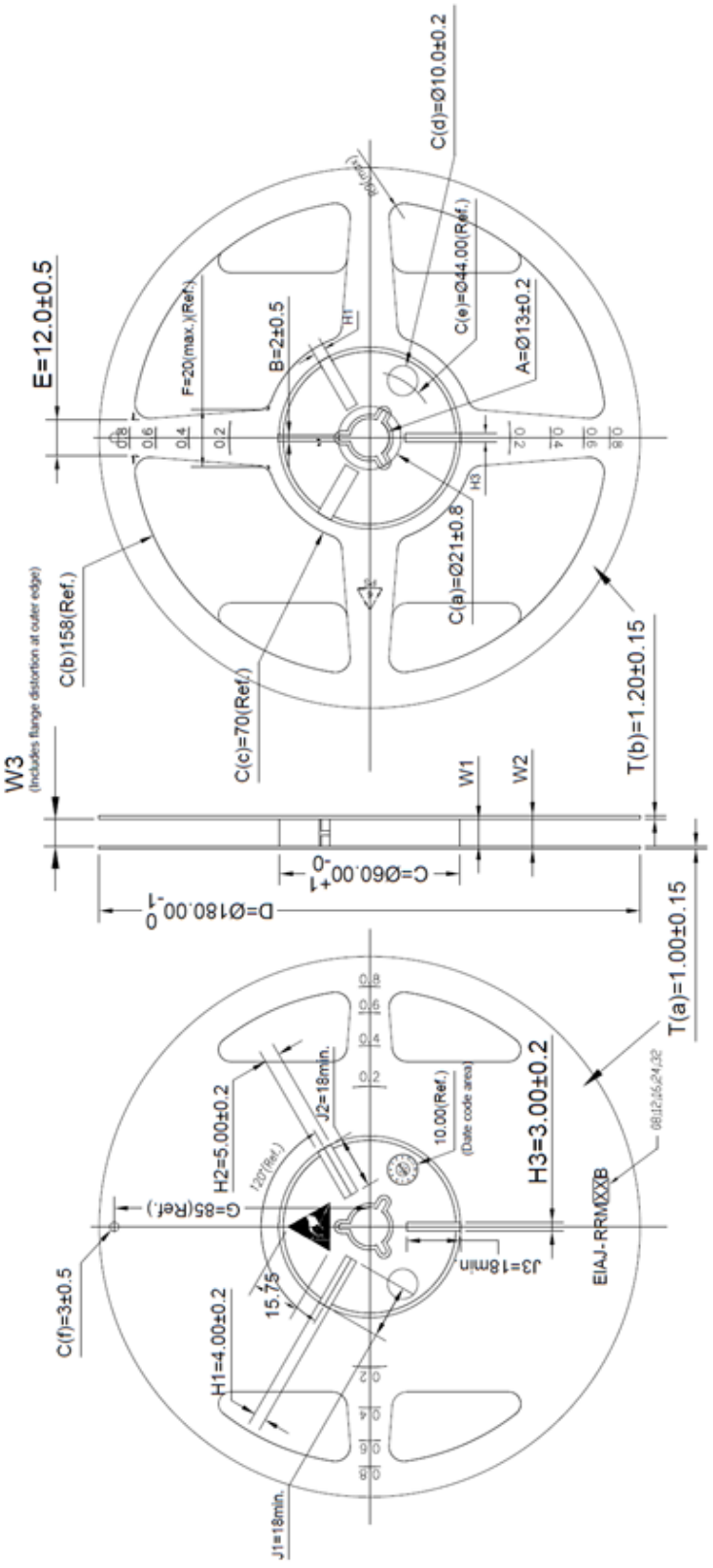
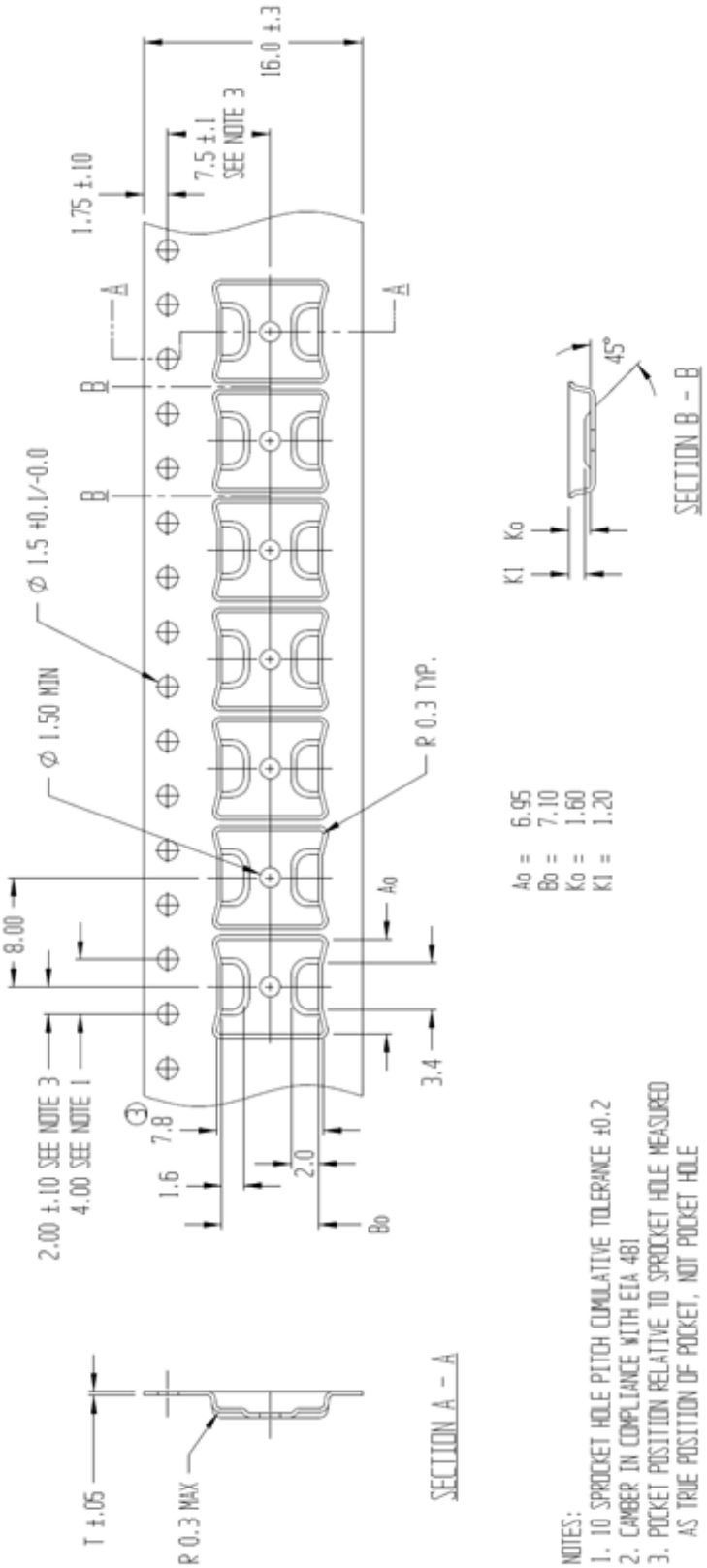


Figure 10. **TSSOP-20 tape (dimensions in mm) outline**



8 Ordering information

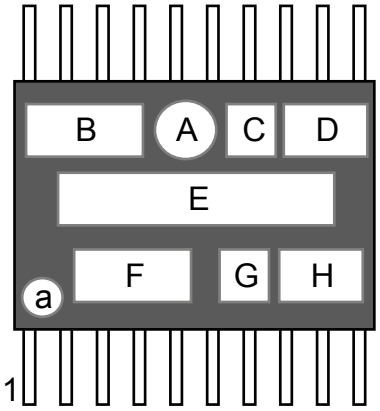
Table 9. Ordering information

Order code	Quality Level	Package	Lead-finish	Marking	Packing
LEOLVDSRDPT-D	Development sample	TSSOP-20	NiPdAu	DLEOLVDSRD	Tape and reel
LEOLVDSRDPT	Flight model	TSSOP-20	NiPdAu	LEOLVDSRD	Tape and reel

Table 10. Order code

LEO	LVDSRD	P	T
LEO qualification	Name	TSSOP-20 package	Tape and reel

Figure 11. TSSOP-20 marking



a: pin-1 reference
A : Second Level of interconnexion (type of lead-finishing)
B: ST logo
C: Assy plant
D: Lot code
E: Marking area
F: Country of origin
G: Assy year
H: Assy week

Revision history

Table 11. **Document revision history**

Date	Version	Changes
14-Jun-2021	1	Initial release.
30-Aug-2021	2	Updated Section 8 Ordering information.
14-Sep-2021	3	Updated Table 6. Electrical characteristics.
15-Jun-2022	4	Updated Features on the cover page.

Contents

List of tables

List of figures