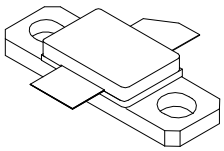
LET16045C

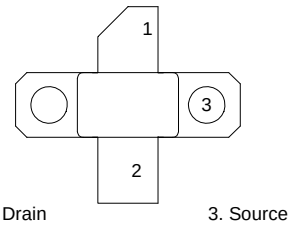
RF power transistor from the LdmoST family of n-channel enhancement-mode lateral MOSFETs

Datasheet - production data



M243
epoxy sealed

Figure 1. Pin out



1. Drain
2. Gate
3. Source

Features

- Excellent thermal stability
- Common source configuration
- P_{OUT} (@28 V) = 45 W with 16 dB gain @ 1600 MHz
- BeO free package
- In compliance with the 2002/95/EC European directive

Description

The LET16045C is a common source N-channel enhancement-mode lateral field-effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1.6 GHz. The LET16045C is designed for high gain and broadband performance operating in common source mode at 28 V. It is ideal for INMARSAT satellite communications.

Table 1. Device summary

Order code	Package	Branding
LET16045C	M243	LET16045C

1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	-0.5 to +15	V
I_D	Drain current	9	A
P_{DISS}	Power dissipation (@ T_C = 70 °C)	100	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Junction-case thermal resistance	1.3	°C/W

2 Electrical characteristics

T_C = 25 °C

Table 4. Static

Symbol	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V; I_{DS} = 10 mA	80			V
I_{DSS}	V_{GS} = 0 V; V_{DS} = 28 V			1	µA
I_{GSS}	V_{GS} = 20 V; V_{DS} = 0 V			1	µA
$V_{GS(Q)}$	V_{DS} = 28 V; I_D = 300 mA	2.0		5.0	V
$V_{DS(ON)}$	V_{GS} = 10 V; I_D = 3 A			1.1	V
G_{FS}	V_{DS} = 10 V; I_D = 3 A	2.5			mho
C_{ISS}	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz		58		pF
C_{OSS}	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz		29		pF
C_{RSS}	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz		0.8		pF

Table 5. Dynamic

Symbol	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	V_{DD} = 28 V; I_{DQ} = 400 mA; P_{IN} = 2 W	45	54	-	W
G_{PS}	V_{DD} = 28 V; I_{DQ} = 400 mA; P_{OUT} = 45 W	15	16		dB
h_D	V_{DD} = 28 V; I_{DQ} = 400 mA; P_{OUT} = 45 W	50	55		%
Load mismatch	V_{DD} = 28 V; I_{DQ} = 400 mA; P_{OUT} = 50 W; f = 1600 MHz All phase angles		20:1		VSWR

Table 6. Impedance data

Frequency (MHz)	Z source (Ω)	Z load (Ω)
1600	1.1 - j1.6	1.1 - j0.6

3 Typical performances

Figure 2. Gain and efficiency vs output power

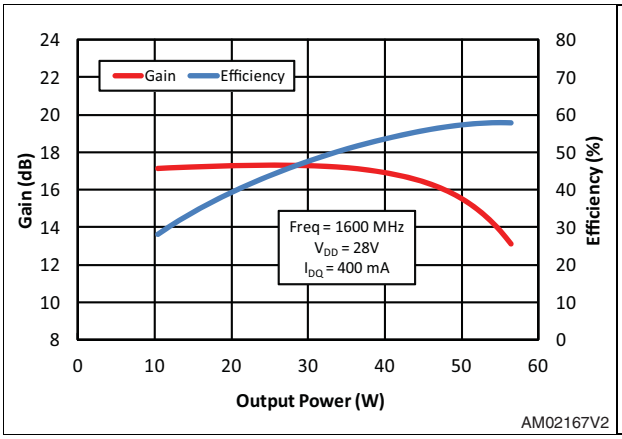


Figure 3. Gain vs ouptut power and bias current

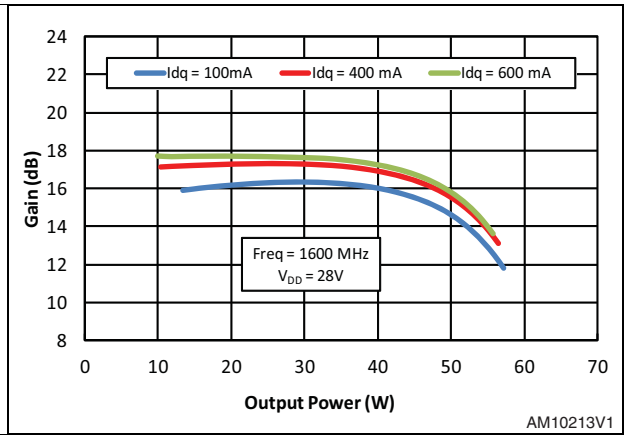
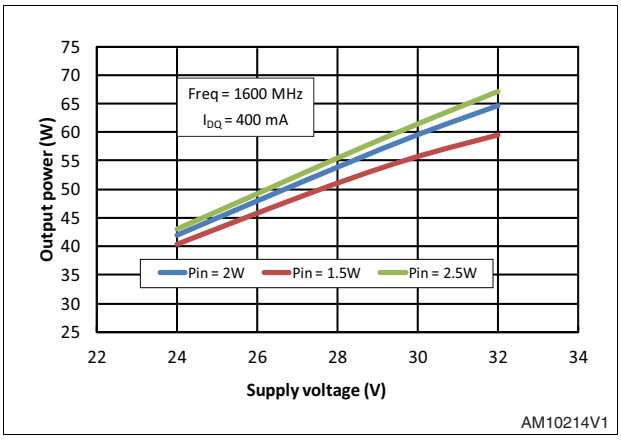


Figure 4. Ouptut power vs drain supply voltage



4 Board layout, schematic and BOM

Figure 5. Board layout

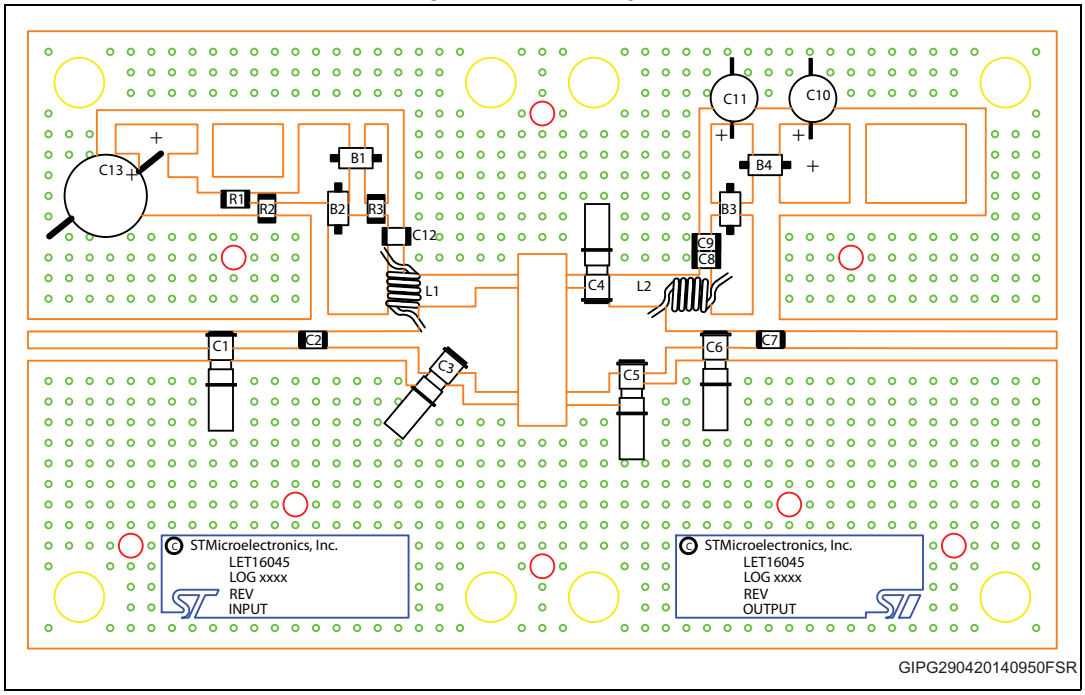


Figure 6. Schematic

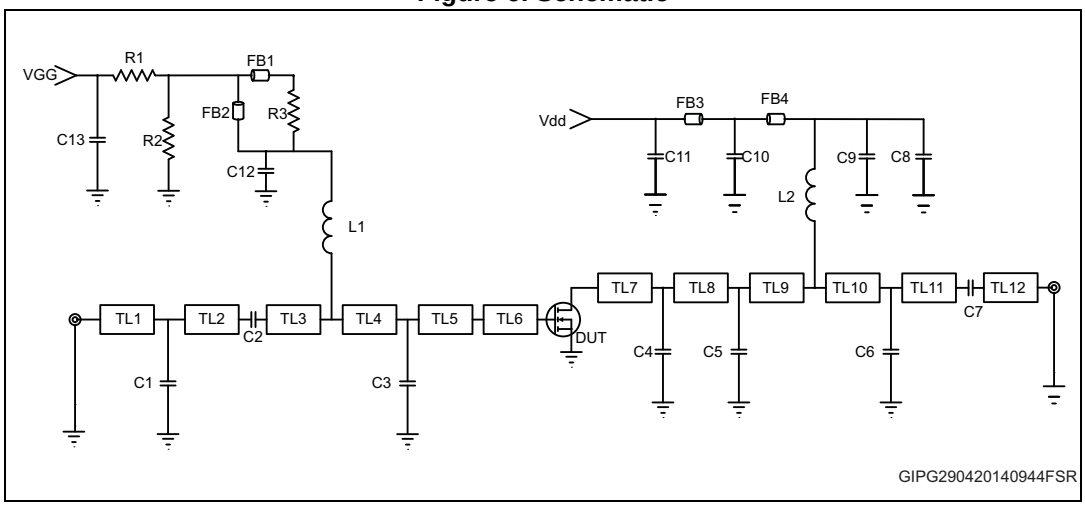


Table 7. Component list

Item	Qty	Part number	Vendor	Description
R1	1	CR1206-8W-561JB	VENKEL	560 OHM, 1/8W surface mount chip resistor
R2	1	CR1206-8W-132JB	VENKEL	1.3K OHM, 1/8W surface mount chip resistor
R3	1	CR1206-8W-100JB	VENKEL	10 OHM, 1/8W surface mount chip resistor
FB1,2,3,4,	4	2743021447	FAIR-RITE CORP	Surface Mount EMI sheild bead
C1,C4,C5,C6	4		JOHANSON	0.6-4.5pF giga trim variable capacitor
C2,C7,C9,C12	4	ATC100B470XXXX	ATC	47 pF chip capacitor
C3	1	27291PC	JOHANSON	0.8-8pF giga trim variable capacitor
C8	1	ATC100B330XXXX	ATC	33pF chip capacitor
C10	1			330uF, 50V electrolytic capacitor
C11	1			10uF, 63V electrolytic capacitor
C13	1			100uF, 63V electrolytic capacitor
L1, L2	2	1812SMS-33NJ	Coilcraft	33 nH coil
TL1, TL2	2			L= 1.350in [34.29mm] W=0.082in [2.080mm]
TL3	1			L= 0.469in [11.91mm] W=0.080in [2.020mm]
TL4, TL5	2			L= 0.277in [7.03mm] W=0.323in [8.210mm]
TL6	1			L= 0.207in [5.26mm] W=0.506in [12.85mm]
TL7	1			L= 0.208in [5.28mm] W=0.506in [12.85mm]
TL8,TL9	2			L= 0.275in [6.98mm] W=0.324in [8.230mm]
TL10,TL11	2			L= 0.470in [11.93mm] W=0.080in [2.020mm]
TL12	1			L= 1.351in [34.33mm] W=0.082in [2.080mm]
Board 3X5	1		Rogers Corp	Er=2.55 t=0.0026in h=0.030in

5 Package mechanical data

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Figure 7. M243 package dimensions

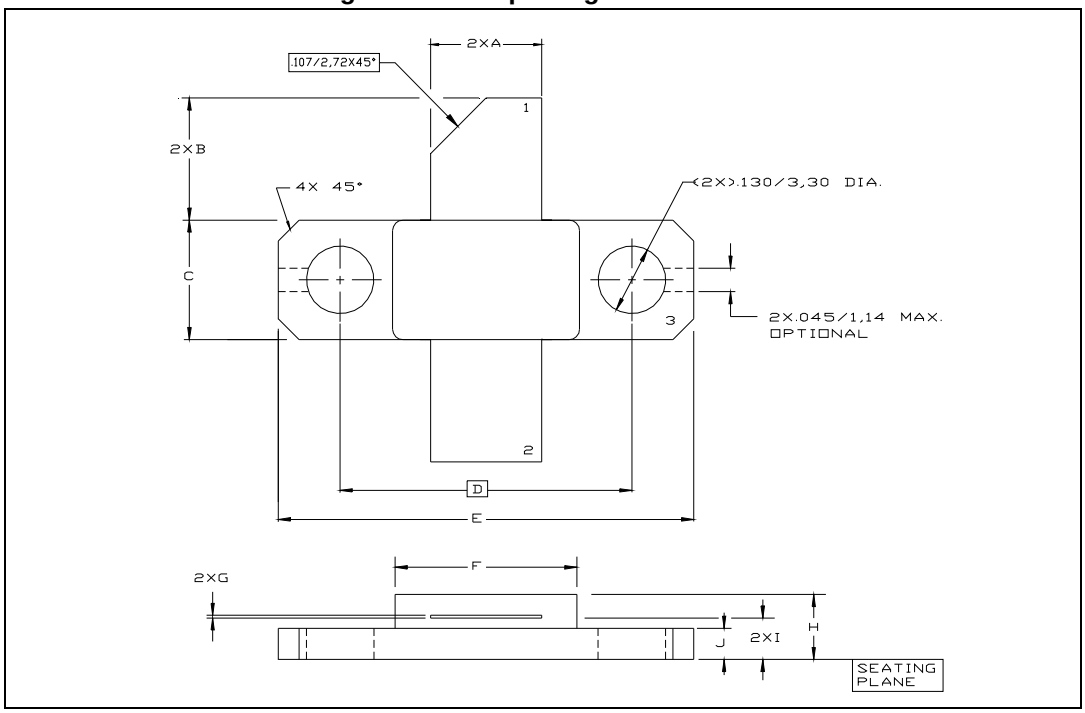

Table 8. M243 (.230 x .360 2L N/HERM W/FLG) mechanical data

Dim.	mm			inch		
	Min.	Typ	Max.	Min.	Typ	Max.
A	5.21		5.72	0.205		0.225
B	5.46		6.48	0.215		0.255
C	5.59		6.1	0.22		0.24
D		14.27			0.562	
E	20.07		20.57	0.79		0.81
F	8.89		9.4	0.35		0.37
G	0.1		0.15	0.004		0.006
H	3.18		4.45	0.125		0.175
I	1.83		2.24	0.072		0.088
J	1.27		1.78	0.05		0.07

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Sep-2011	1	Initial release.
04-Nov-2011	2	Updated *Table 3: Thermal data*, *Table 4: Static*, *Table 5: Dynamic* and *Figure 3: Gain vs ouptut power and bias current*. Inserted *Table 6: Impedance data* and *Figure 2: Gain and efficiency vs output power* and *Figure 4: Ouptut power vs drain supply voltage*.
29-Apr-2014	3	Added *Section 4: Board layout, schematic and BOM*.

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