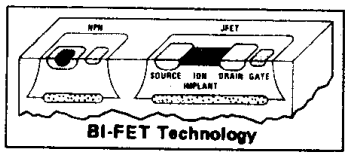
National Semiconductor

A to D, D to A



LF13300 Integrating A/D Analog Building Block

General Description

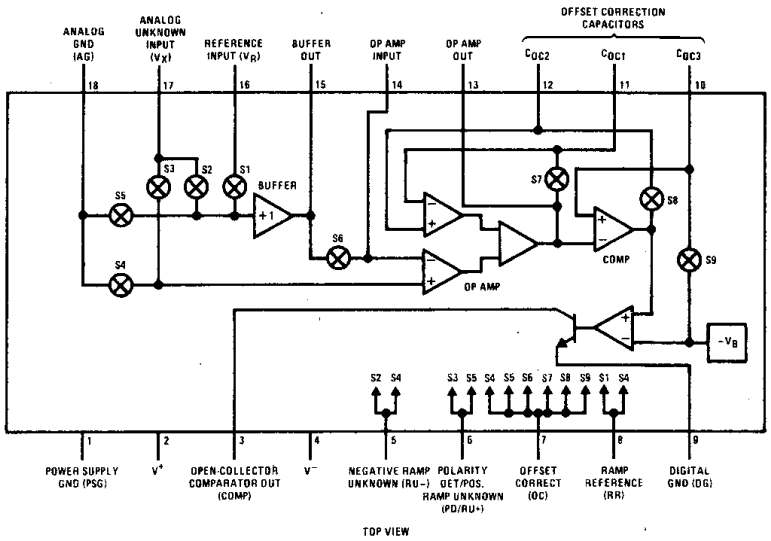
The LF13300 is the analog section of a precision integrating analog-to-digital (A/D) system. JFET and bipolar transistors (BI-FET) are combined on the same chip to provide a high input impedance unity gain buffer, comparator and integrator, along with 9 JFET analog switches. The LF13300 has sufficient resolution to construct up to a 4 1/2-digit Digital Panel Meter (DPM) or a 12-bit (plus sign) Data Acquisition System and is specifically designed for use with the ADB1200 12-bit binary building block.

*See ADB1200 data sheet for more information.

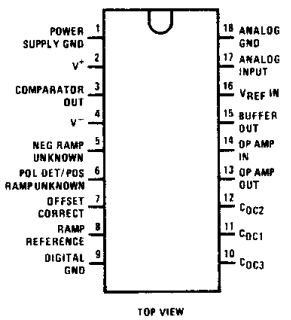
Features

- Rugged JFETs allow blow-out free handling
- High input impedance 10,000 MΩ typ
- Automatic offset correction
- Analog circuitry can be physically and electrically isolated from high noise digital circuits
- Analog input range of ±11V with ±15V supplies
- Wide power supply voltage range ±5V to ±18V
- TTL and CMOS compatible logic
- Can interface directly with microprocessors
- Versatile: can be used as a 12-bit plus sign binary A/D, 4 1/2-digit, 3 3/4-digit and 3 1/2-digit Digital Panel Meter (DPM)
- Low cost

Block and Connection Diagrams



Dual-In-Line Package



Order Number LF13300D
See NS Package D18A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation, (Note 1)	570 mW
Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

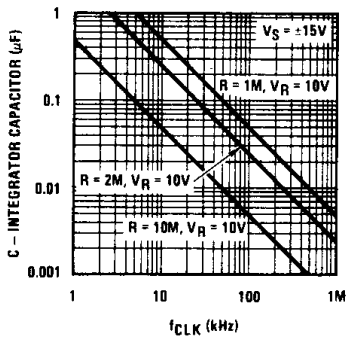
Electrical Characteristics (V_S = ±15V, T_A = 25°C, unless otherwise noted)

PARAMETER	CONDITIONS	TEST CIRCUIT	LF13300 MIN	LF13300 TYP	LF13300 MAX	UNITS
Analog Input Current, I_{IN}	V_X = 0	1, 2		80	500	pA
	$T_{MIN} \leq T_A \leq T_{MAX}$				5	nA
Analog Input Voltage Range	V_X Adjusted until $\|I_{IN}\| \geq$ 10 nA	1, 2			±11	V
Analog Input Resistance	V_X = 0	1, 2		10,000		MΩ
Reference Input Currents, I_R	V_R = 10V			1	100	nA
	$T_{MIN} \leq T_A \leq T_{MAX}$	3			10	μA
Reference Input Voltage Range	V_R Adjusted until $\|I_R\| \geq 10\,\mu A$	3	0		11	V
Reference Input Resistance	V_R = 10V	3		1000		MΩ
Offset Correction Voltage, $-V_B$		4		−12		V
Offset Correction		5		20	2000	pA
Input Current, I_{OC}		5			20	nA
Op Amp Slew Rate		6		10		V/μs
Op Amp Bandwidth		7		3		MHz
Buffer Slew Rate		9		25		V/μs
Comparator Response Time	200 μV Input Stop, 100 μV Overdrive	11		2.5		μs
Comparator Output Saturation Voltage	V_{CC} = 5V, R_L = 2k, $T_{MIN} \leq T_A \leq T_{MAX}$	11		0.25	0.4	V
Logic "1" Input Voltage	All Switching Input Pins 5, 6, 7, 8, $T_{MIN} \leq T_A \leq T_{MAX}$		2.0		5.0	V
Logic "0" Input Voltage	All Switching Input Pins 5, 6, 7, 8, $T_{MIN} \leq T_A \leq T_{MAX}$		−2.0		0.8	V
Logic Input Current	All Switching Input Pins 5, 6, 7, 8, $0 \leq V_L \leq 5V$, $T_{MIN} \leq T_A \leq T_{MAX}$			15	50	μA
Power Supply Voltage Range ±V_S	$V_R \leq V^+ - 3V$, V_{IN} = 0V		±4.75		±18	V
				3.0		mA
				−5.5		mA
	$T_{MIN} \leq T_A \leq T_{MAX}$				±11	mA

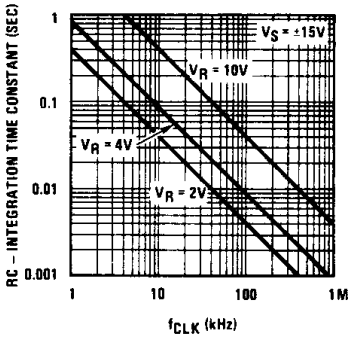
Note 1: For operating at elevated temperatures, the LF13300 in the dual-in-line package must be derated based on the thermal resistance of 100°C/W junction to ambient.

Typical Performance Characteristics

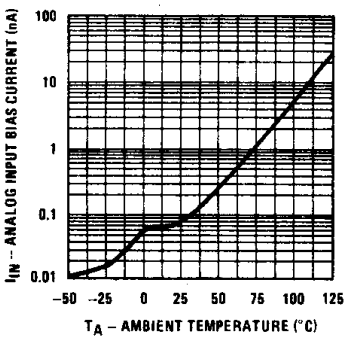
Integrator Capacitance, C vs f_{CLK} for Different Integrator Resistances, R



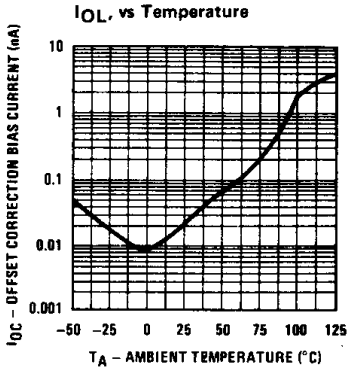
Integration Time Constant (RC) vs f_{CLK} for Different Reference Voltages, V_R



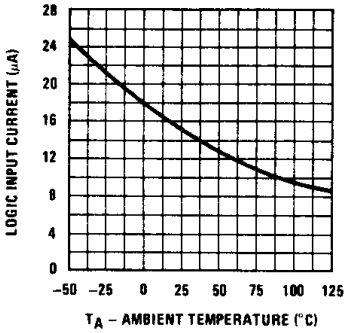
Analog Input Bias Current, I_{IN}, V_X = 0V, vs Temperature



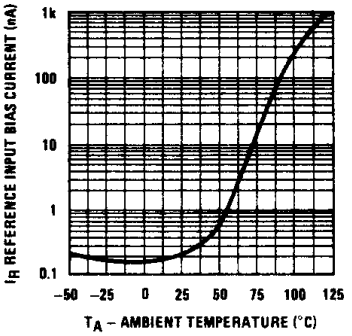
Offset Correction Bias Current, I_{OL}, vs Temperature



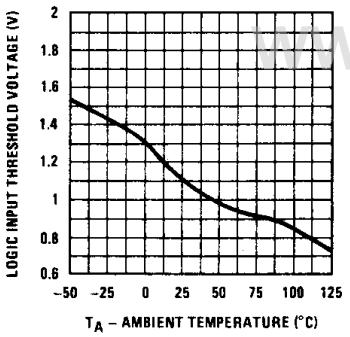
Logic Input Current vs Temperature



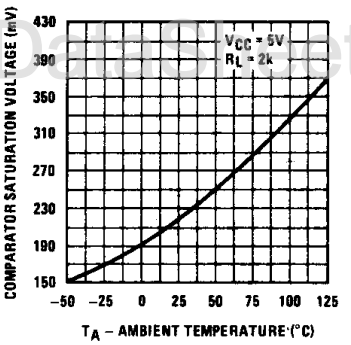
Reference Input Bias Current, I_R, vs Temperature



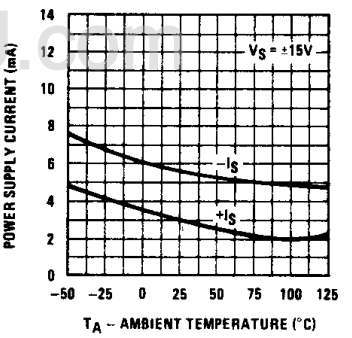
Logic Input Threshold Voltage vs Temperature



Comparator Saturation Voltage vs Temperature



Power Supply Current vs Temperature



Functional Description

The LF13300 goes through the following 5 states during normal cycle: 1) Offset Correction; 2) Polarity Determination; 3) Initialization; 4) Ramp Unknown; 5) Ramp Reference

Offset Correction Description *(Figure 1)*

The Offset Correction scheme will drive the input of the comparator to its switching threshold when the analog input is zero and the timing components, RC, are bypassed.

The Offset Correction input (OC) is driven high, closing switches S4–S9.

The offset voltages are assigned as follows: V_{OS1} – the input offset voltage of the buffer; V_{OS2} – the input offset voltage of A1; V_{OS3} – the input offset voltage of A2; V_{OS4} – the input offset voltage of the comparator.

S5 grounds the input of the buffer so that its output voltage is simply V_{OS1}. S6 bypasses R to keep the integration time constant, RC, from affecting the circuit operation. S4 makes the total equivalent input voltage to A1 be $-V_{OS1} - V_{OS2}$. S7 puts the op amp in a unity gain configuration with respect to the input of A2. S8 keeps the output voltage of the op amp at $-V_B + V_{OS4} = -V_B'$ (the Offset Correction potential) since the comparator is placed inside the loop. C3 samples the output of the $-V_B$ generator. The voltage at the non-inverting input of A2 is $-V_B - V_{OS1} -$

Functional Description (Continued)

$V_{OS2} - V_{OS3} + V_{OS4} = V1$. Thus, the sum of the offsets is stored on C1, and the differential voltage across the comparator is zero.

Polarity Determination *(Figure 2)*

The simplified diagram of the LF13300 in the Polarity Determination state is shown in *Figure 2*. S5 and S3 are closed during this period. S5 grounds the buffer input and V_X (the unknown voltage) is applied through S3 to the non-inverting input of A1. The equation that describes the op amp output voltage is given in *Figure 2*. When V_X is applied to A1 at t_1, the output of the op amp slews to V_X and is integrated until t_2, when S3 opens and S4 closes. At t_2, V_{OUT} slews down by $-V_X$ leaving $\frac{1}{RC}\int_{t_2}^{t_2} V_X dt - V_B'$ at the op amp output.

Just before t_2, the comparator senses the op amp output with respect to $-V_B$; the comparator output goes high if $V_X > 0$ and remains low if $V_X \leq 0$.

Initialization *(Figure 1)*

During initialization, the configuration is the same way as it is in the Offset Correction state and the op amp output is brought back to the Offset Correction potential $-V_B'$.

Ramp Unknown *(Figures 2 and 3)*

In the Ramp Unknown state, if $V_X \geq 0$, S3 and S5 are closed as shown in *Figure 2*, and V_X is applied to the + input of the integrator. If $V_X < 0$, the device is connected as in *Figure 3* with S2 and S4 closed. V_X is now applied through the buffer to the − input of the integrator. In either Ramp Unknown case, the op amp output ramps in the positive direction and V_X is applied to a high impedance JFET input.

Ramp Reference *(Figure 4)*

In this state, the LF13300 is configured with switches S1 and S4 closed. The reference voltage, V_R, a positive voltage, is applied to the buffer input and the op amp output ramps down until $V_{OUT} = -V_B'$ where the comparator will trip.

If V_X and V_R are assumed to be constant over their respective integration periods, the integrals of *Figure 4* are reduced to,

$$\frac{V_X (t_4 - t_3)}{RC} = \frac{V_R (t_5 - t_4)}{RC}$$

or

$$\frac{V_X}{V_R} = \frac{t_5 - t_4}{t_4 - t_3}.$$

Since $t_4 - t_3 = 4096$ clock periods and $t_5 - t_4$ can be measured in clock periods, $V_X/V_R = X/2^{12}$, where X is a digital binary output representing an analog input V_X with respect to V_R.

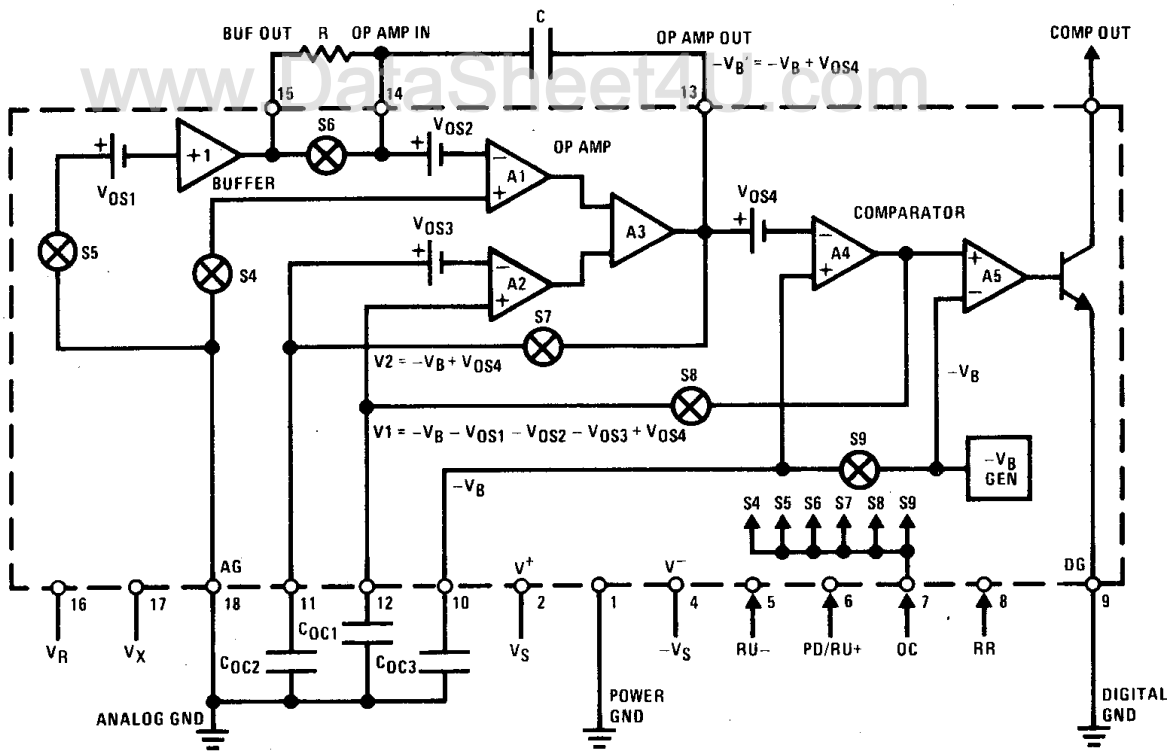


FIGURE 1. Offset Correction Circuit

Functional Description (Continued)

$$V_{OUT} = \begin{cases} -V_B' + V_X + \frac{1}{RC}\int_{t_3}^{t_4} V_X\,dt: \text{Ramp Unknown for } V_X \geq 0 \\ -V_B' + V_X + \frac{1}{RC}\int_{t_1}^{t_2} V_X\,dt: \text{Polarity Determination} \end{cases}$$

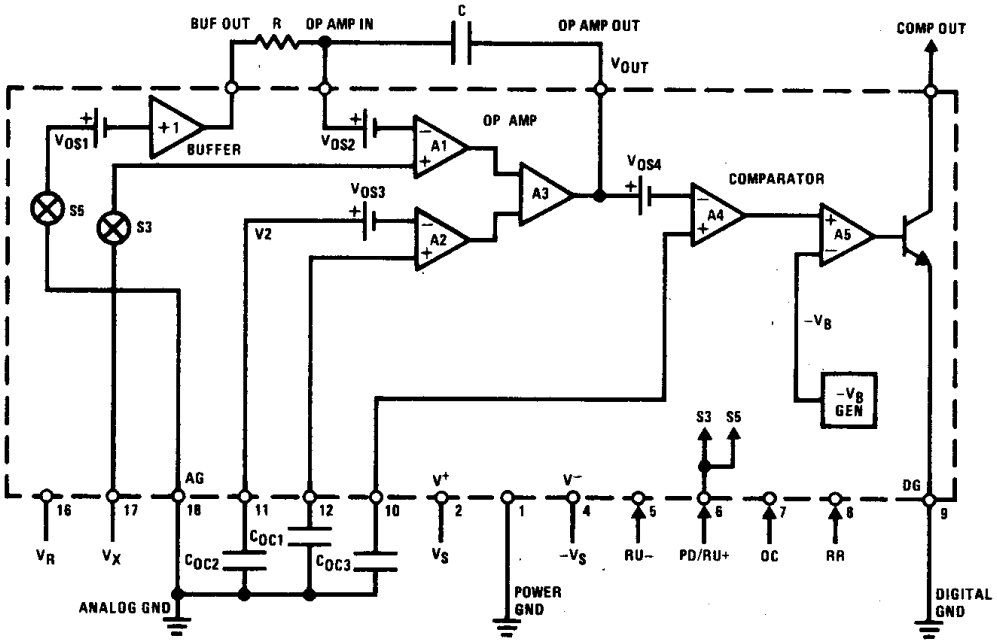


FIGURE 2. Polarity Determination Circuit or Ramp Unknown Circuit for $V_X \geq 0$

$$V_{OUT} = -V_B' + \frac{1}{RC}\int_{t_3}^{t_4} V_X\,dt: \text{Ramp Unknown for } V_X < 0$$

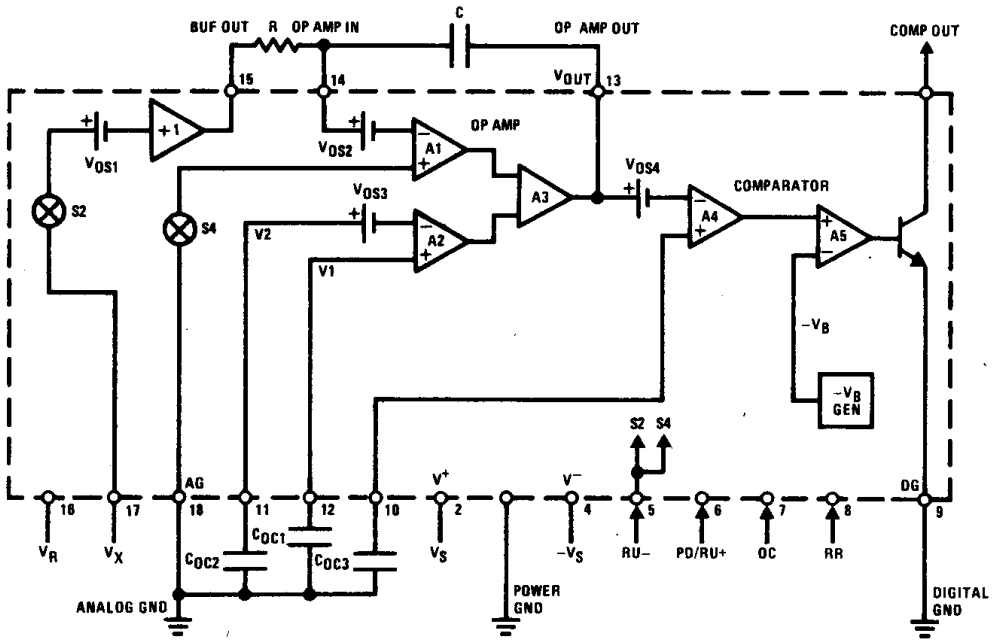
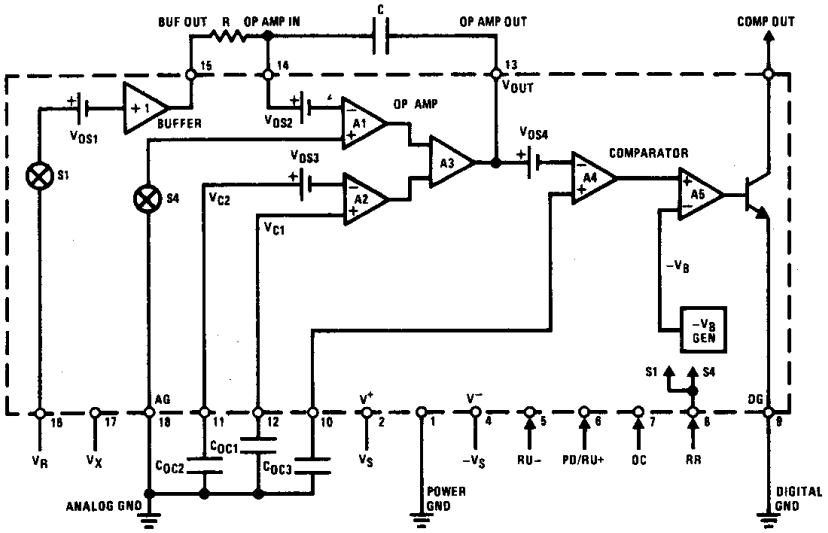


FIGURE 3. Ramp Unknown for $V_X < 0$

Functional Description (Continued)

$$V_{OUT}^{*} = -V_B' + \frac{1}{RC}\left(\int_{t_3}^{t_4} V_X\,dt - \int_{t_4}^{t_5} V_R\,dt\right)$$



*More accurately

$$V_{OUT} = -V_B' + \frac{1}{RC}\left(\int_{t_4}^{t_5+\Delta} V_R\,dt + \int_{t_3}^{t_4} V_X\,dt\right) + \delta$$

Where δ is the incremental voltage overdrive needed to fully switch the comparator and Δ is the sum of the additional time required to develop δ and the comparator propagation delay.

FIGURE 4. Ramp Reference Circuit

12-Bit A/D Converter Electrical Characteristics

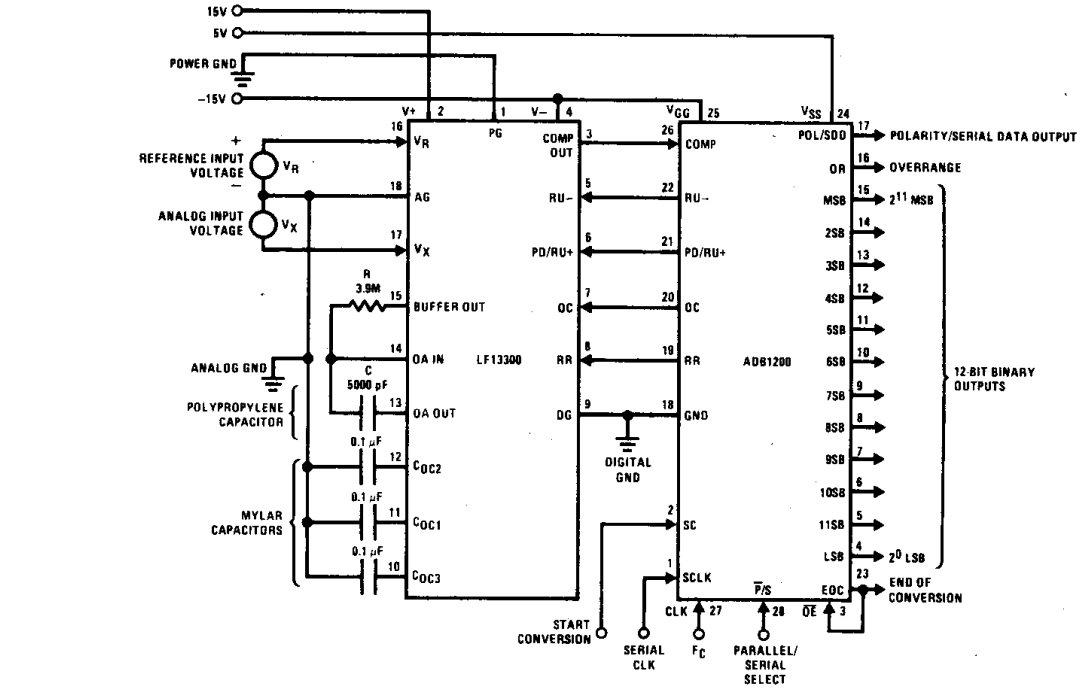
12-bit plus sign. (LF13300 with ADB1200). (V_R = 10.000V, F_C = 250 kHz, 0°C ≤ T_A ≤ +70°C unless otherwise noted.)

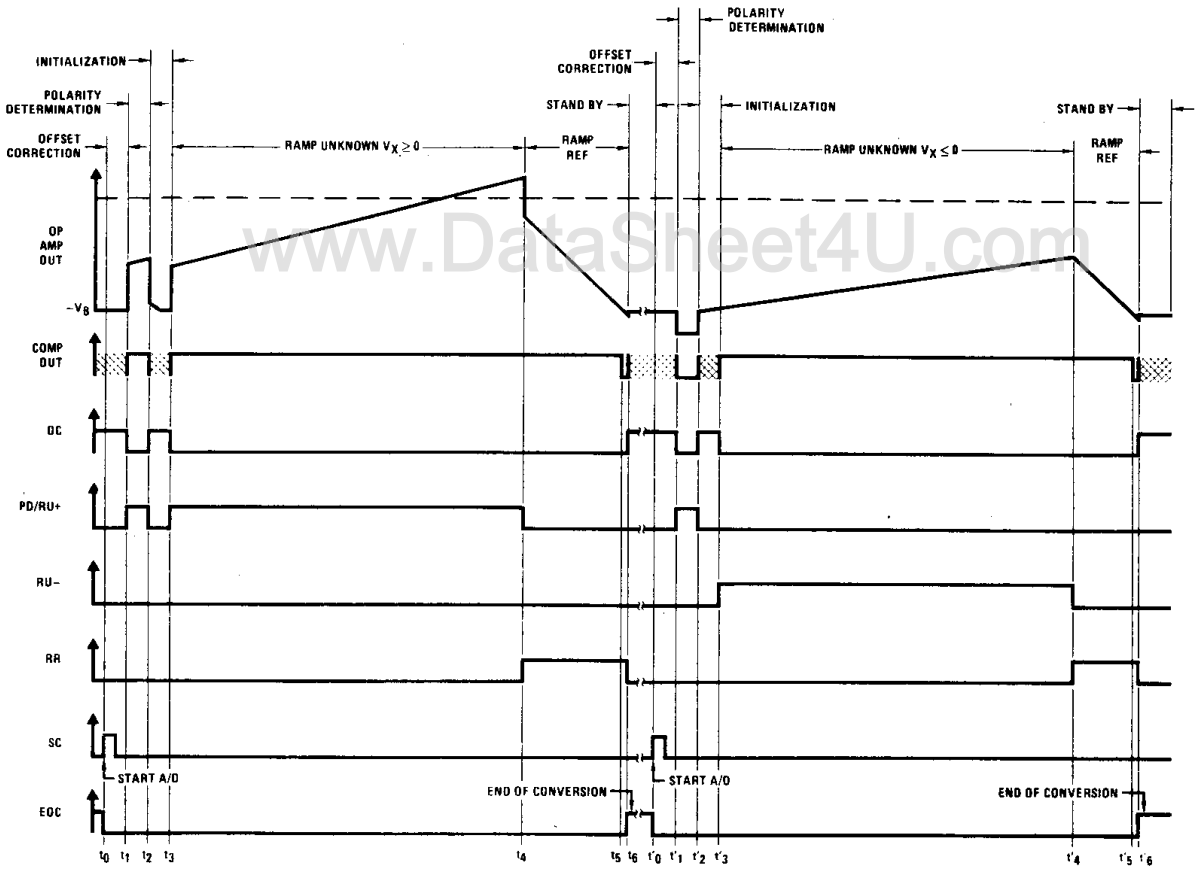
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution (Note 3)	V_R = 5.000V, −10V ≤ V_X ≤ +10V	13			Bits
	F_C = 125 kHz, T_A = 25°C	14			Bits
Non-Linearity			±1/8	±1/2	LSB
Ratiometric Gain Error (Def.)	V_X = ±10.000V, T_A = 25°C, (Note 2)		±1/2	±2	LSB
Gain Error Drift	V_X = 10.000V		±1		ppm/°C
Zero Reading Drift	V_X = 0V		±0.5		ppm/°C
Analog Input Voltage Range		±11	±12		V
Analog Input Leakage Current	V_X = 0V, T_A = 25°C		80	500	pA
Analog Input Resistance	V_X = 0V, T_A = 25°C	100	1000		MΩ
Reference Input Voltage Range	V_R Varied, T_A = 25°C	4		12	V
Reference Input Leakage Current	V_R = 10.000V, T_A = 25°C		1	100	nA
Reference Input Resistance	V_R = 10.000V, T_A = 25°C	100	1000		MΩ
Start Conversion Pulse Width	V_{SC} = 2.4V	2.4			μs
Conversion Time	V_{IN} = 10.000V $t_c = 8960/F_C$			36	ms
15V Supply Currents	LF13300, V^+ Current			11	mA
−15V Supply Currents	LF13300, V^- Current, ADB1200 V_{GG} Current		27	45	mA
5V Supply Currents	V_{IN} = 0V, ADB1200 V_{SS} Current		23	39	mA

Note 2: The A/D converter system must have been operational for a minimum of 30 seconds before this measurement is made. This is to relax the dielectric absorption effects of the integration capacitor, C.

Note 3: Polarity and Overrange outputs are considered as additional output bits.

12-Bit A/D Converter Circuit and Timing Diagrams





*Note. All TTL signal level.

FIGURE 5.

Application Hints

Increasing the Input Impedance of the LF13300, MM5863 12-Bit A/D Converter

The input impedance of the LF13300, ADB1200 (MM5863) A/D converter can be increased 1 to 2 orders of magnitude over the typical 1000 MΩ cited in the 12-bit A/D specifications by insuring that the signals that switch the LF13300 do not overlap. A circuit that eliminates switching overlap by introducing a Delay (t_d) ≈ 3.3k x 100 pF ≈ 300 ns to the rising edge of the signals from the ADB1200 (MM5863) is shown in *Figure 6*. *Figure 7* shows the operation of this circuit. The total delay time t_r' of the output will be equal to the inherent gate rise time, t_r, plus the RC delay, t_d. The fall time, t_f will be the basic gate delay.

Nulling the Residual Offset

The residual offset is < 200 μV which is negligible for most applications. This can be reduced to < 40 μV by lowering the clock frequency from 250 kHz to about 75 kHz. If a lower residual offset is required, we may trim out the remainder as shown in *Figure 8*. This circuit applies a negative step to the offset correction capacitor, C_{OC2}, by means of a variable capacitor which is adjusted until charge injection imbalance of the offset correction switches are cancelled.

Eliminating Errors Due to Power Supply Noise

For many applications, power supply noise (f ≥ 10 Hz) causes errors which reduces the accuracy of the system. In most applications, noise can be adequately eliminated by putting a series resistor (100Ω) in the power supply line with a 10 μF tantalum capacitor connected at the power supply pins *(Figure 9)*. The 10 μF capacitor is, in addition to the normal 0.1 μF ceramic disc capacitors, used as supply bypass capacitors.

Errors caused by noise on the negative supply, $-V_S$, can be further reduced by replacing, C_{OC3} with a 10 μF low leakage tantalum capacitor. Since $-V_B$ is 3V above $-V_S$, any noise appearing at $-V_S$ appears at $-V_B$; the 10 μF capacitor eliminates this noise.

Continuous Conversion Mode

For using the MM5863 in the continuous conversion mode, connect the end of conversion output, EOC (pin 23), to the output enable input, OE (pin 3), and connect the start conversion input, SC (pin 2) to 5V.

Miscellaneous

Since none of the output pins employ short-circuit protection, extreme care should be taken when breadboarding or troubleshooting with the power ON.

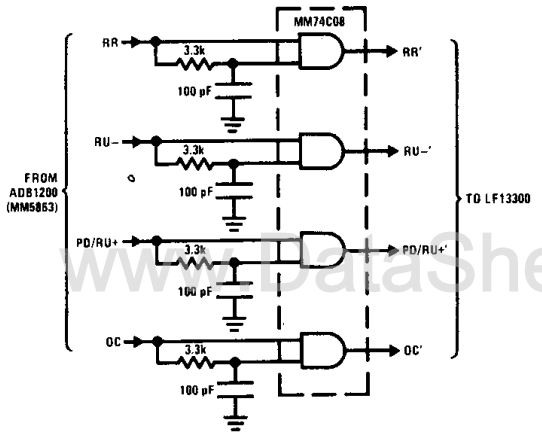


FIGURE 6. Overlap Elimination Circuit

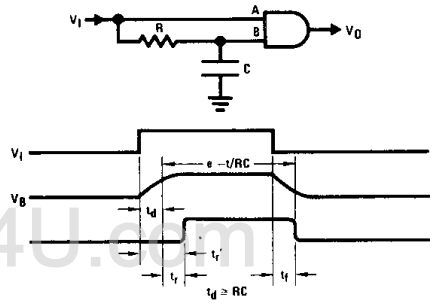


FIGURE 7. Rise Time Delay Circuit

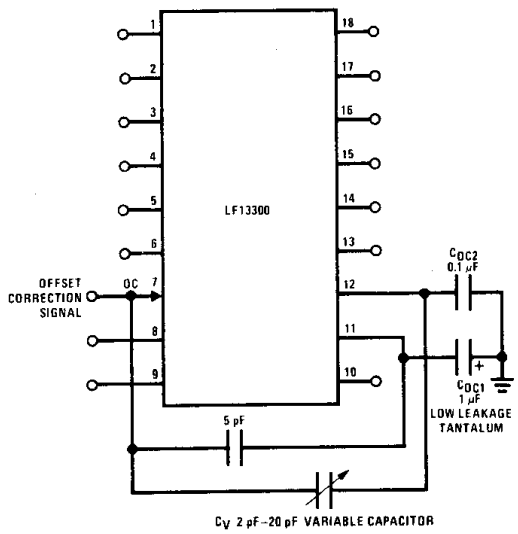


FIGURE 8. Residual Offset Nulling Circuit

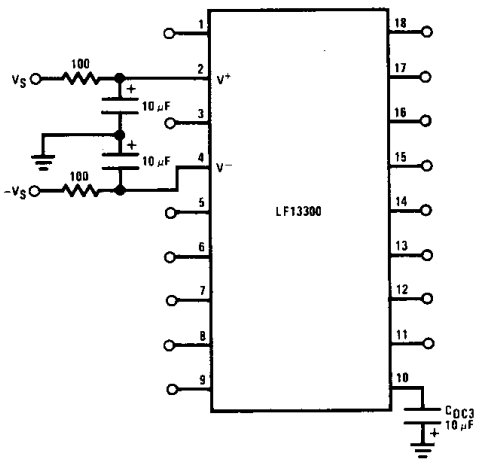
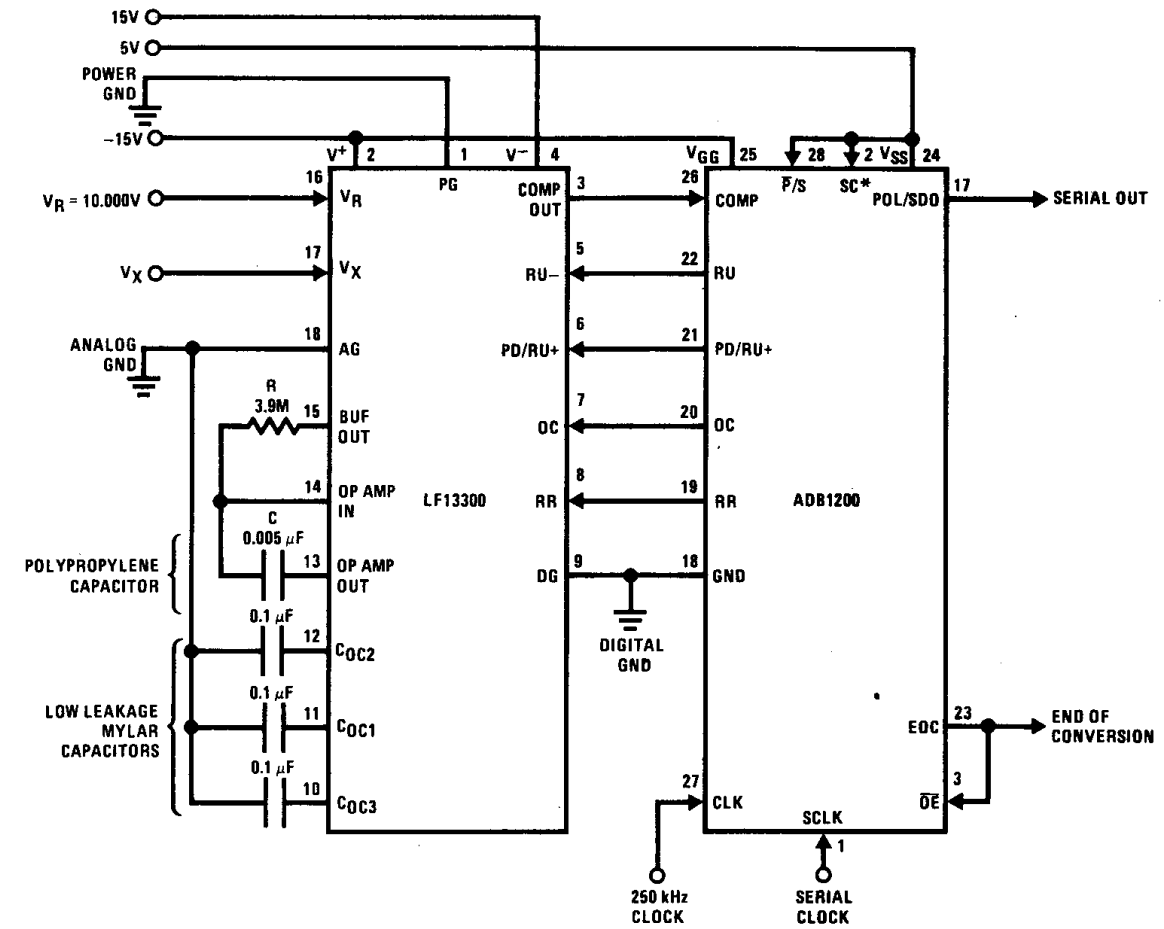


FIGURE 9. Power Supply Noise Reduction Circuit

Typical Applications



*SC at logic "1" for continuous conversion mode

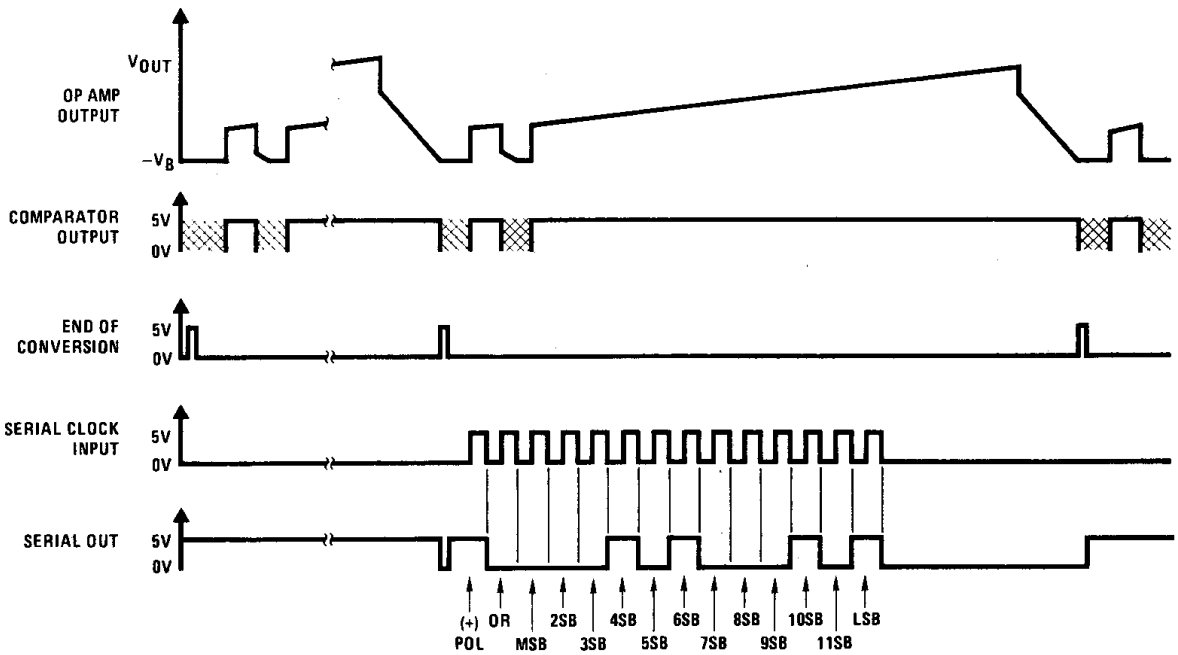
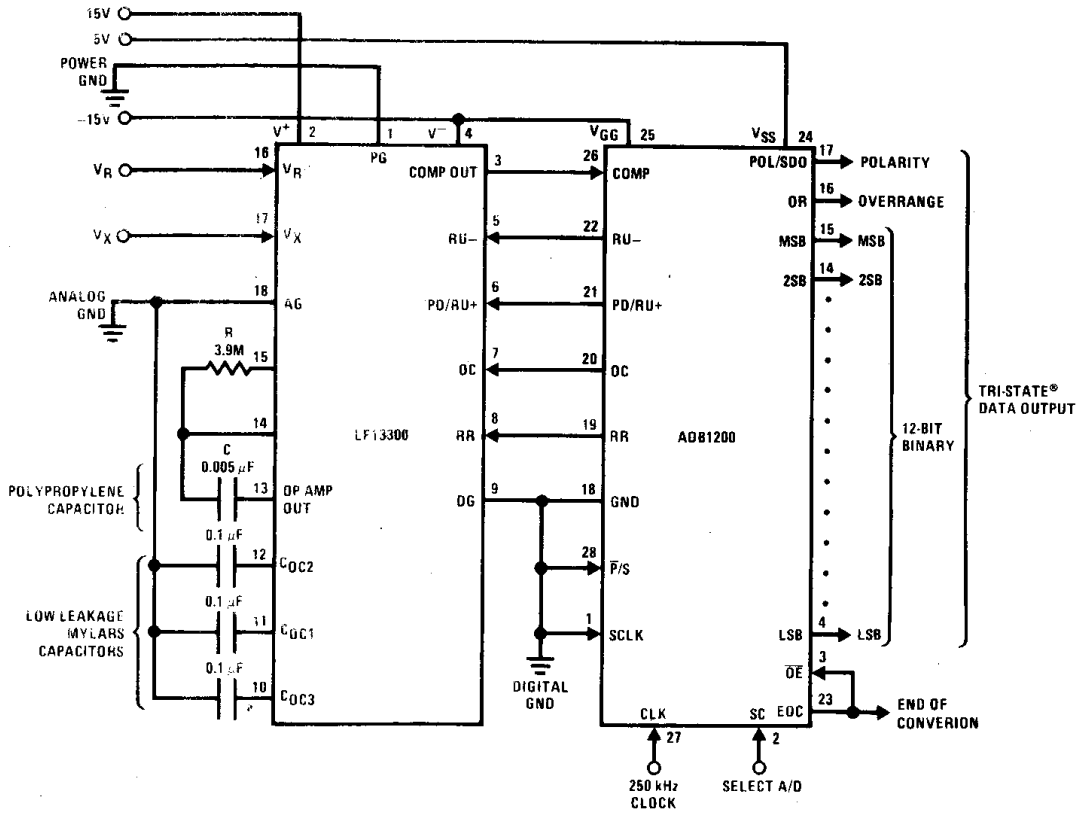
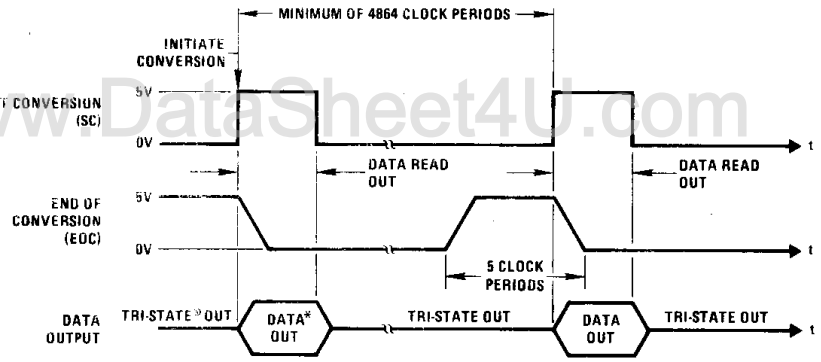


FIGURE 10. Continuous Conversion 12-Bit Plus Sign Serial Output A/D Using the LF13300 and the ADB1200

Typical Applications (Continued)





* Note. Prior to the first conversion cycle, the data outputs will all be in a "1" state when the outputs are enabled ($\overline{OE}$ in "0" state).

FIGURE 11. 12-Bit Plus Sign A/D in Command Conversion Mode

4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

Figure 12 shows a low speed, high accuracy, data acquisition unit where the analog input signal is acquired differentially and preconditioned through an LF352 monolithic instrumentation amplifier. To eliminate amplifier offset errors, autozeroing circuitry is added around the LF352 and is timed through the ADB1200 and flip-flop C. Flip-flops A and B form a 2-bit up counter for channel select.

The instrumentation amplifier is zeroed at power-up and after each conversion as shown in the timing diagram; during autozero the multiplexer is disabled. When the system does polarity detection and A/D conversion, the LF352 is active and the multiplexer is enabled. The zeroing cycle for the LF13300 and the LF352 lasts for 256 clock periods, so the maximum clock frequency will depend upon the required accuracy and the minimum zeroing time of the instrumentation amplifier. Notice here that the system accuracy will be less than 12 bits since it will be affected by the gain linearity of the instrumentation amplifier.

For more details concerning data acquisition, see AN-156 and LF11508/LF11509 data sheet. For details on the instrumentation amplifier, see the LF352 data sheet.

Typical Applications (Continued)

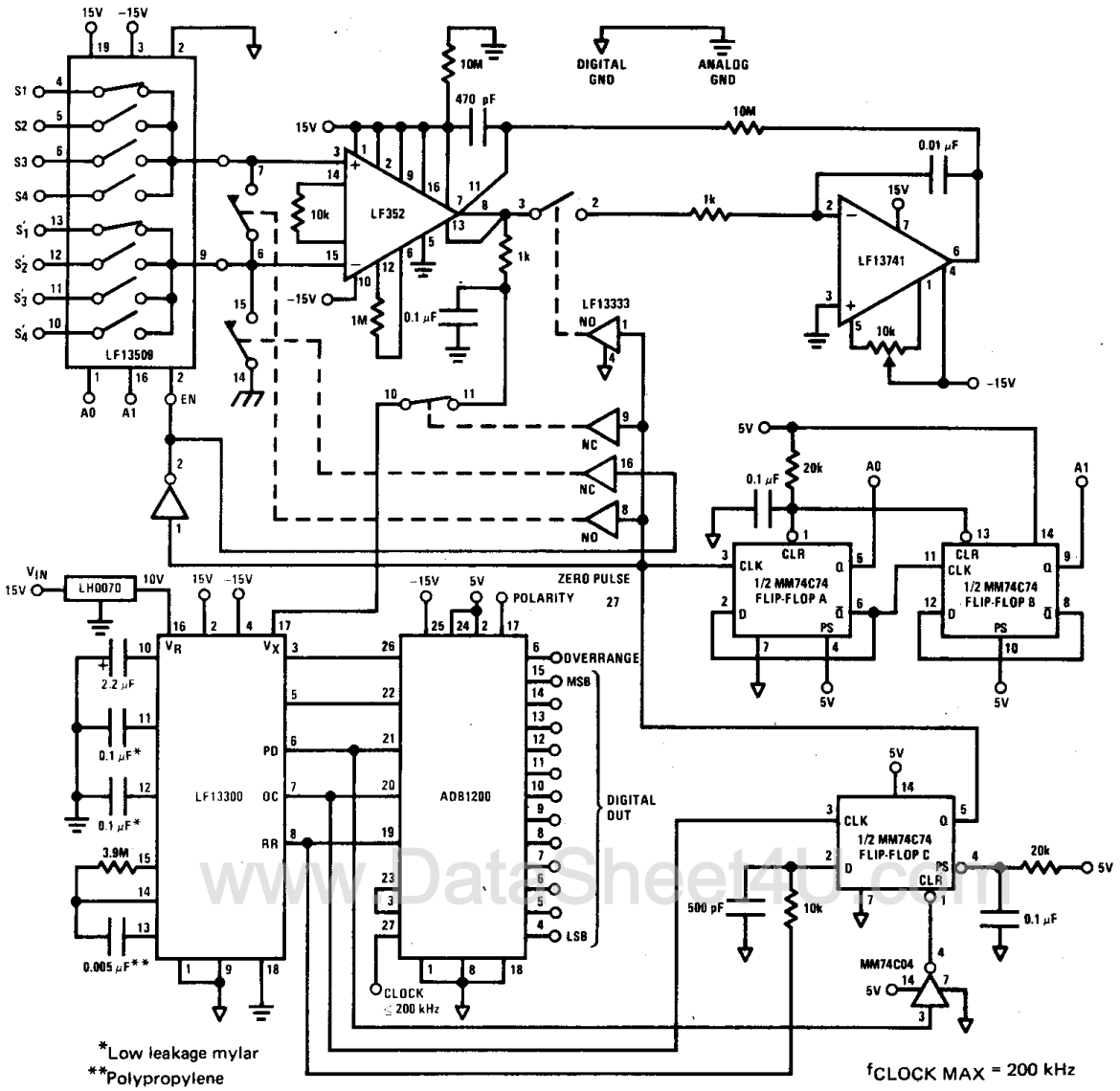


FIGURE 12. 4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

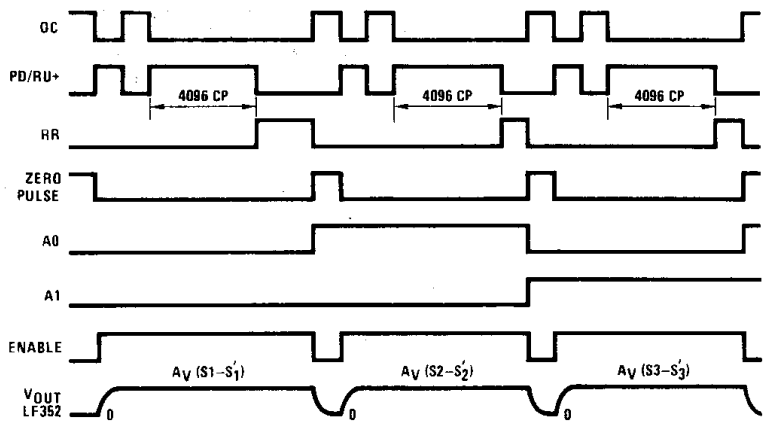
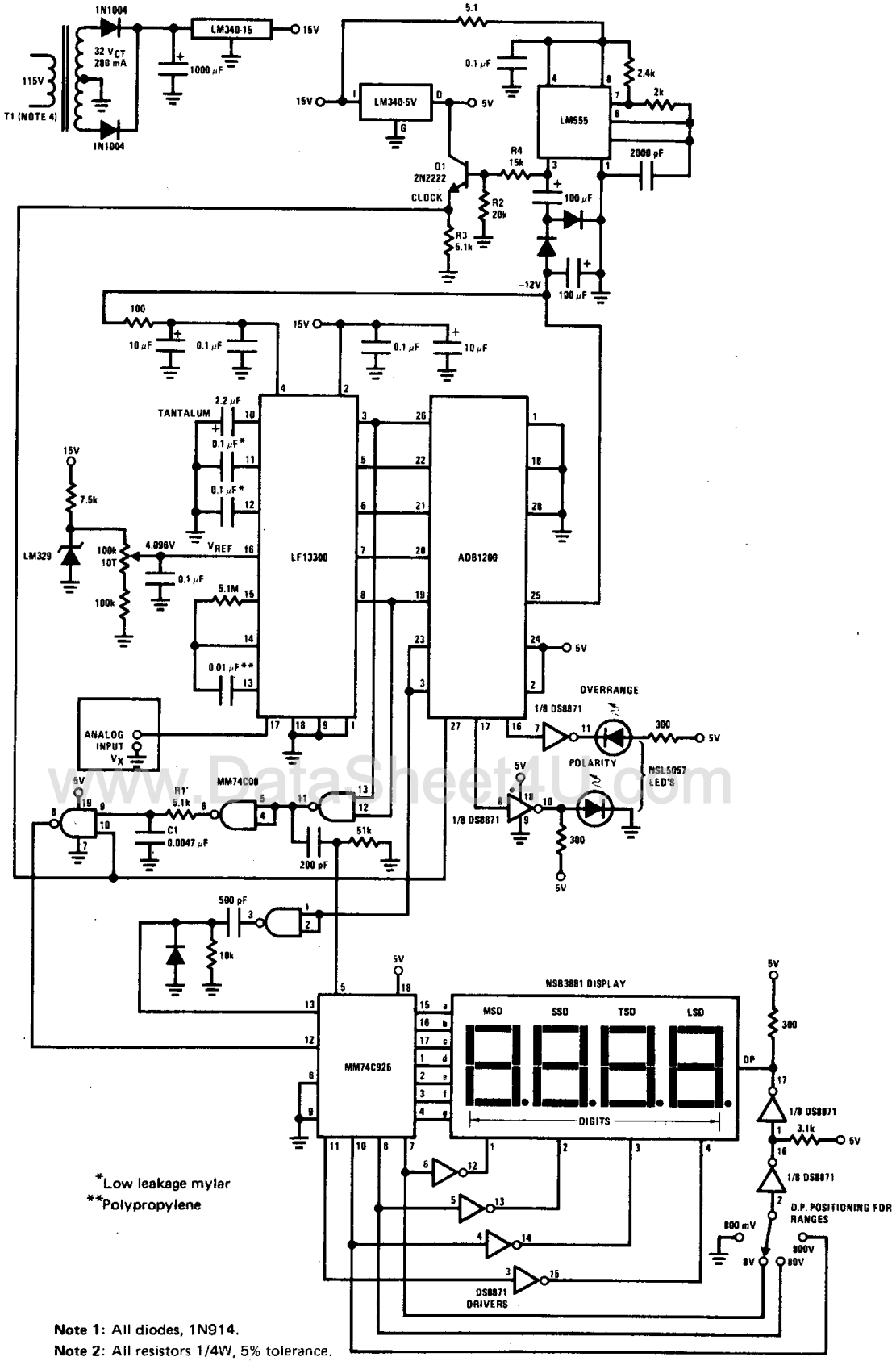


FIGURE 13. Timing Diagram for *Figure 12*

Typical Applications (Continued)



*Low leakage mylar
**Polypropylene

Note 1: All diodes, 1N914.
Note 2: All resistors 1/4W, 5% tolerance.
Note 3: Circuit drawn for 8V full scale operation input scaling not shown.
Note 4: Inductive components U4X003 or Microtran PC6714.

FIGURE 14. 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM Schematic Diagram

Typical Applications (Continued)

3 3/4 Plus Digit (±8191 Counts)/3 1/2-Digit (±1999 Counts) DPM

In this circuit of *Figure 14*, the LF13300 and ADB1200 interact as previously described. The CMOS counter (MM74C926, MM74C928) is connected to count clock pulses during the ramp reference cycle. The counts are latched into the display when the comparator output trips, (goes low), as shown in the timing diagram *Figure 15*.

The RC network consisting of R1 and C1 is a low pass filter that prohibits the fast transients that occur on the comparator output during Offset Correction from loading any erroneous counts into the counter.

The DPM is able to operate from a single 15V power supply with the aid of a dc-dc converter. The LM555 generates the negative voltages required in the circuit and also doubles as the clock. The combination of Q1, R2, R3 and R4 forms a level shift to convert the output swing of the LM555 to a 0V–5V swing that is compatible with the logic. The LM340–5 drops the incoming 15V to 5V for use by the logic circuits and the LED display.

This circuit can be a 3 3/4 plus digit DPM if the MM74C926 is used or a 3 1/2-digit DPM if the MM74C928 is used. These counters are pin compatible and physically interchangeable.

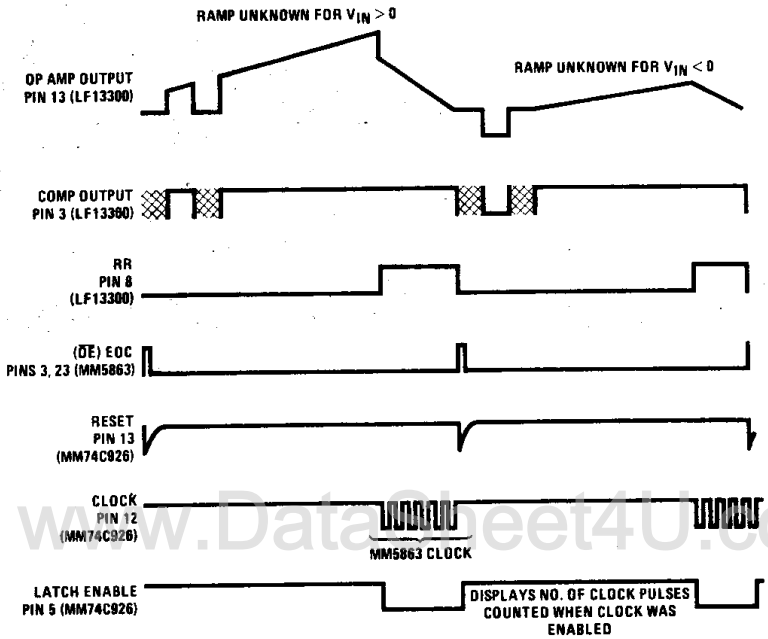


FIGURE 15. Timing Diagram for 3 3/4-Digit DVM

3 3/4-Digit DPM Electrical Characteristics

3 3/4 plus digits plus sign (±8191 counts) DPM system characteristics.
(Circuit as in *Figure 14*, V_S = ±15V, V_R = 4.096V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	$-8.2V \leq V_X \leq +8.2V$	16,382			Counts
Nonlinearity	V_{IN} = 4.000V		±1/8	±1/2	Counts
Ratiometric Gain Error	V_{IN} = 4.000V		±1/2	±2	Counts
Gain Error Drift	V_{IN} = 4.000V, $0°C \leq T_A \leq +70°C$		±1		ppm/°C
Zero Reading Drift	V_{IN} = 0V		±1		ppm/°C
Analog Input Voltage Range				±11	V
Reference Input Voltage Range	Reference Varied	0		+12	V
Analog Input Leakage Current	V_{IN} = 0V		80	500	pA
Reference Input Leakage Current			1	100	nA
Analog Input Resistance	V_{IN} = 0V		1000		MΩ
Conversion Time	V_{IN} = 4.000V, f_C = 125 kHz			74	ms

Typical Applications (Continued)

Component Side Foil

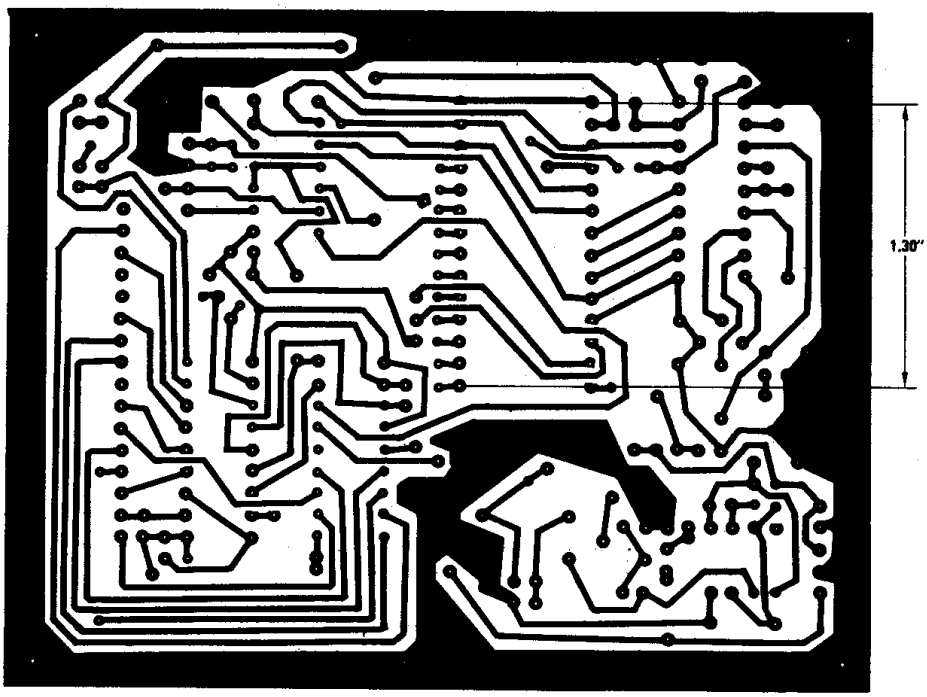


FIGURE 16. PC Board for 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM

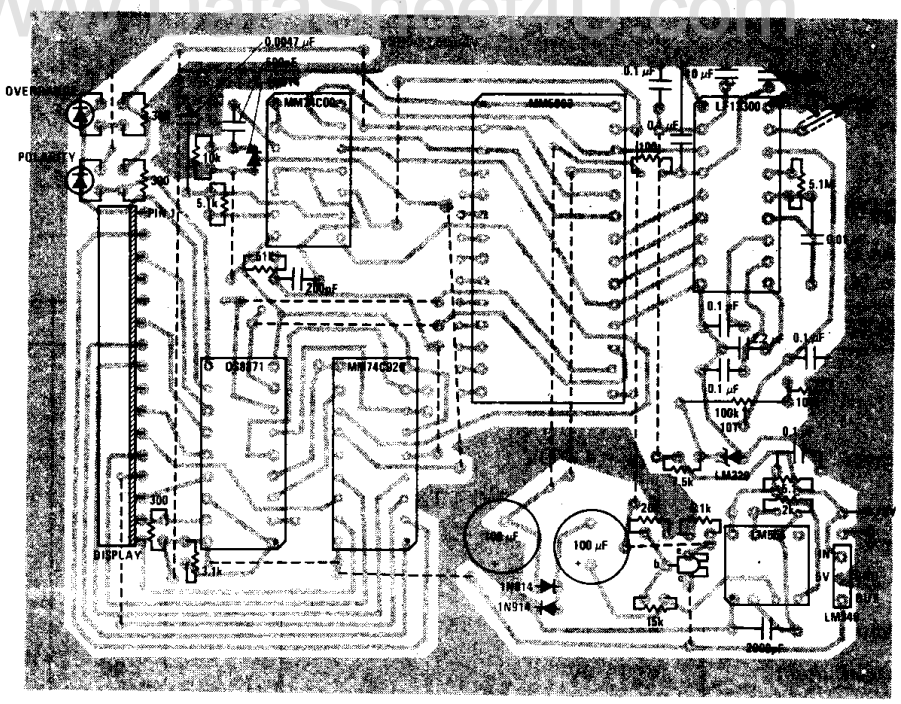
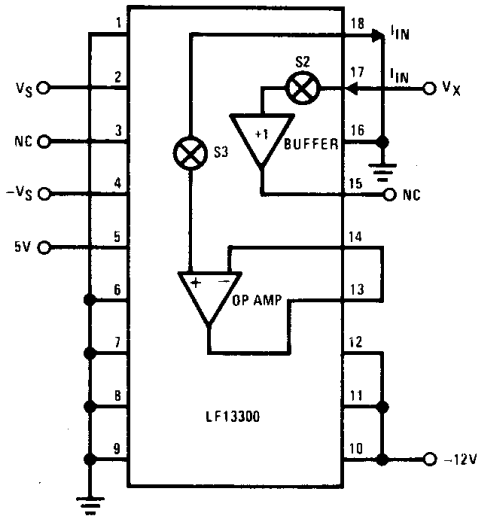


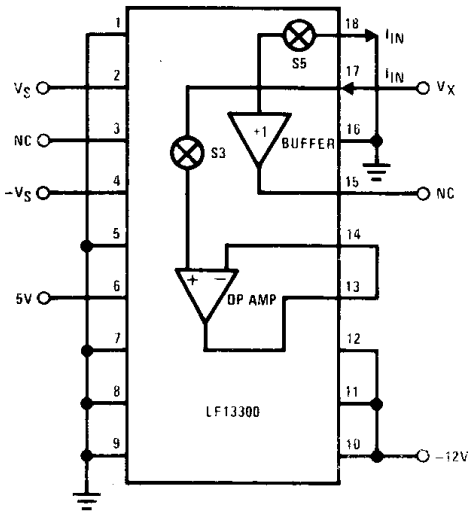
FIGURE 17. Stuffing Diagram for 3 3/4 Plus (±8191 Counts) and 3 1/2-Digit DPM

AC Test Circuits

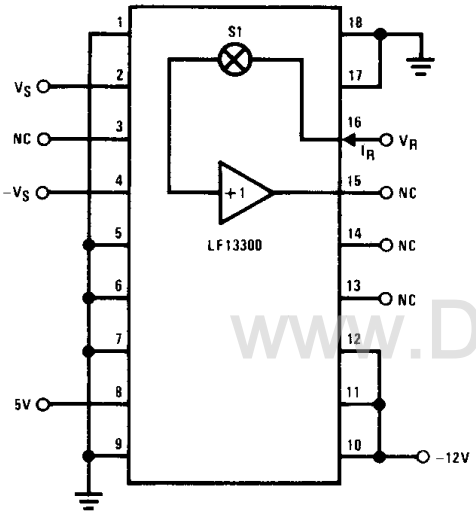
Test Circuit 1
Analog Input Characteristics Test with RU – High



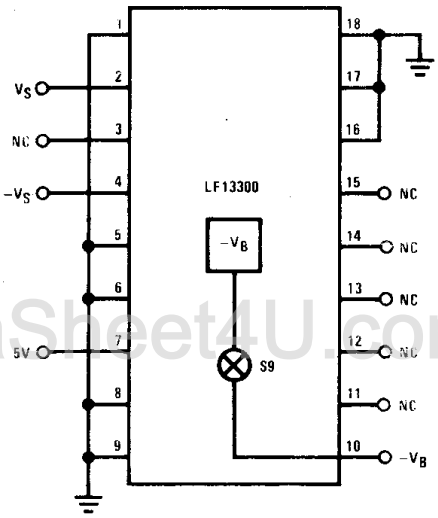
Test Circuit 2
Analog Input Characteristics Test with PD/RU+ High



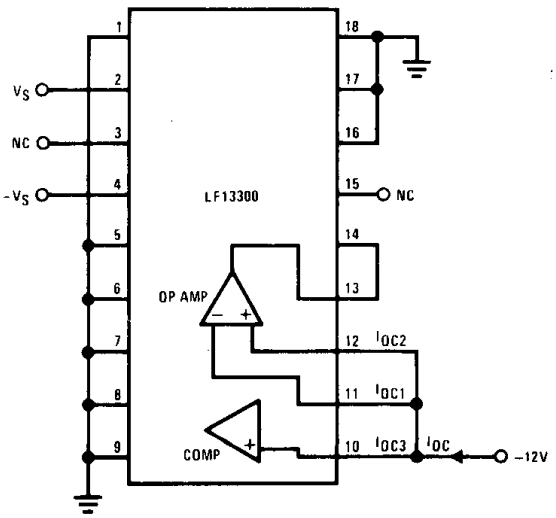
Test Circuit 3
Reference Input Characteristic Test with RR High



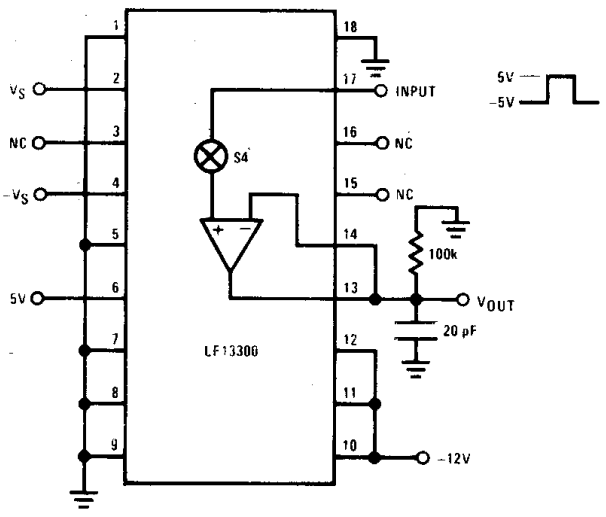
Test Circuit 4
–VB Voltage Measurement Test



Test Circuit 5
Offset Correction Input Current, I_{OC} Test

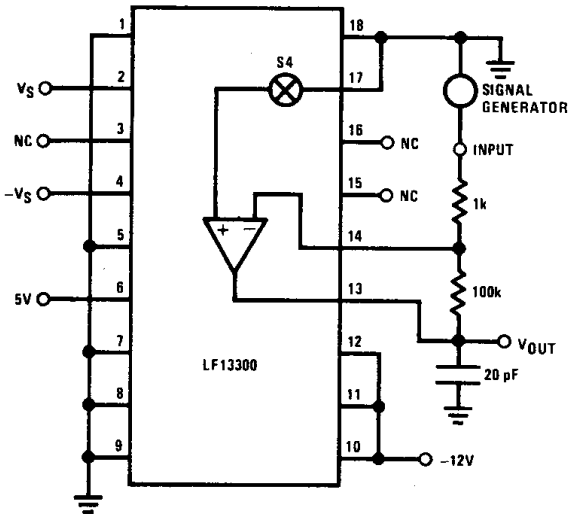


Test Circuit 6
Op Amp Slew Rate Test

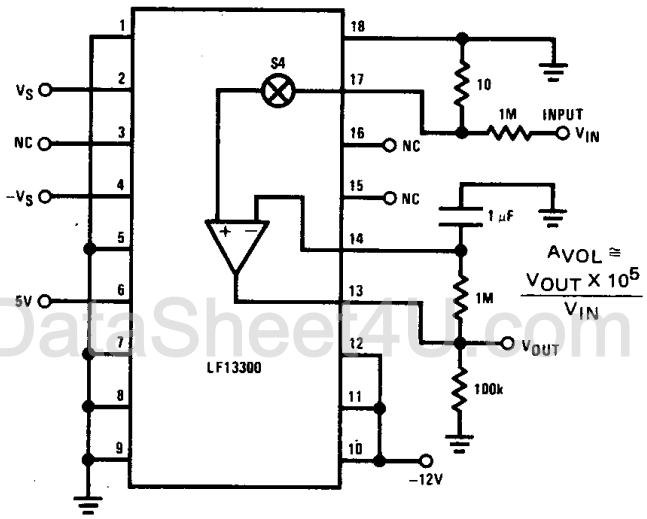


AC Test Circuits (Continued)

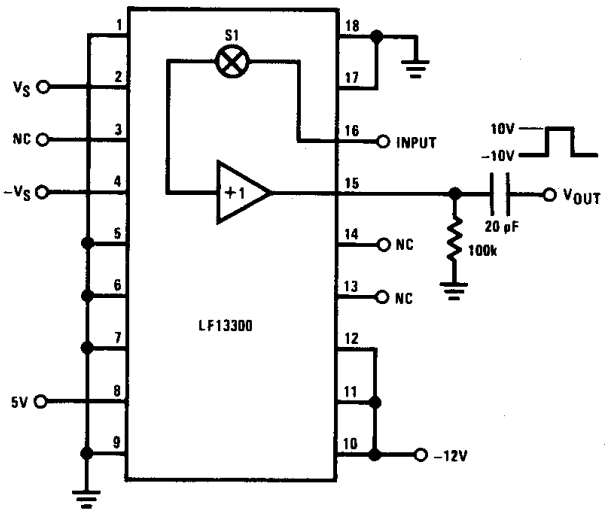
Test Circuit 7
Frequency Response Test



Test Circuit 8
Open Loop Gain Test

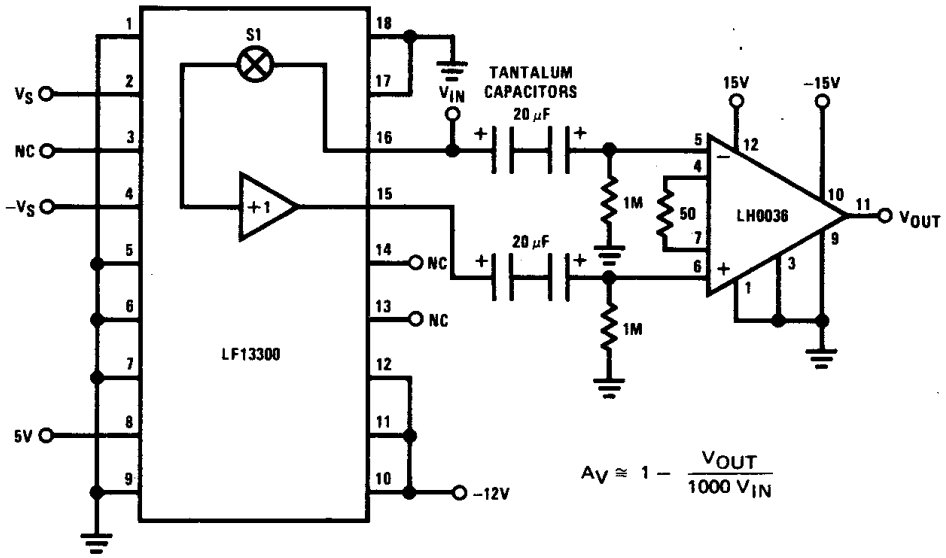


Test Circuit 9
Buffer Slew Rate Test

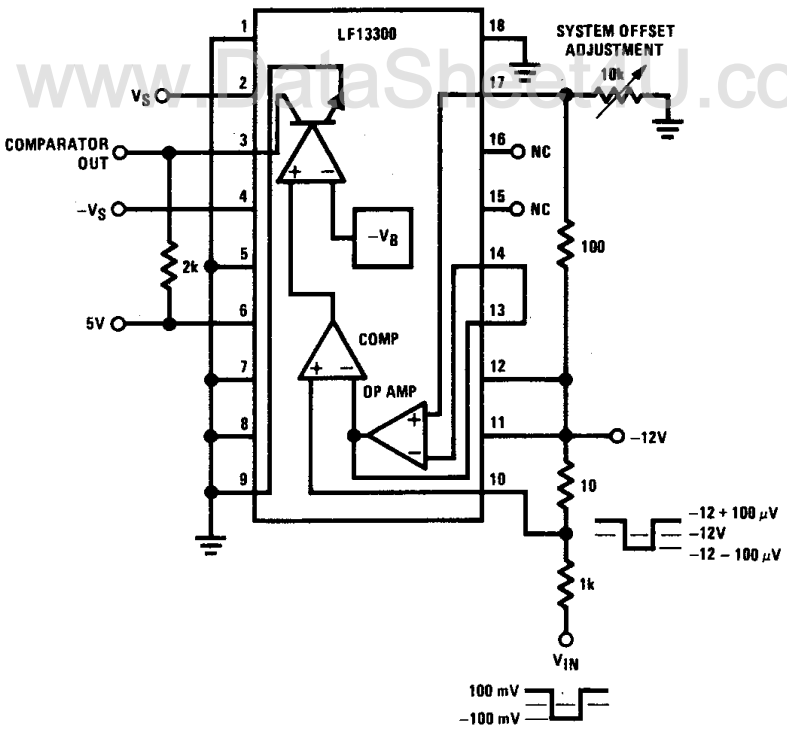


AC Test Circuits (Continued)

Test Circuit 10
Buffer Voltage Gain Test



Test Circuit 11
Comparator Response Time Test



Typical Applications (Continued)

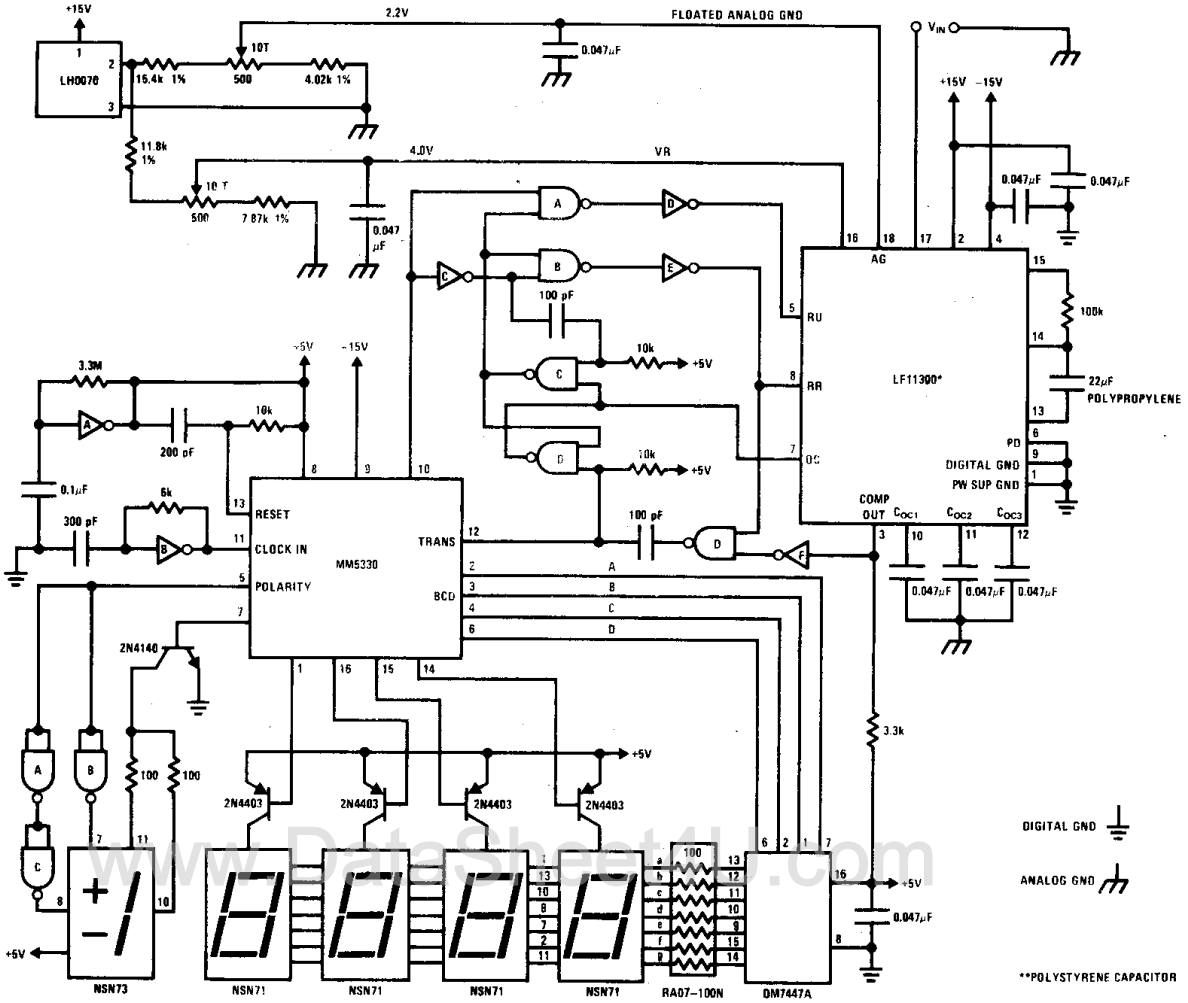


FIGURE 18. LF11300, MM5330 DPM Application