LF147QML Wide Bandwidth Quad JFET Input Operational Amplifier

Check for Samples: LF147QML

FEATURES

- **Internally Trimmed Offset Voltage: 5 mV Max**
- **Low Input Bias Current: 50 pA Typ.**
- **Low Input Noise Current: 0.01 pA/√Hz Typ.**
- **Wide Gain Bandwidth: 4 MHz Typ.**
- **High Slew Rate: 13 V/µs Typ.**
- **Low Supply Current: 7.2 mA Typ.**
- **High Input Impedance: $10^{12}\Omega$ Typ.**
- **Low Total Harmonic Distortion:**
  - **A_V = 10, R_L = 10KΩ, V_O = $20V_{P-P}$**
  - **BW = 20Hz – 20KHz ≤0.02% Typ.**
- **Low 1/f Noise Corner: 50 Hz Typ.**
- **Fast Settling Time to 0.01%: 2 µs Typ.**

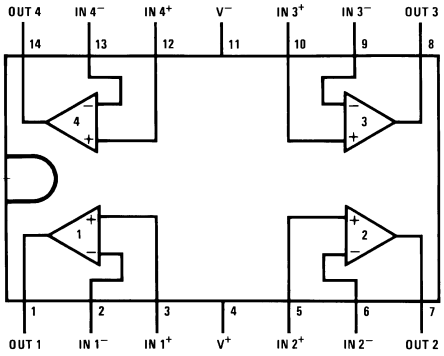
DESCRIPTION

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

CONNECTION DIAGRAM

Dual-In-Line Package (CDIP)
Top View



See Package Number J0014A

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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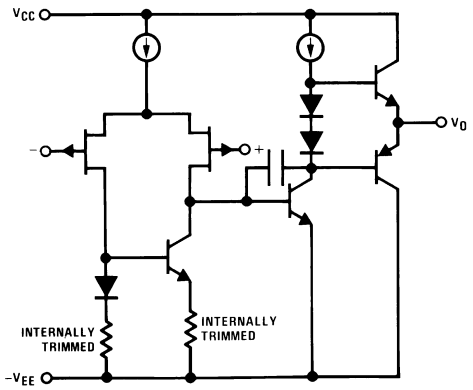
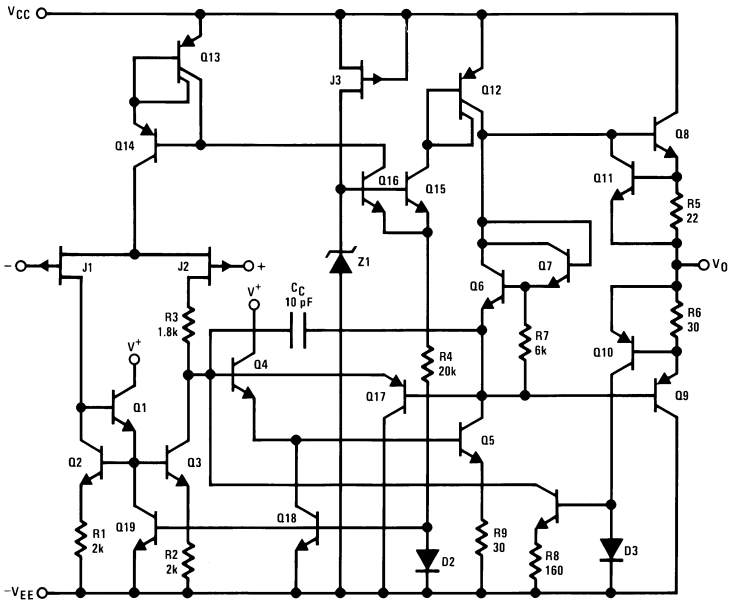
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Simplified Schematic

Figure 1. ¼ Quad



Detailed Schematic



Absolute Maximum Ratings (1)

Supply Voltage	±22V
Differential Input Voltage	±38V
Input Voltage Range (2)	±19V
Output Short Circuit Duration (3)	Continuous
Power Dissipation (4) (5)	900 mW
T_J max	150°C
θ_{JA} CERDIP	70°C/W
Operating Temperature Range	−55°C ≤ T_A ≤ 125°C
Storage Temperature Range	−65°C ≤ T_A ≤ 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD (6)	900V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (Package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} — T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside specified limits.
(6) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

LF147 883 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified: V_S = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	R_S = 10KΩ			5	mV	1
					8	mV	2, 3
I_{IO}	Input Offset Current	R_L = 10KΩ			0.1	nA	1
					25	nA	2, 3
$±I_{IB}$	Input Bias Current	R_L =10KΩ		-0.2	0.2	nA	1
				-50	50	nA	2, 3
V_{CM}	Input Common Mode Voltage Range		(1)	-16	16	V	1, 2, 3
CMRR	Common Mode Rejection Ratio	R_S ≤ 10KΩ, V_{CM} = ±16V		80		dB	1, 2, 3
PSRR	Power Supply Rejection Ratio	V_S = ±20V to V_S = ±5V		80		dB	1, 2, 3
I_S	Supply Current				11	mA	1, 2, 3
I_{OS}	Output Short Circuit	V_S = ±15V, V_I = +1V, Output short to GND		-57	-13	mA	1, 3
				-40	-6	mA	2
		V_S = ±15V, V_I = -1V, Output short to GND		13	57	mA	1, 3
				6	40	mA	2
A_{VS}	Large Signal Voltage Gain	V_S = ±15V, V_O = 0 to +10V, R_L = 2KΩ, R_S = 10KΩ	(2)	50		V/mV	4
			(2)	25		V/mV	5, 6
		V_S = ±15V, V_O = 0 to -10V R_L = 2 KΩ, R_S=10KΩ	(2)	50		V/mV	4
			(2)	25		V/mV	5, 6
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10KΩ, V_I = +1V		12		V	4, 5, 6
		V_S = ±15V, R_L = 10KΩ, V_I = -1V			-12	V	4, 5, 6
		V_S = ±15V, R_L = 2KΩ, V_I = +1V		10		V	4, 5, 6
		V_S = ±15V, R_L = 2KΩ, V_I = -1V			-10	V	4, 5, 6

(1) Specified by CMRR test
(2) V/mV in units column is equivalent to K in datalog

LF147 883 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified: V_S = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR	Slew Rate	V_I = -5V to +5V, A_V=1 R_L = 2KΩ, CL = 100pF		8		V/µs	7
				5		V/µs	8A, 8B
		V_I = +5V to -5V, A_V = 1 R_L = 2KΩ, CL = 100pF		8		V/µS	7
				5		V/µS	8A, 8B

LF147 SMD Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified: V_S = ±15V, V_{CM} = 0V, R_S = 0Ω, R_L = Open

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	Vcc = ±15V		-9	9	mV	1
				-15	15	mV	2, 3
		Vcc = ±9V		-9	9	mV	1
I_{IO}	Input Offset Current			-0.1	0.1	nA	1
				-20	20	nA	2
$±I_{IB}$	Input Bias Current			-0.2	0.2	nA	1
				-50	50	nA	2
A_{VS}	Large Signal Voltage Gain	V_S = ±15V, V_O = 0 to +10V, R_L = 2KΩ		35		V/mV	4
				15		V/mV	5, 6
		V_S = ±15V, V_O = 0 to -10V, R_L = 2KΩ		35		V/mV	4
				15		V/mV	5, 6
$+V_O$	Output Voltage Swing	V_S = ±15V, R_L = 10KΩ		12		V	4, 5, 6
		V_S = ±15V, R_L = 2KΩ		10		V	4, 5, 6
$-V_O$	Output Voltage Swing	V_S = ±15V, R_L = 10KΩ			-12	V	4, 5, 6
		V_S = ±15V, R_L = 2KΩ			-10	V	4, 5, 6
V_{CM}	Input Common Mode Voltage Range		(1)	±11		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V		80		dB	1
+PSRR	Power Supply Rejection Ratio	$+V_S$ = 15 to 9V, $-V_S$ = -15V		80		dB	1
-PSRR	Power Supply Rejection Ratio	$+V_S$ = 15V, $-V_S$ = -15 to -9V		80		dB	1
$+I_S$	Supply Current				14	mA	1
$-I_S$	Supply Current			-14		mA	1
$+I_{OS}$	Output Short Circuit Current	V_S = ±15V		-57	-13	mA	1, 3
				-40	-6	mA	2
$-I_{OS}$	Output Short Circuit Current	V_S = ±15V		13	57	mA	1, 3
				6	40	mA	2

(1) Specified by CMRR test

LF147 SMD Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified: V_S = ±15V, V_{CM} = 0V, R_S = 0Ω, R_L = Open

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR	Slew Rate	V_I = -5V to +5V, A_V=1 R_L = 2KΩ, C_L = 100pF		8		V/µs	7
				5		V/µs	8A, 8B
		V_I = +5V to -5V, A_V=1 R_L = 2KΩ, C_L = 100pF		8		V/µS	7
				5		V/µS	8A, 8B

Typical Performance Characteristics

Input Bias Current

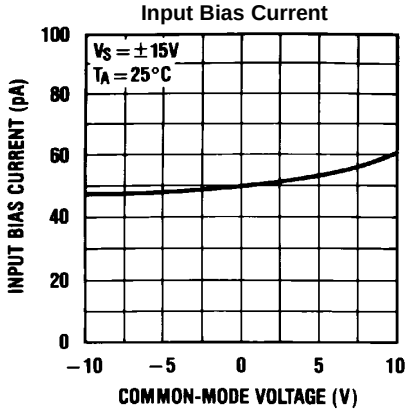


Figure 2.

Input Bias Current

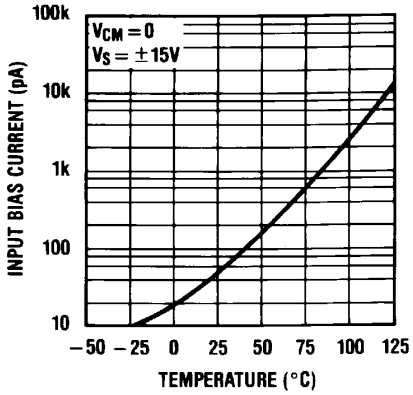


Figure 3.

Supply Current

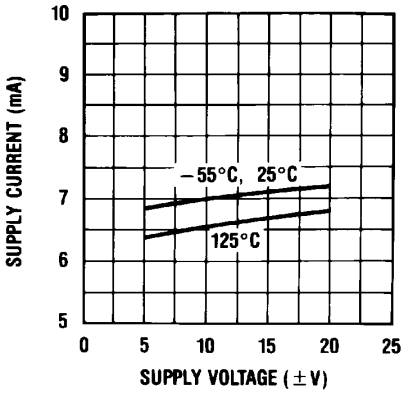


Figure 4.

Positive Common-Mode Input Voltage Limit

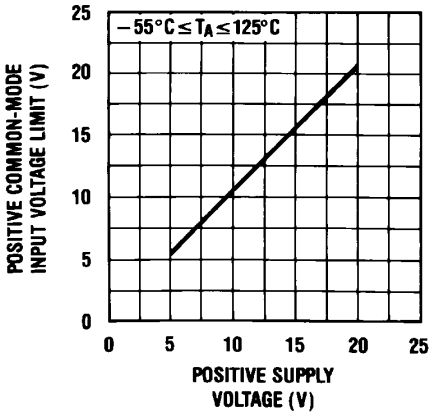


Figure 5.

Negative Common-Mode Input Voltage Limit

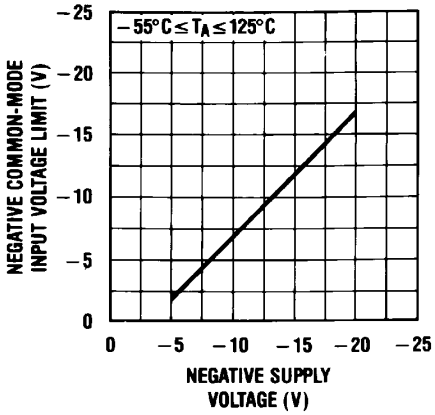


Figure 6.

Positive Current Limit

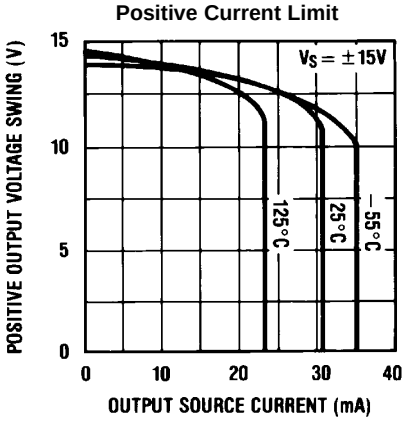


Figure 7.

Typical Performance Characteristics (continued)

Negative Current Limit

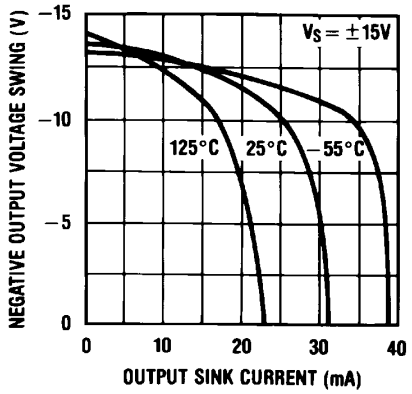


Figure 8.

Output Voltage Swing

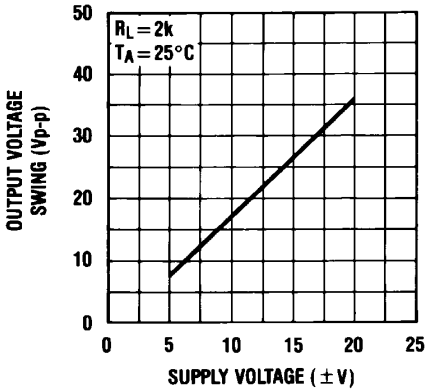


Figure 9.

Output Voltage Swing

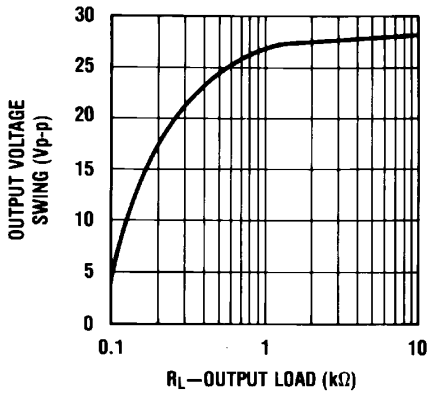


Figure 10.

Gain Bandwidth

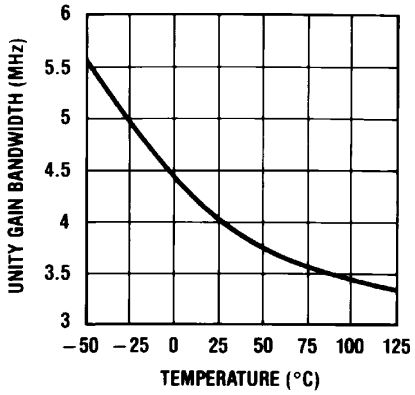


Figure 11.

Bode Plot

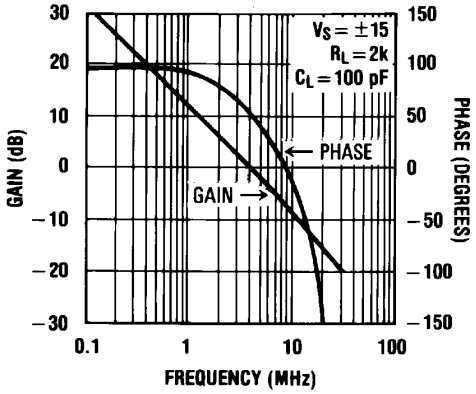


Figure 12.

Slew Rate

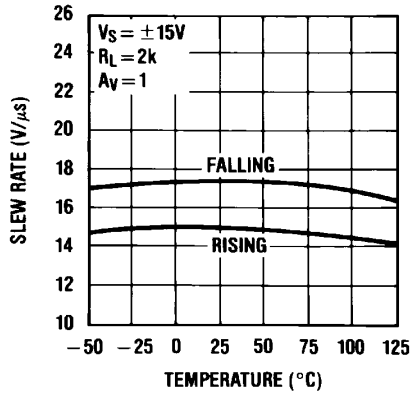


Figure 13.

Typical Performance Characteristics (continued)

Distortion vs Frequency

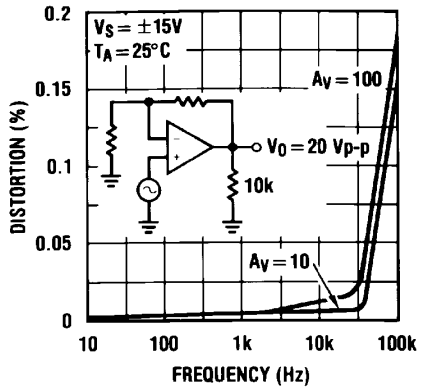


Figure 14.

Undistorted Output Voltage Swing

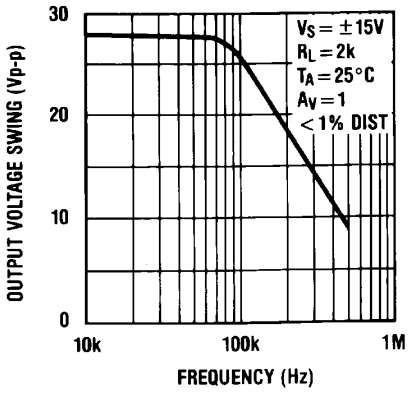


Figure 15.

Open Loop Frequency Response

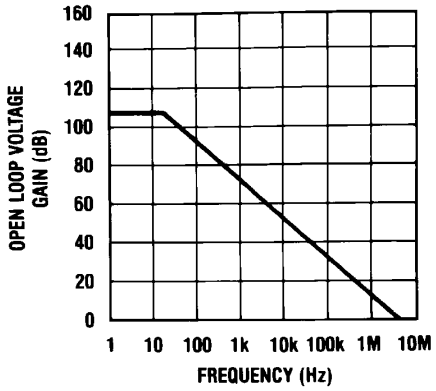


Figure 16.

Common-Mode Rejection Ratio

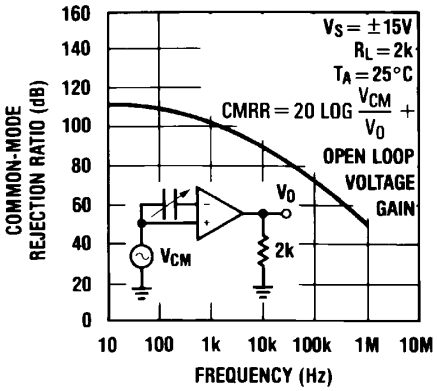


Figure 17.

Power Supply Rejection Ratio

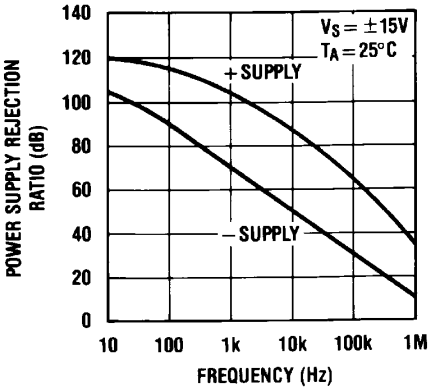


Figure 18.

Equivalent Input Noise Voltage

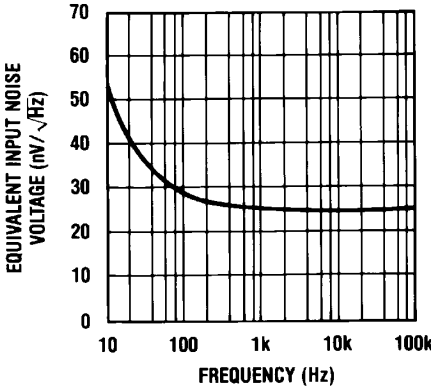


Figure 19.

Typical Performance Characteristics (continued)

Open Loop Voltage Gain

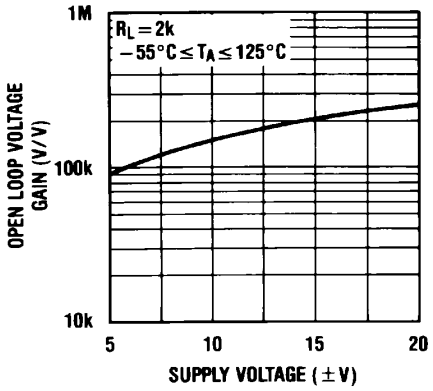


Figure 20.

Output Impedance

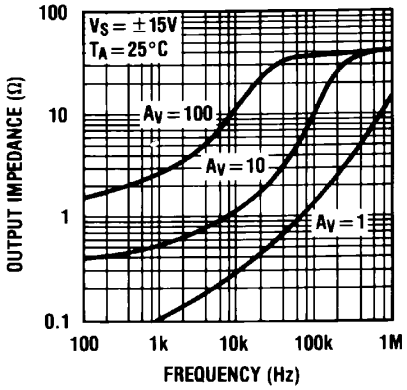


Figure 21.

Inverter Settling Time

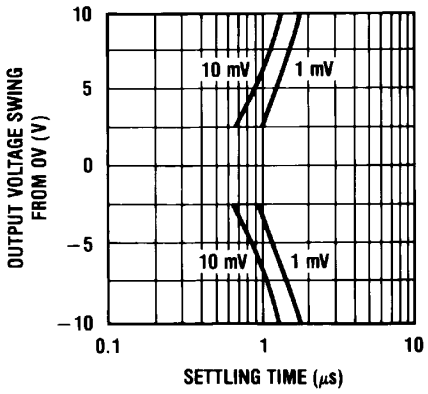
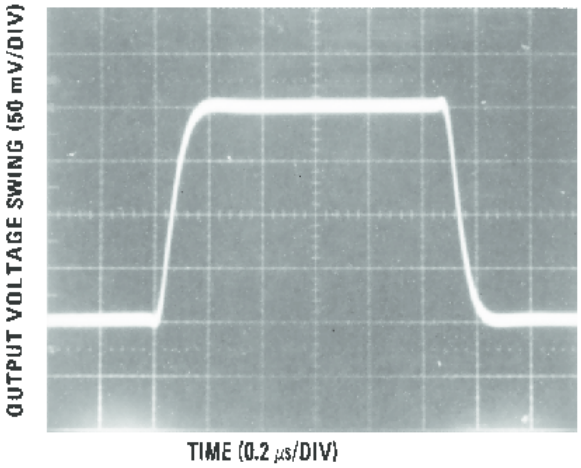


Figure 22.

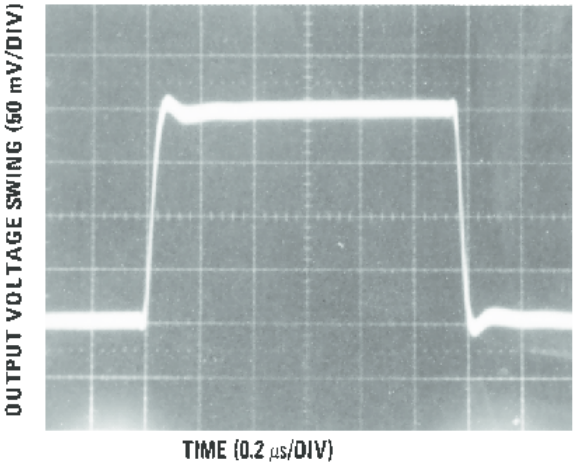
Pulse Response

R_L = 2 kΩ, C_L = 10 pF

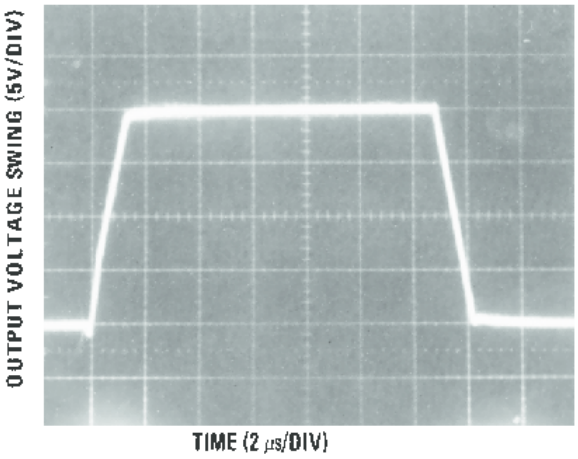
Small Signal Inverting



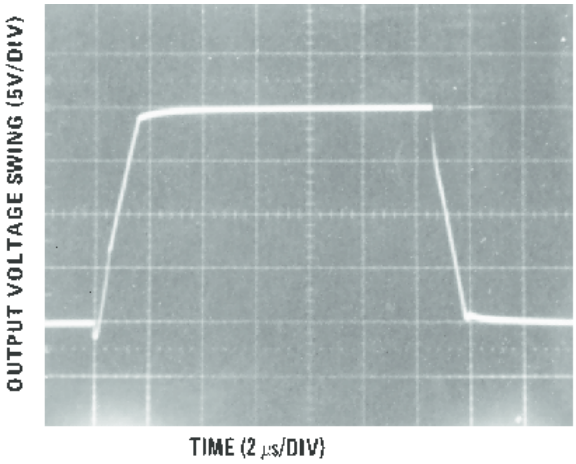
Small Signal Non-Inverting



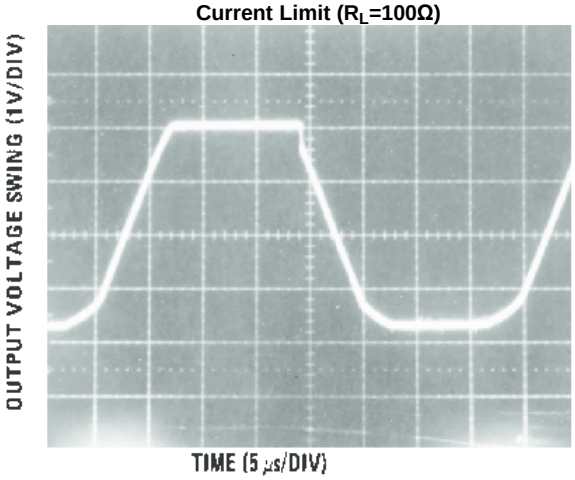
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L=100Ω)



APPLICATION INFORMATION

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

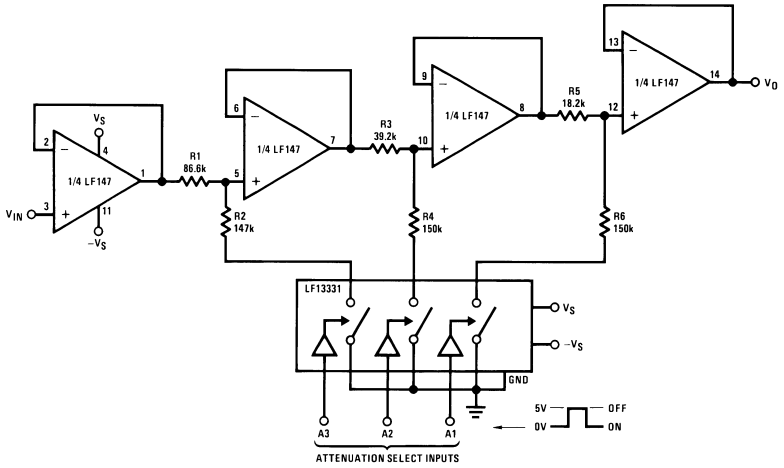
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Figure 23. Digitally Selectable Precision Attenuator

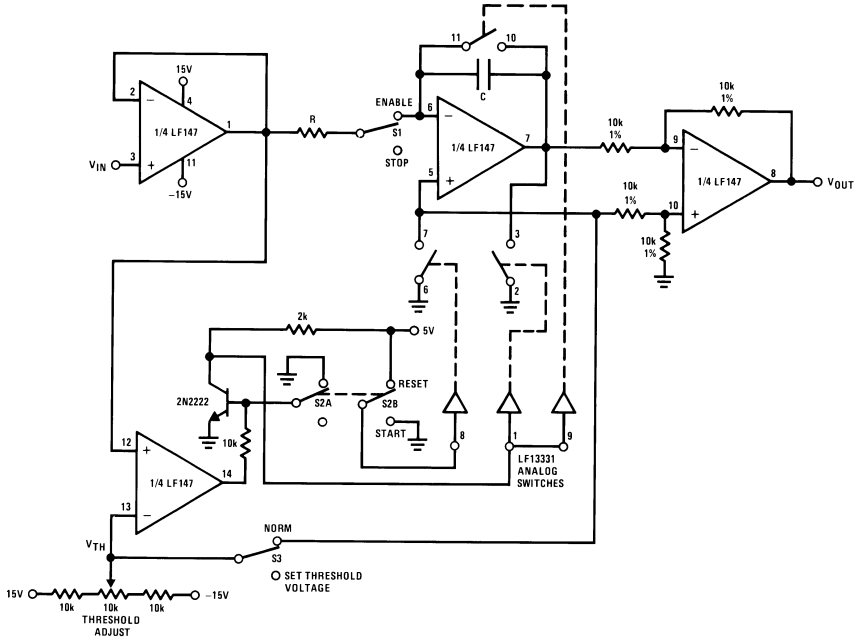


All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
  No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

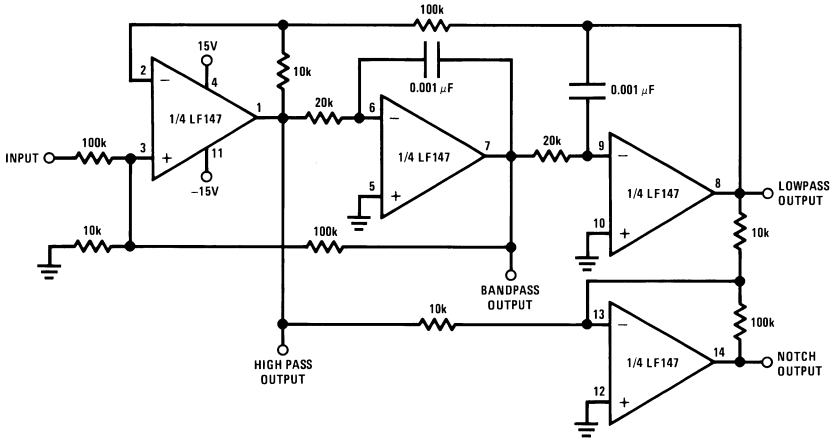
A1	A2	A3	V_O
			Attenuation
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

Figure 24. Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:
  $V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$
- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Figure 25. Universal State Variable Filter



For circuit shown: f_O= 3 kHz, f_{NOTCH}= 9.5 kHz
Q=3.4
Passband gain: Highpass—0.1
Bandpass—1
Lowpass—1
Notch—10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

Date Released	Revision	Section	Originator	Changes
04/18/05	A	New Release into corporate format	L. Lytle	2 MDS datasheets converted into one Corp. datasheet format. MNLF147–X Rev. 0A2 and MDLF147–X Rev. 0A1, data sheets will be Archived
03/20/13	A	All		Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LF147J/883	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	LF147J/883 Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

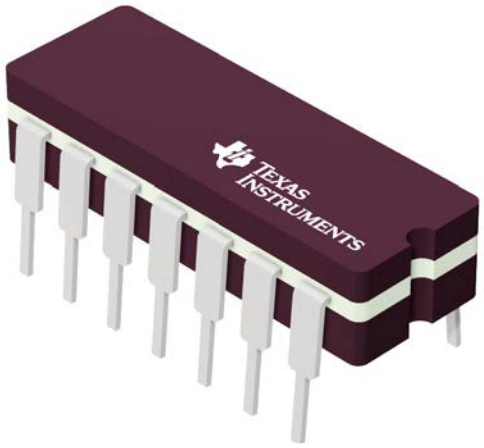
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

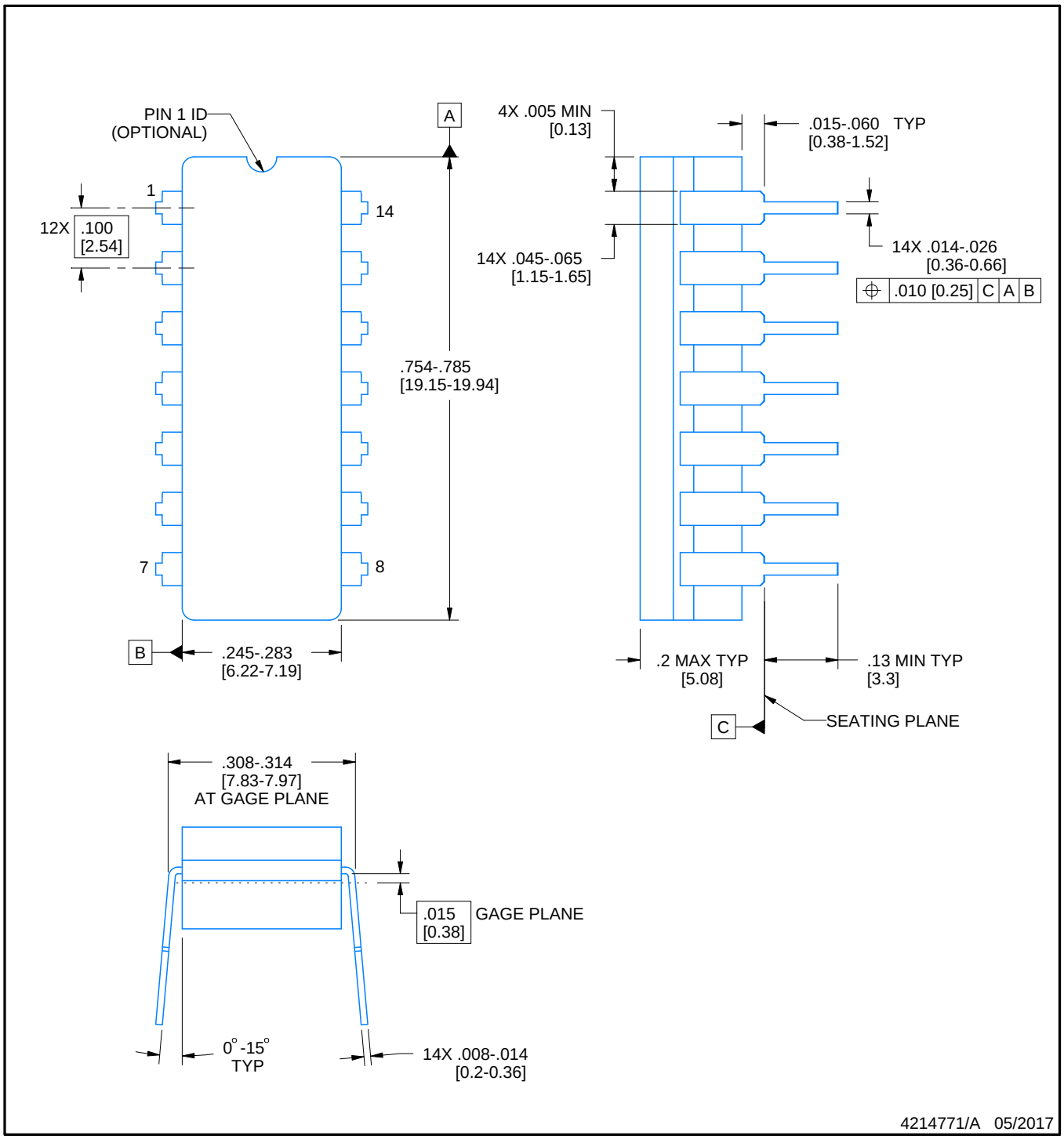
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

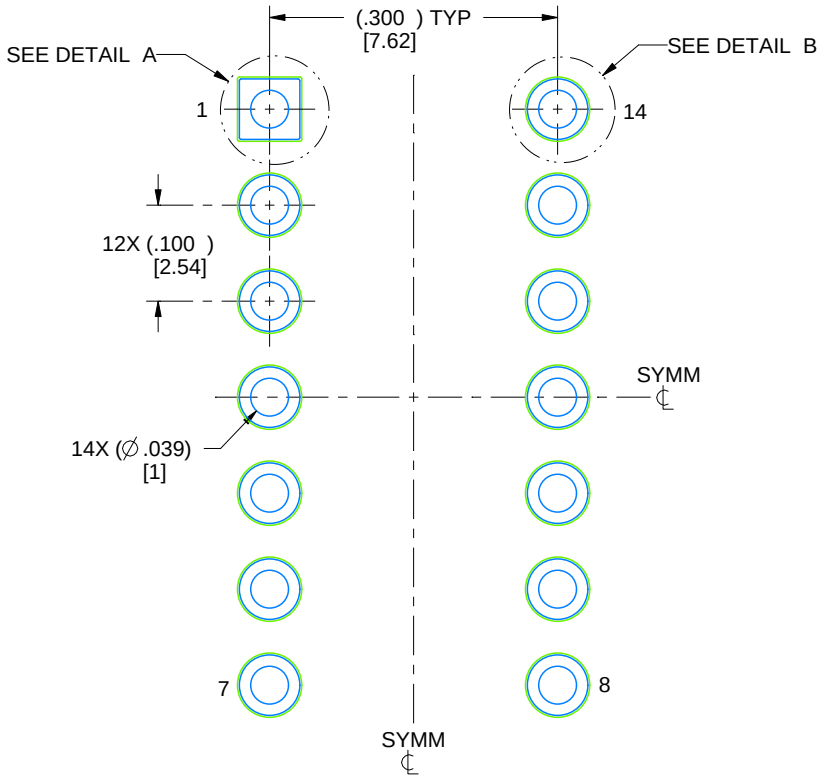
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

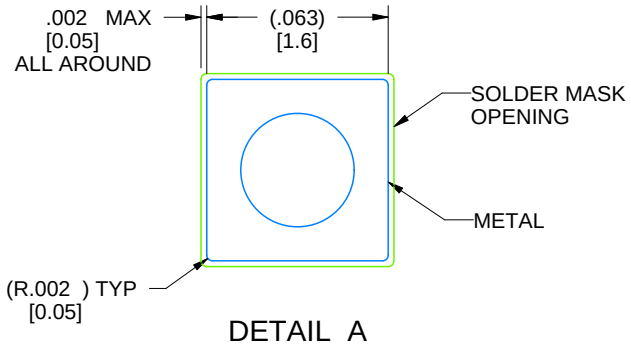
J0014A

CDIP - 5.08 mm max height

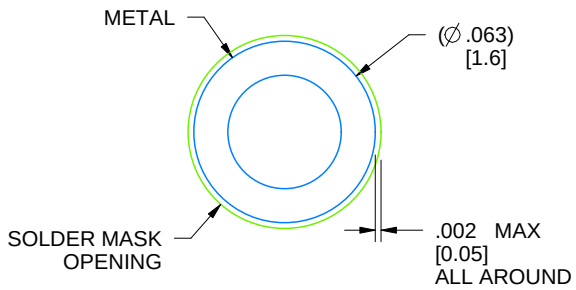
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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