Analog Switches

LF1650/LF2650/LF3650 quad JFET analog switch

general description

The LF1650/LF2650/LF3650 is a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad FET switch. A unique circuit technique is employed to maintain a constant R_{ON} over the analog voltage range. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break before make action.

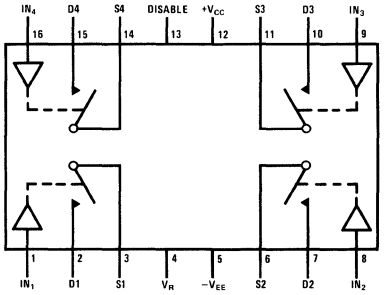
features

- Constant ON resistance for signals ±10V and 100 kHz
- $t_{OFF} < t_{ON}$, break before make action
- Open switch isolation at 1.0 MHz —50 dB
- < 1.0 nA leakage in OFF state
- TTL, DTL, RTL direct drive compatibility
- Single disable pin turns all switches in package OFF

The LF1650/LF2650/LF3650 is designed to operate from ±15V supplies and swing a ±10V analog signal. The FET switches can be used wherever a dc to medium frequency analog signal needs to be controlled.

connection diagram

Dual-In-Line Package
(Logic "0" In).



TOP VIEW

Order Number LF1650D, LF2650D or LF3650D
See Package 2

Order Number LF3650N
See Package 23

typical circuit and schematic diagrams

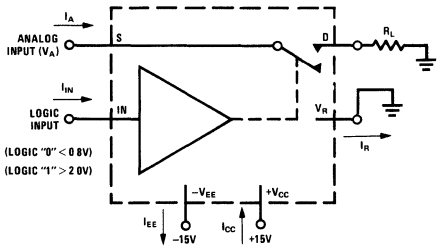


FIGURE 1.

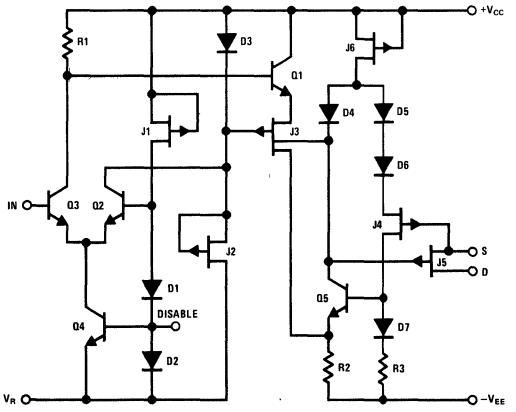


FIGURE 2.

absolute maximum ratings

Positive Supply – Negative Supply	36V
Positive Supply – Reference Supply	36V
Input Voltage	V_{CC} – 2.5V
Reference Voltage	V_{CC} – 5.0V ≥ V_R ≥ – V_{EE}
Input Voltage + Reference Voltage	–4.0V
Input Voltage – Reference Voltage	6.0V
Positive Analog Voltage	V_{CC}
Negative Analog Voltage	V_{EE}
Analog Current	$\|I_A\|$ < 20 mA
Power Dissipation (Note 1)	
Molded DIP (LF3650N)	570 mW
Cavity DIP (LF1650D, LF2650D, LF3650D)	800 mW
Operating Temperature Range	
LF1650	–55°C to +125°C
LF2650	–25°C to +85°C
LF3650	0°C to +70°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics ($+V_{CC}$ = 15V, $-V_{EE}$ = –15V, T_A = 25°C, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ON Resistance (R_{ON})	V_A = 0V, I_D = 1.0 mA		150		Ω
Maximum Analog Swing (V_{AMAX}) (Figure 1)			+11 –12		V V
Analog Current Loss ($I_{S(ON)}$ + $I_{D(ON)}$)	Switch ON, Source and Drain Connect to +10V		0.3		nA
Source Current OFF ($I_{S(OFF)}$)	Switch OFF, Source at +10V, Drain at –10V		0.4		nA
Drain Current OFF ($I_{D(OFF)}$)	Switch OFF, Source at +10V, Drain at –10V		0.1		nA
Logic Input Bias Current (I_{INH})	V_{IN} at +5.0V		3.6		μA
Delay Time ON (t_{ON}) (Figures 3 and 4)	Source at –10V		500		ns
Delay Time OFF (t_{OFF}) (Figures 3 and 4)	Source at +10V		90		ns
Source Capacitance ($C_{S(OFF)}$)	Switch OFF Source at –10V		4.0		pF
Drain Capacitance ($C_{D(OFF)}$)	Switch OFF Drain at –10V		3.0		pF
Active Source and Drain Capacitance ($C_{S(ON)}$ and $C_{D(ON)}$)	Switch ON Source and Drain at 0V		5.0		pF
OFF Isolation	Switch OFF, 1 0 MHz Signal on Source (Figure 5)		–50		dB
Crosstalk	One Switch OFF Another Switch ON with 1.0 Vrms @ 1.0 MHz at Source (Figure 5)		–65		dB
Positive Supply Current (I_{CC})	All Switches OFF		5.0		mA
Negative Supply Current (I_{EE})	All Switches OFF		–3.0		mA
Reference Supply Current (I_R)	All Switches OFF		–2.0		mA
V_{IN} Logic "0"				0.8	V
V_{IN} Logic "1"		2.0			V
Signal Path Slew Rate			50		V/μs

Note 1: For operating at high temperatures the molded DIP products must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at +100°C/W.

est circuits

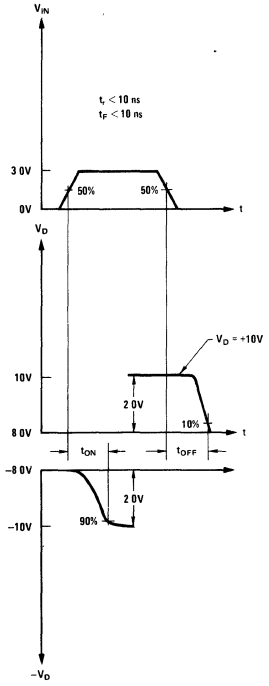


FIGURE 3. t_{ON}, t_{OFF}, Test

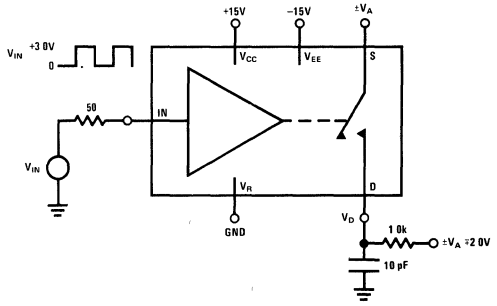


FIGURE 4. t_{ON}, t_{OFF} Test Circuit

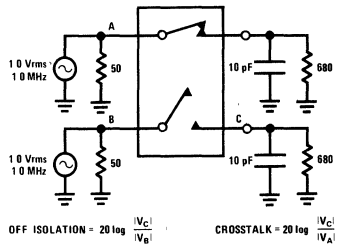
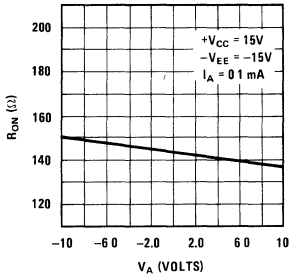


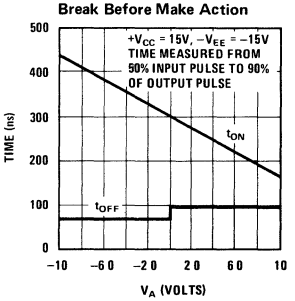
FIGURE 5. OFF Isolation and Crosstalk

ypical performance characteristics

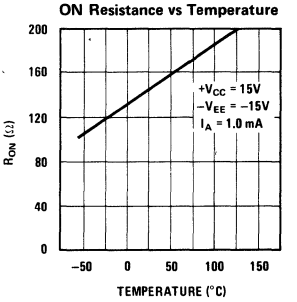
ON Resistance vs Analog Voltage



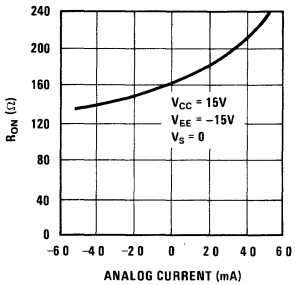
Break Before Make Action



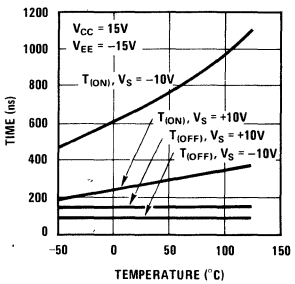
ON Resistance vs Temperature



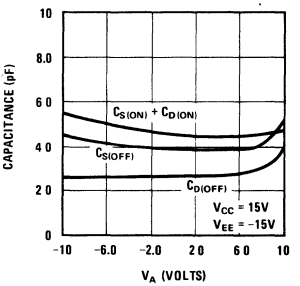
On Resistance vs Analog Current



Switching Times vs Temperature



Switch Capacitances vs Analog Voltage



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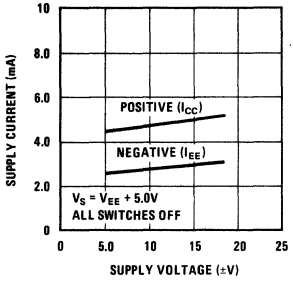
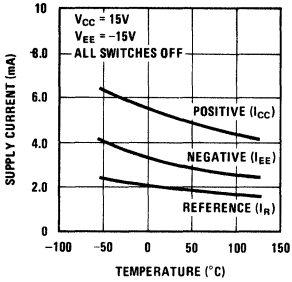
typical performance characteristics (con't)

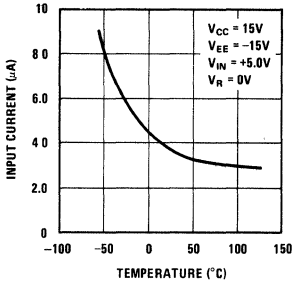
Supply Current vs Supply Voltage



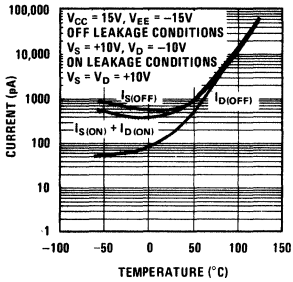
Supply Current vs Temperature



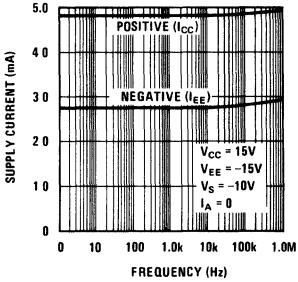
Logic "1" Input Bias Current vs Temperature



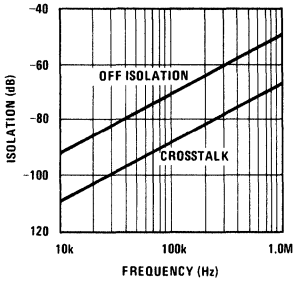
Switch Leakage Currents vs Temperature



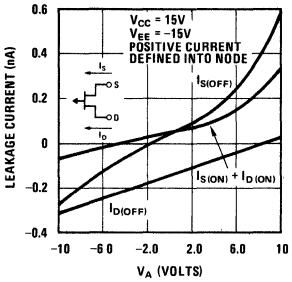
Supply Current vs Toggle Rate



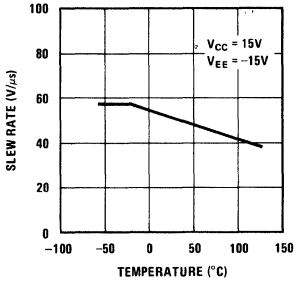
Crosstalk and OFF Isolation vs Frequency Using Test Circuit of Figure 5



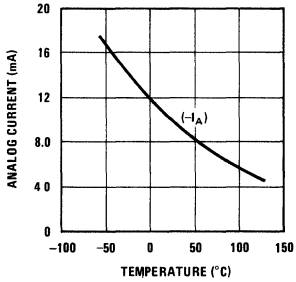
Leakage Currents vs Analog Voltage



Slew Rate of Analog Voltage Above Which Signal Loading Occurs



*See Note



***Note:** The above graph indicates the analog current at which 1% of the analog current is lost.

When the drain of the analog switch is positive with respect to the source the drain gate junction tends to forward bias and the output FET becomes a PNP transistor with base and substrate current losses. Operation in this mode allows much higher analog currents while maintaining a minimum R_{ON}.