LF3347
High-Speed Image Filter with Coefficient RAM

FEATURES

- 83 MHz Data Input and Computation Rate
- Four 12 x 12-bit Multipliers with Individual Data and Coefficient Inputs
- Four 256 x 12-bit Coefficient Banks
- 32-bit Accumulator
- Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- Two's Complement Operands
- 3.3 Volt Power Supply
- 5 Volt Tolerant I/O
- 120-pin PQFP

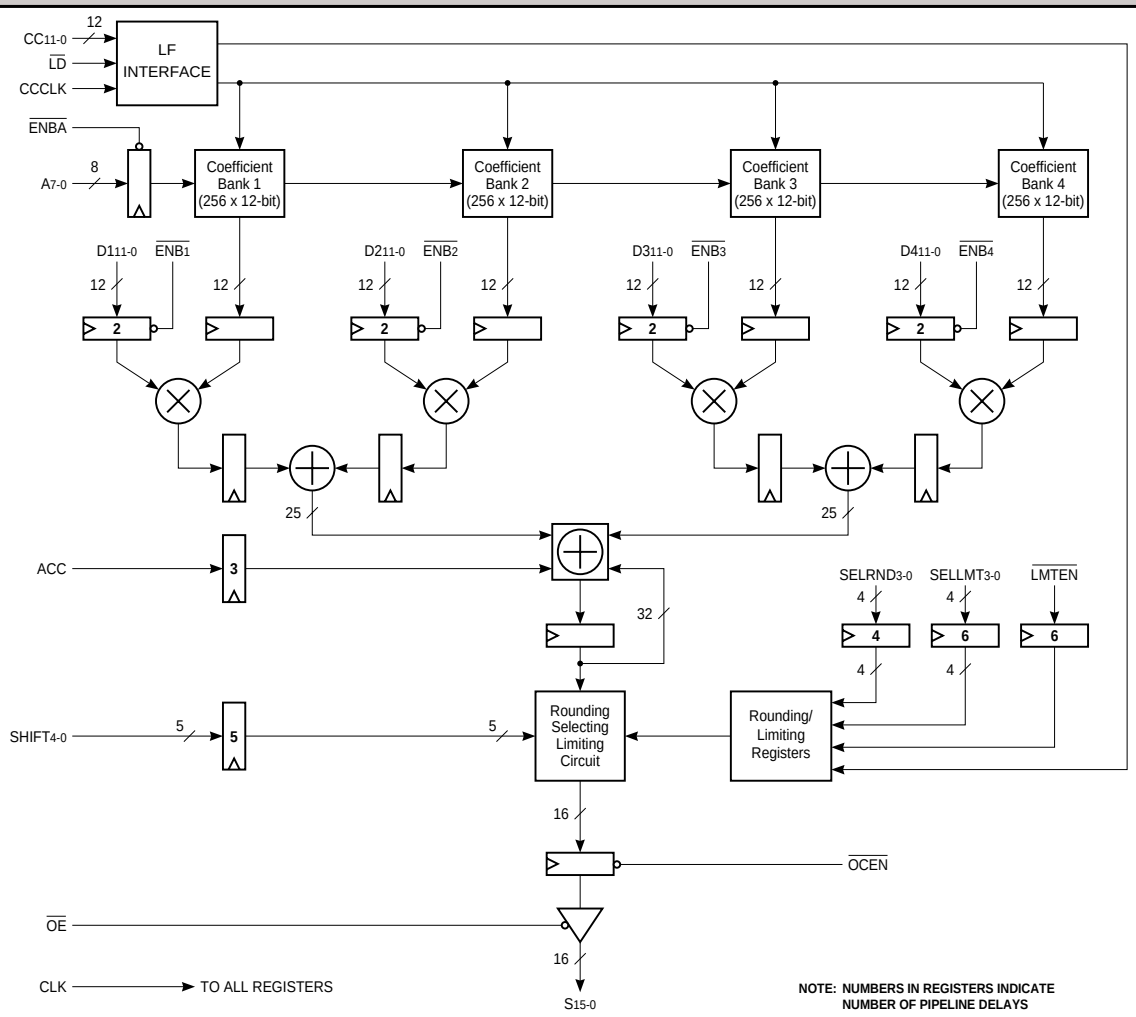
DESCRIPTION

The **LF3347** consists of an array of four 12 x 12-bit registered multipliers followed by two summers and a 32-bit accumulator. The LF3347 provides four 256 x 12-bit coefficient banks which are capable of storing 256 different sets of filter coefficients for the multiplier array. All multiplier data inputs are user accessible and can be updated every clock cycle with two's complement data. The pipelined architecture has fully registered input and output ports and an asynchronous three-state output enable control to simplify the design of complex systems.

A 32-bit accumulator allows cumulative word growth which may be internally rounded to 16-bits. Output data is updated every clock cycle and may be held under user control. The data inputs/outputs and control inputs are registered on the rising edge of CLK. The Control/Coefficient Data Input, *CC11-0*, is registered on the rising edge of CCCLK.

The LF3347 is ideal for performing pixel interpolation in image manipulation and filtering applications. The LF3347 can perform a bilinear interpolation of an image (4-pixel kernels) at real-time video rates when used

LF3347 BLOCK DIAGRAM



with an image resampling sequencer. Larger kernels or more complex functions can be realized by utilizing multiple devices.

Unrestricted access to all data ports and addressable coefficient banks provides the LF3347 with considerable flexibility in applications such as digital filters, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

SIGNAL DEFINITIONS

Power

V_{CC} and GND

+3.3 V power supply. All pins must be connected.

Clocks

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

CCCLK — Coefficient/Control Clock

When $\overline{LD}$ is LOW, the rising edge of CCCLK latches data on $CC_{11\text{-}0}$ into the device.

Inputs

$D1_{11\text{-}0}$ – $D4_{11\text{-}0}$ — Data Input

D1–D4 are the 12-bit registered data input ports. Data is latched on the rising edge of CLK.

$A_{7\text{-}0}$ — Row Address

$A_{7\text{-}0}$ determines which row in the coefficient banks feed data to the multipliers. $A_{7\text{-}0}$ is latched on the rising edge of CLK. When a new row address is loaded into the row address register, data from the coefficient banks will be latched into the multiplier input registers on the next rising edge of CLK.

FIGURE 1. INPUT FORMATS

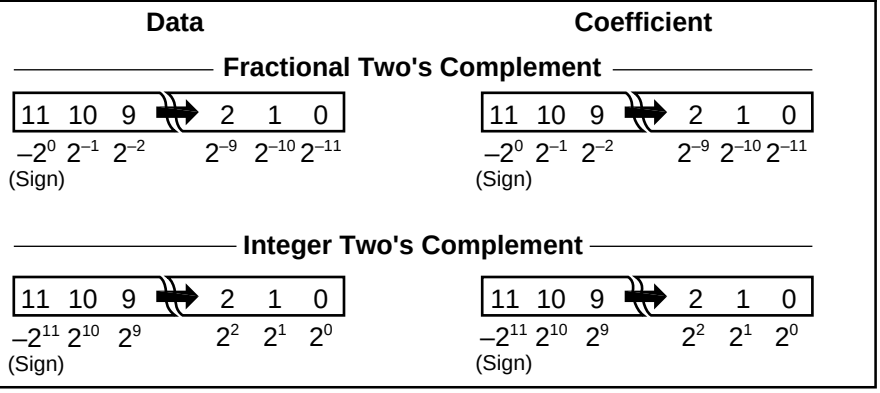


TABLE 1. OUTPUT FORMATS

SHIFT4-0	S15	S14	S13	· · ·	S8	S7	· · ·	S2	S1	S0
00000	F15	F14	F13	· · ·	F8	F7	· · ·	F2	F1	F0
00001	F16	F15	F14	· · ·	F9	F8	· · ·	F3	F2	F1
00010	F17	F16	F15	· · ·	F10	F9	· · ·	F4	F3	F2
·	·	·	·		·	·		·	·	·
·	·	·	·		·	·		·	·	·
·	·	·	·		·	·		·	·	·
01110	F29	F28	F27	· · ·	F22	F21	· · ·	F16	F15	F14
01111	F30	F29	F28	· · ·	F23	F22	· · ·	F17	F16	F15
10000	F31	F30	F29	· · ·	F24	F23	· · ·	F18	F17	F16

$CC_{11\text{-}0}$ — Control/Coefficient Data Input

$CC_{11\text{-}0}$ is used to load data into the coefficient banks and control registers. Data present on *$CC_{11\text{-}0}$* is latched on the rising edge of CCCLK when $\overline{LD}$ is LOW.

Outputs

$S_{15\text{-}0}$ — Data Output

$S_{15\text{-}0}$ is the 16-bit registered data output port.

Controls

$\overline{ENB1}$–$\overline{ENB4}$ — Data Input Enables

The $\overline{ENB_N}$ (N = 1, 2, 3, or 4) inputs allow the D_N registers to be updated on each clock cycle. When $\overline{ENB_N}$ is LOW, data on $D_{N11\text{-}0}$ is latched into the D_N register on the rising edge of CLK. When $\overline{ENB_N}$ is HIGH, data on $D_{N11\text{-}0}$ is not latched into the D_N register and the register contents will not be changed.

$\overline{ENBA}$ — Row Address Input Enable

The $\overline{ENBA}$ input allows the row address register to be updated on each clock cycle. When $\overline{ENBA}$ is LOW, data on $A_{7\text{-}0}$ is latched into the row address register on the rising edge of CLK. When $\overline{ENBA}$ is HIGH, data on $A_{7\text{-}0}$ is not latched into the row address register and the register contents will not be changed.

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, $S_{15\text{-}0}$ is enabled for output. When $\overline{OE}$ is HIGH, $S_{15\text{-}0}$ is placed in a high-impedance state.

TABLE 2. REGISTER FORMATS

Register	Load Address	Bits	Register Description	A7-0	SELRND3-0	SELLMT3-0
CS0	000H	11-0	Coefficient Set 0	00H		
CS1	001H	11-0	Coefficient Set 1	01H		
:	:	:	:	:		
CS255	0FFH	11-0	Coefficient Set 255	FFH		
RND0	800H	31-0	Rounding Register 0		0 0 0 0	
RND1	801H	31-0	Rounding Register 1		0 0 0 1	
:	:	:	:		:	
RND15	80FH	31-0	Rounding Register 15		1 1 1 1	
LMT0	C00H	31-16/15-0	Upper / Lower Limit Register 0			0 0 0 0
LMT1	C01H	31-16/15-0	Upper / Lower Limit Register 0			0 0 0 1
:	:	:	:			:
LMT15	C0FH	31-16/15-0	Upper / Lower Limit Register 15			1 1 1 1

$\overline{OCEN}$ — Output Clock Enable

When $\overline{OCEN}$ is LOW, the output register is enabled for data loading. When $\overline{OCEN}$ is HIGH, output register loading is disabled and the register's contents will not change.

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. When ACC is HIGH, the emerging product is added to the sum of the previous products.

$\overline{LD}$ — Load Control

$\overline{LD}$ enables the loading of data into the coefficient banks and control registers (control registers are the round and limit registers). When $\overline{LD}$ is LOW, data on CC11-0 is latched into the device on the rising edge of CCCLK. When $\overline{LD}$ is HIGH, data cannot be loaded into the coefficient banks and control registers. When enabling the input circuitry for data loading, the LF3347 requires a HIGH to LOW transition of $\overline{LD}$ in order to function properly. Therefore, $\overline{LD}$ needs to be set HIGH immediately after power up to ensure proper operation of the input circuitry.

It takes five CCCLK clock cycles to load one coefficient set into the four coefficient banks or to load one control register. When the input circuitry is enabled ($\overline{LD}$ goes LOW), the first value loaded into the device on CC11-0 is an address which determines what will be loaded (see Table 2). The next four values loaded on CC11-0 is the data to be loaded into the coefficient banks or control register (see Tables 3-5). After the last data value is loaded, another coefficient bank address or control register may be loaded by feeding another address into CC11-0. When all desired coefficient banks and control registers are loaded, the input circuitry must be disabled by setting $\overline{LD}$ HIGH.

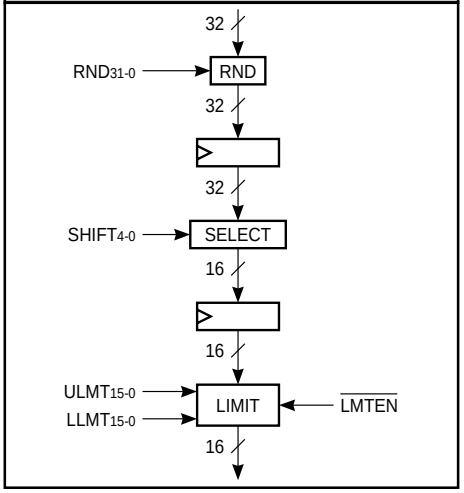
SELRND3-0 — Round Select

SELRND3-0 allows the user to select which rounding register will be used in the rounding circuit to round / offset the data.

SHIFT4-0 — Shift

SHIFT4-0 determines which 16-bits of the 32-bits from the accumulator are passed to the output (see Table 1).

FIGURE 2. ROUNDING, SELECTING, LIMITING CIRCUITRY



SELLMT3-0 — Limit Select

SELLMT3-0 allows the user to control which limiting register will be used in the limiting circuit to set the upper and lower limits on the data.

$\overline{LMTEN}$ — Limit Enable

When $\overline{LMTEN}$ is LOW, limiting is enabled and the selected limit register is used to determine the valid range of output values for the overall filter. When HIGH, limiting is disabled.

FUNCTIONAL DESCRIPTION

Coefficient Banks

The LF3347 has four coefficient banks which feed coefficient values to the multipliers. Each bank can store 256 12-bit coefficients. In the example shown in Table 3, address 10 in coefficient banks 1 through 4 is loaded with the following values: ABCH, 789H, 456H, 123H. The coefficient banks are not written to until all four coefficients have been loaded into the device.

A7-0 determines which coefficient set is sent to the multipliers. A value of 0 on A7-0 selects set 0. A value of 1 selects set 1 and so on.

Rounding/Offset

The accumulator output may be rounded before being sent to the output select section. Rounding is user-selectable and is accomplished by adding the contents of a round register to the accumulator output (see Figure 2). There are sixteen 32-bit round registers. In the example in Table 4, round register 10 is loaded with 76543210H. A round register is not written to until all four data values have been loaded into the device.

SELRND3-0 determines which round register is used for rounding. A value of 0 on SELRND3-0 selects round register 0. A value of 1 selects round register 1 and so on. If rounding is not desired, a round register should be loaded with 0 and selected as the register for rounding.

Output Select

The filter output word width is 32-bits. However, only 16-bits may be sent to the device output. SHIFT4-0 determines which 16 bits are passed to the device output (See Table 1).

Output Limiting

An output limiting function is provided for the output of the filter. When limiting is enabled (LMTEN LOW), the limit register selected with SELLMT3-0 determines the valid range of output values for the overall filter. There are sixteen 32-bit limit registers. Each limit register contains both an upper and lower limit value. The lower limit is stored in bits 15-0 and the upper limit is stored in bits 31-16. If the value fed to the limiting circuitry is less than the lower limit, the lower limit is passed to the device output. If the value fed to the limiting circuitry is greater than the upper limit, the upper limit is passed to the device output. When loading limit values into the device, the upper limit must be greater than the lower limit. In the example shown in Table 4, limit register 15 is loaded with a lower limit of 0123H and an upper limit of 7FEDH. A limit register is not written to until all four data values have been loaded into the device.

SELLMT3-0 determines which limit register is used for limiting. A value of 0 on SELLMT3-0 selects limit register 0. A value of 1 selects limit register 1 and so on.

TABLE 3. COEFFICIENT BANK LOADING FORMAT

	CC11	CC10	CC9	CC8	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
1st Word Address	0	0	0	0	0	0	0	0	1	0	1	0
2nd Word Bank 1	1	0	1	0	1	0	1	1	1	1	0	0
3rd Word Bank 2	0	1	1	1	1	0	0	0	1	0	0	1
4th Word Bank 3	0	1	0	0	0	1	0	1	0	1	1	0
5th Word Bank 4	0	0	0	1	0	0	1	0	0	0	1	1

TABLE 4. ROUND REGISTER LOADING FORMAT

	CC11	CC10	CC9	CC8	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
1st Word Address	1	0	0	0	0	0	0	0	1	0	1	0
2nd Word	R	R	R	R	0	0	0	1	0	0	0	*0
3rd Word	R	R	R	R	0	0	1	1	0	0	1	0
4th Word	R	R	R	R	0	1	0	1	0	1	0	0
5th Word	R	R	R	R	**0	1	1	1	0	1	1	0

R = Reserved. Must be set to "0".
* This bit represents the LSB of the Round Register.
** This bit represents the MSB of the Round Register.

TABLE 5. LIMIT REGISTER LOADING FORMAT

	CC11	CC10	CC9	CC8	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
1st Word Address	1	1	0	0	0	0	0	0	1	1	1	1
2nd Word	R	R	R	R	0	0	1	0	0	0	1	1
3rd Word	R	R	R	R	*0	0	0	0	0	0	0	1
4th Word	R	R	R	R	1	1	1	0	1	1	0	1
5th Word	R	R	R	R	**0	1	1	1	1	1	1	1

R = Reserved. Must be set to "0".
* This bit represents the MSB of the Lower Limit Register.
** This bit represents the MSB of Upper Limit Register.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +4.5 V
Input signal with respect to ground	–0.5 V to 5.5 V
Signal applied to high impedance output	–0.5 V to 5.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA
ESD Classification (MIL-STD-883E METHOD 3015.7)	Class 3

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	3.00 V ≤ V_{CC} ≤ 3.60 V
Active Operation, Military	–55°C to +125°C	3.00 V ≤ V_{CC} ≤ 3.60 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			150	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			2	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

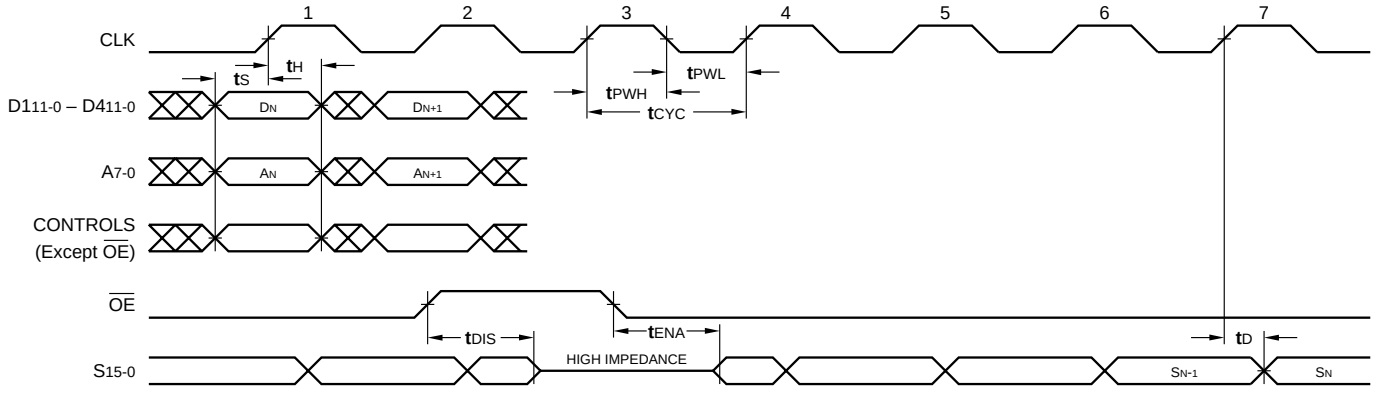
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF3347–					
		25*		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	25		15		12	
t_{PWL}	Clock Pulse Width Low	10		7		5	
t_{PWH}	Clock Pulse Width High	10		7		5	
t_S	Input Setup Time	8		5		3	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		13		10		8
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		12		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		11		8

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF3347–					
		25*		15*		12*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	25		15		12	
t_{PWL}	Clock Pulse Width Low	10		7		5	
t_{PWH}	Clock Pulse Width High	10		7		5	
t_S	Input Setup Time	8		5		3	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		13		10		8
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		12		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		11		8

SWITCHING WAVEFORMS: DATA I/O



*DISCONTINUED SPEED GRADE

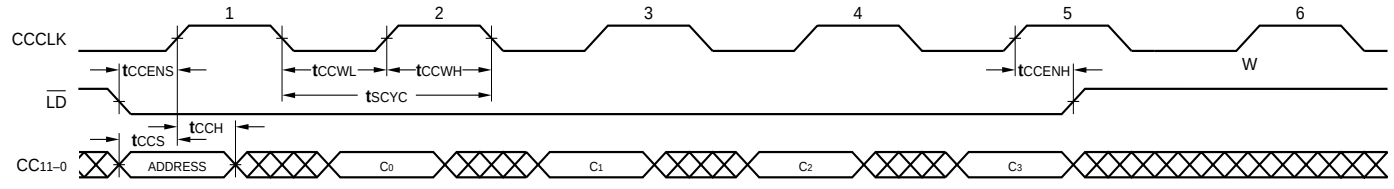
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF3347–					
		25*		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CCCYC}	Control Coefficient Interface Cycle Time	25		15		12	
t_{CCWL}	Control Coefficient Clock Pulse Width Low	10		7		5	
t_{CCWH}	Control Coefficient Clock Pulse Width High	10		7		5	
t_{CCENS}	Control Coefficient Enable Setup Time	8		5		3	
t_{CCENH}	Control Coefficient Enable Hold Time	0		0		0	
t_{CCS}	Control Coefficient Data Input Setup Time	8		5		5	
t_{CCH}	Control Coefficient Data Input Hold Time	0		0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF3347–					
		25*		15*		12*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CCCYC}	Control Coefficient Interface Cycle Time	25		15		12	
t_{CCWL}	Control Coefficient Clock Pulse Width Low	10		7		5	
t_{CCWH}	Control Coefficient Clock Pulse Width High	10		7		5	
t_{CCENS}	Control Coefficient Enable Setup Time	8		5		3	
t_{CCENH}	Control Coefficient Enable Hold Time	0		0		0	
t_{CCS}	Control Coefficient Data Input Setup Time	8		5		5	
t_{CCH}	Control Coefficient Data Input Hold Time	0		0		0	

SWITCHING WAVEFORMS: COEFFICIENT BANK AND CONTROL REGISTER INPUT



W: Coefficient Banks/Control Registers written to on this clock cycle.

*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. The device can withstand indefinite operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 30 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except **t**DIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and **V**CC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the **t**ENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the **t**DIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

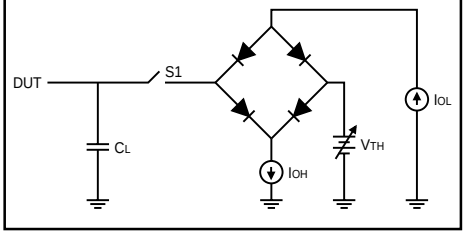
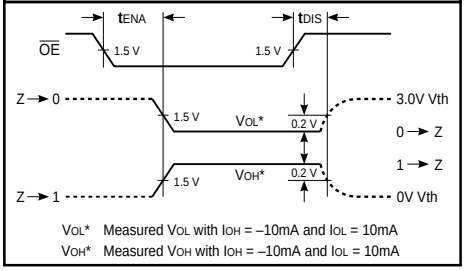
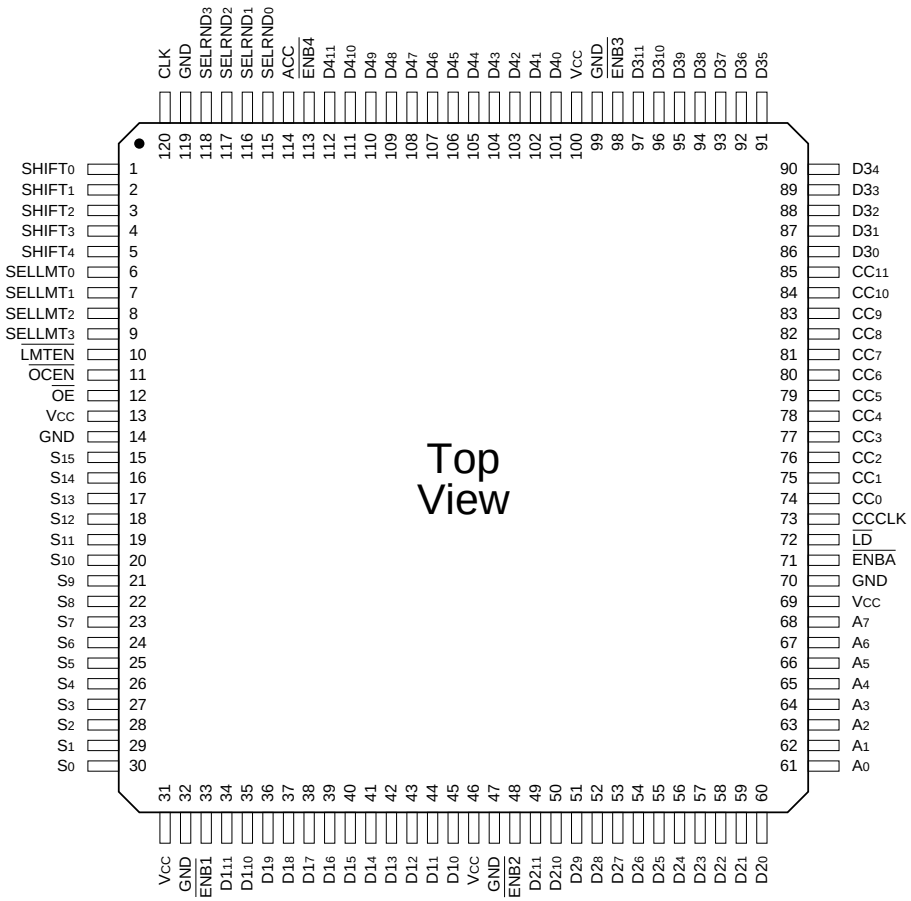


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

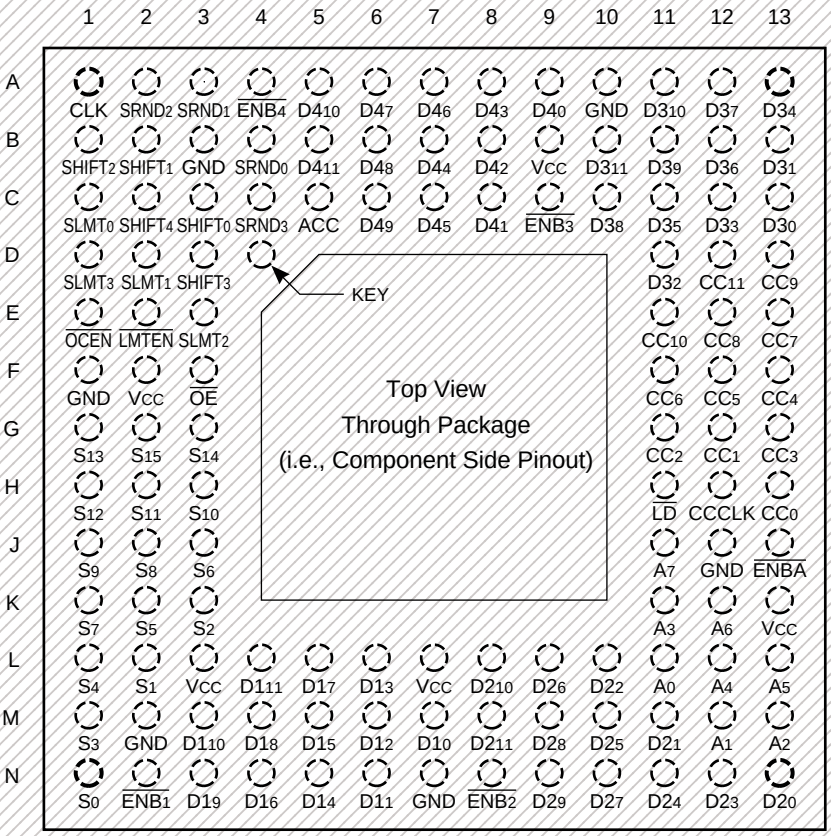
120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
15 ns	LF3347QC15
12 ns	LF3347QC12

ORDERING INFORMATION

120-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
	–55°C to +125°C — COMMERCIAL SCREENING
	–55°C to +125°C — MIL-STD-883 COMPLIANT