

# Low Power JFET Input Operational Amplifiers

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The LF441C device provides for the external null adjustment of input offset voltage.

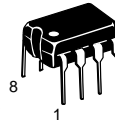
These devices are specified over the commercial temperature range. All are available in plastic dual in-line and SOIC packages.

- Low Supply Current: 200  $\mu$ A/Amplifier
- Low Input Bias Current: 5.0 pA
- High Gain Bandwidth: 2.0 MHz
- High Slew Rate: 6.0 V/ $\mu$ s
- High Input Impedance:  $10^{12}$   $\Omega$
- Large Output Voltage Swing:  $\pm 14$  V
- Output Short Circuit Protection

## LF441C LF442C LF444C

### LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

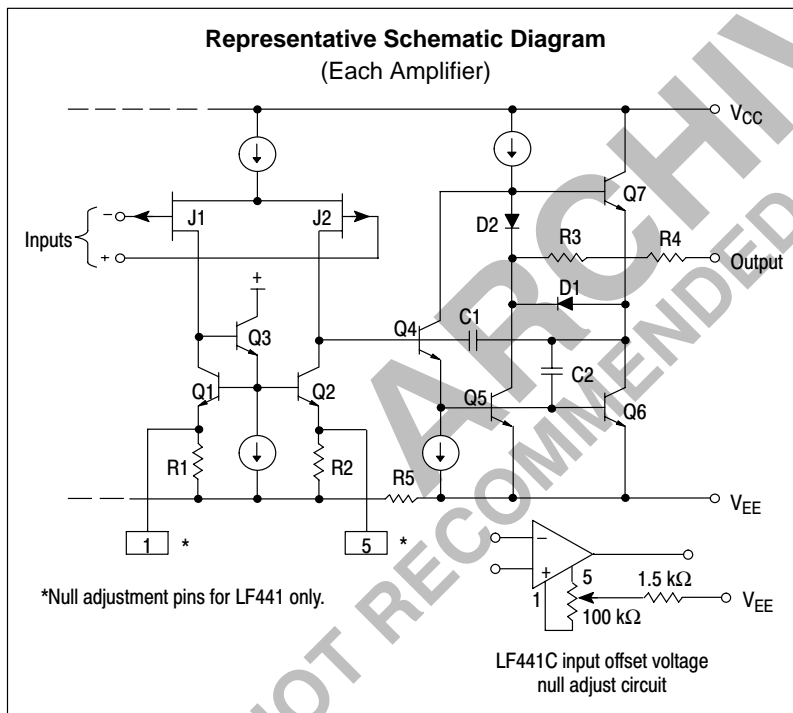
#### SEMICONDUCTOR TECHNICAL DATA



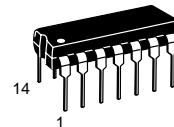
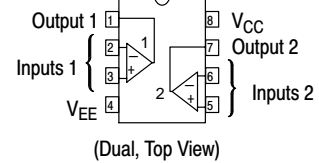
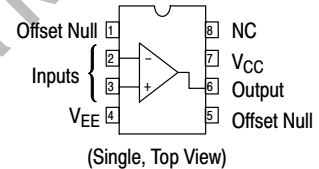
**N SUFFIX**  
PLASTIC PACKAGE  
CASE 626



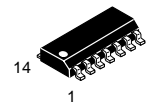
**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751  
(SO-8)



#### PIN CONNECTIONS

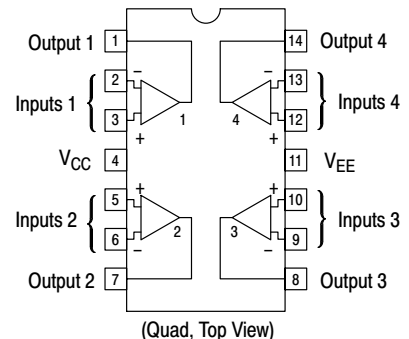


**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646



**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751A  
(SO-14)

#### PIN CONNECTIONS



#### ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF441CD LF441CN	Single	$T_A = 0^\circ$ to $+70^\circ\text{C}$	SO-8 Plastic DIP
LF442CD LF442CN	Dual		SO-8 Plastic DIP
LF444CD LF444CN	Quad		SO-14 Plastic DIP

# LF441C LF442C LF444C

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from $V_{CC}$ to $V_{EE}$ )	$V_S$	+36	V
Input Differential Voltage Range (Note 1)	$V_{IDR}$	$\pm 30$	V
Input Voltage Range (Notes 1 and 2)	$V_{IR}$	$\pm 15$	V
Output Short Circuit Duration (Note 3)	$t_{SC}$	Indefinite	sec
Operating Junction Temperature (Note 3)	$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	-60 to +150	$^{\circ}\text{C}$

- NOTES:**
- Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
  - The magnitude of the input voltage must never exceed the magnitude of the supply or 15 V, whichever is less.
  - Power dissipation must be considered to ensure maximum junction temperature ( $T_J$ ) is not exceeded (see Figure 1).

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $T_A = 0^{\circ}$ to $70^{\circ}\text{C}$ , unless otherwise noted.)

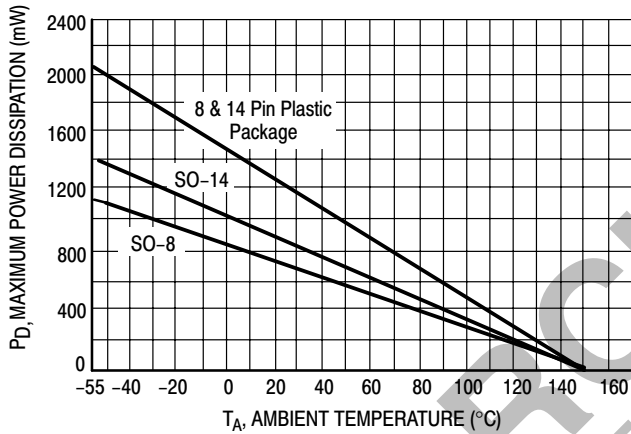
Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ( $R_S = 10\text{ k}\Omega$ , $V_O = 0\text{ V}$ ) Single: $T_A = +25^{\circ}\text{C}$ $T_A = 0^{\circ}$ to $+70^{\circ}\text{C}$ Dual: $T_A = +25^{\circ}\text{C}$ $T_A = 0^{\circ}$ to $+70^{\circ}\text{C}$ Quad: $T_A = +25^{\circ}\text{C}$ $T_A = 0^{\circ}$ to $+70^{\circ}\text{C}$	$V_{IO}$	-	3.0	5.0	mV
Average Temperature Coefficient of Offset Voltage ( $R_S = 10\text{ k}\Omega$ , $V_O = 0\text{ V}$ )	$\Delta V_{IO}/\Delta T$	-	10	-	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current ( $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ ) $T_A = +25^{\circ}\text{C}$ $T_A = 0^{\circ}$ to $+70^{\circ}\text{C}$	$I_{IO}$	-	0.5	50	pA nA
Input Bias Current ( $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ ) $T_A = +25^{\circ}\text{C}$ $T_A = 0^{\circ}$ to $+70^{\circ}\text{C}$	$I_{IB}$	-	3.0	100	pA nA
Common Mode Input Voltage Range ( $T_A = +25^{\circ}\text{C}$ )	$V_{ICR}$	-11	+14.5 -12	+11 -	V
Large Signal Voltage Gain ( $V_O = \pm 10\text{ V}$ , $R_L = 10\text{ k}\Omega$ ) $T_A = +25^{\circ}\text{C}$ $T_A = 0^{\circ}$ to $+70^{\circ}\text{C}$	$A_{VOL}$	25 15	60 -	- -	V/mV
Output Voltage Swing ( $R_L = 10\text{ k}\Omega$ )	$V_{O+}$ $V_{O-}$	+12 -	+14 -14	- -12	V
Common Mode Rejection ( $R_S \leq 10\text{ k}\Omega$ , $V_{CM} = V_{ICR}$ , $V_O = 0\text{ V}$ )	CMR	70	86	-	dB
Power Supply Rejection ( $R_S = 100\ \Omega$ , $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ )	PSR	70	84	-	dB
Power Supply Current (No Load, $V_O = 0\text{ V}$ ) Single Dual Quad	$I_D$	- - -	200 400 800	250 500 1000	$\mu\text{A}$

# LF441C LF442C LF444C

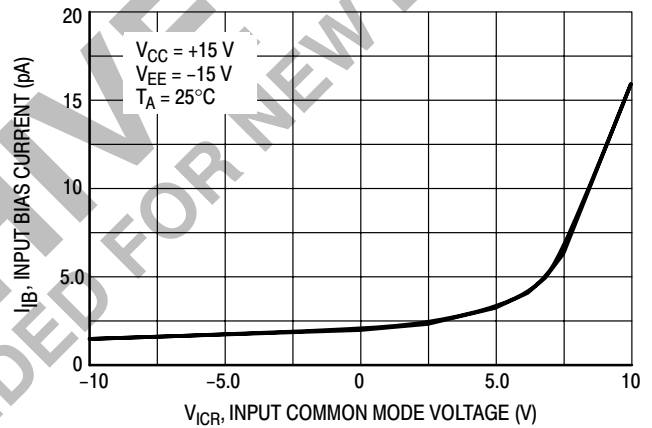
**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +15\text{ V}$ ,  $V_{EE} = -15\text{ V}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ( $V_{in} = -10\text{ V to } +10\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = +1.0$ )	SR	0.6	6.0	–	V/ $\mu\text{s}$
Settling Time ( $A_V = -1.0$ , $R_L = 10\text{ k}\Omega$ , $V_O = 0\text{ V to } +10\text{ V}$ )	$t_s$	–	1.6 2.2	–	$\mu\text{s}$
Gain Bandwidth Product ( $f = 200\text{ kHz}$ )	GBW	0.6	2.0	–	MHz
Equivalent Input Noise Voltage ( $R_S = 100\ \Omega$ , $f = 1.0\text{ kHz}$ )	$e_n$	–	47	–	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current ( $f = 1.0\text{ kHz}$ )	$i_n$	–	0.01	–	pA/ $\sqrt{\text{Hz}}$
Input Resistance	$R_i$	–	$10^{12}$	–	$\Omega$
Channel Separation ( $f = 1.0\text{ Hz to } 20\text{ kHz}$ )	CS	–	120	–	dB

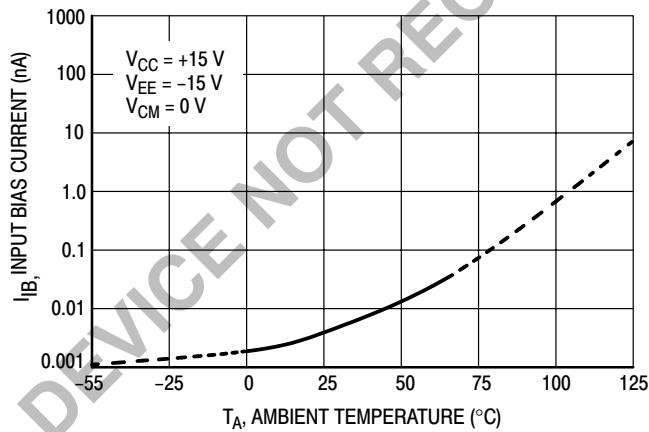
**Figure 1. Maximum Power Dissipation versus Temperature for Package Variations**



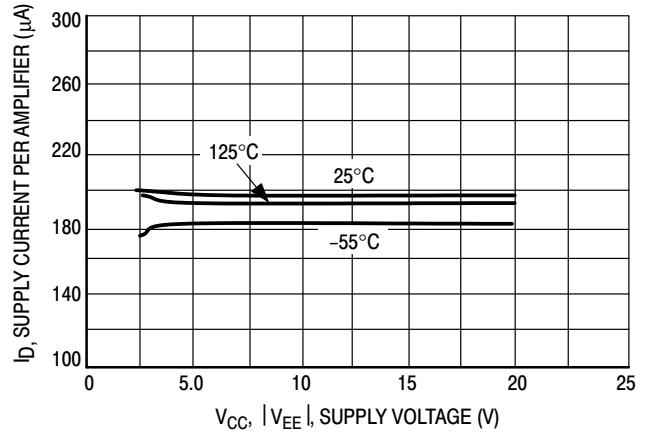
**Figure 2. Input Bias Current versus Input Common Mode Voltage**



**Figure 3. Input Bias Current versus Temperature**



**Figure 4. Supply Current versus Supply Voltage**



LF441C LF442C LF444C

Figure 5. Positive Input Common Mode Voltage Range versus Positive Supply Voltage

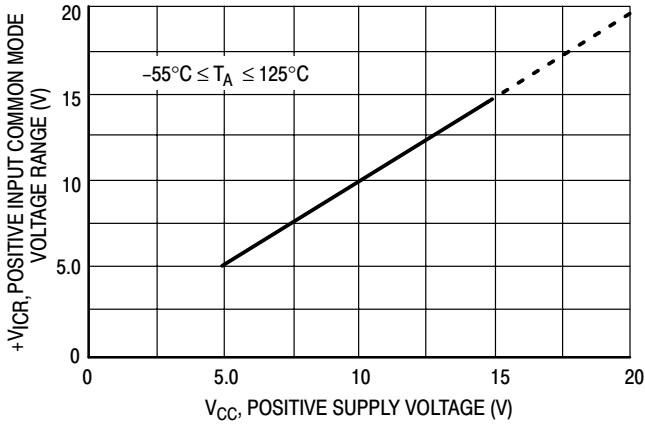


Figure 6. Negative Input Common Mode Voltage Range versus Negative Supply Voltage

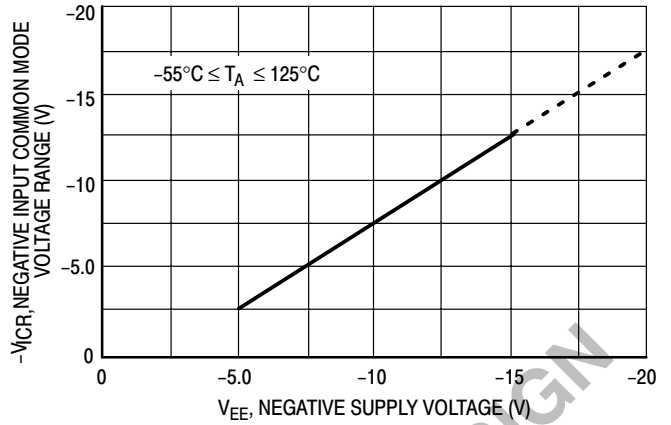


Figure 7. Output Voltage versus Output Source Current

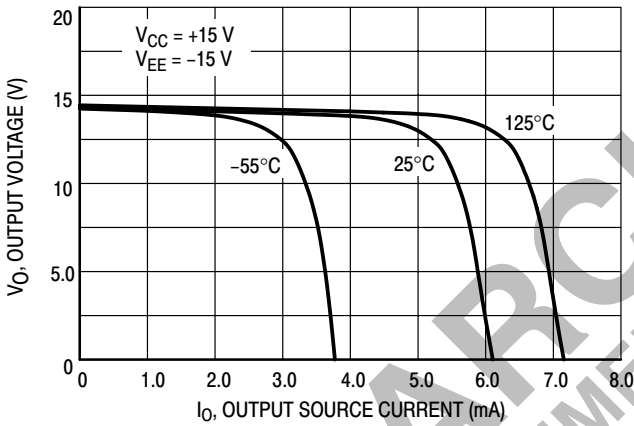


Figure 8. Output Voltage versus Output Sink Current

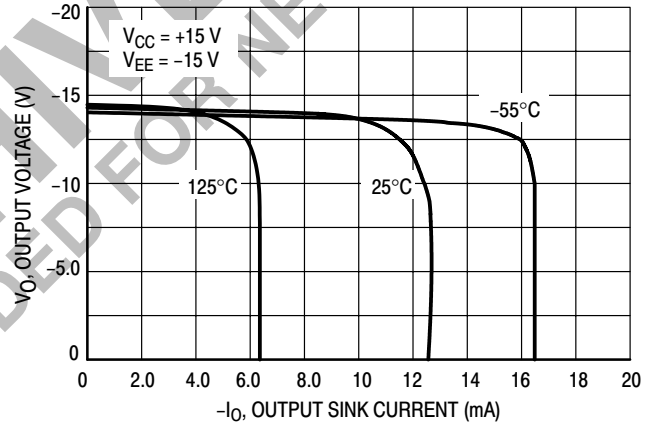


Figure 9. Output Voltage Swing versus Supply Voltage

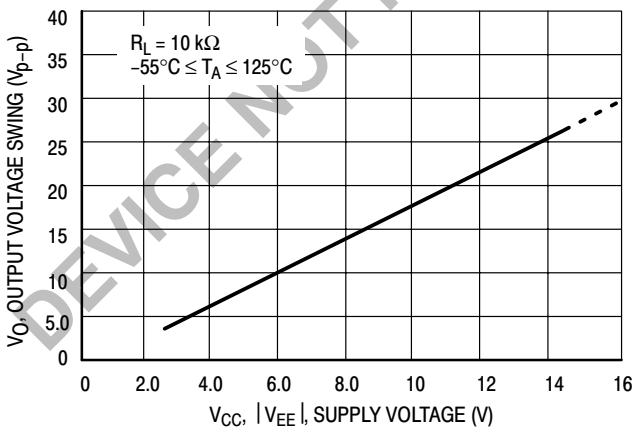


Figure 10. Output Voltage Swing versus Load Resistance

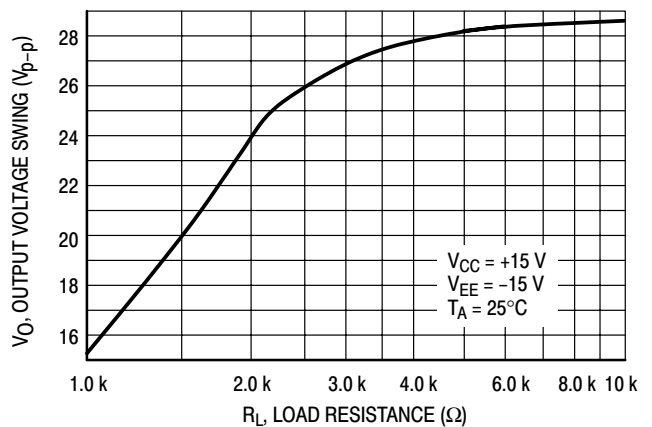


Figure 11. Normalized Gain Bandwidth Product versus Temperature

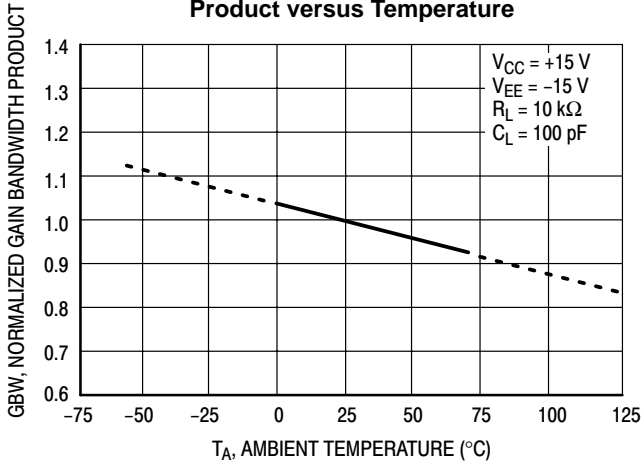


Figure 12. Open Loop Voltage Gain and Phase versus Frequency

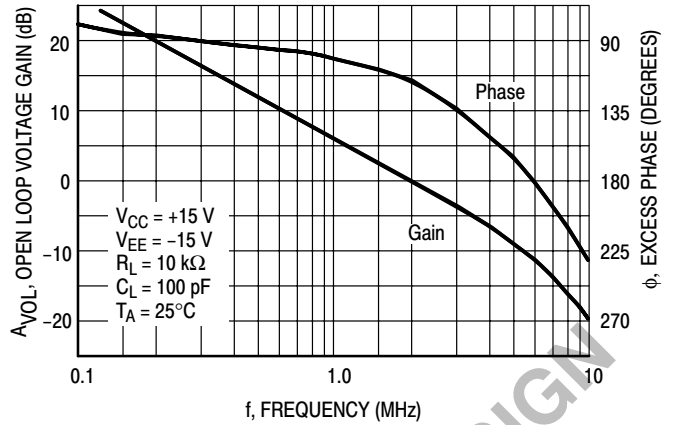


Figure 13. Slew Rate versus Temperature

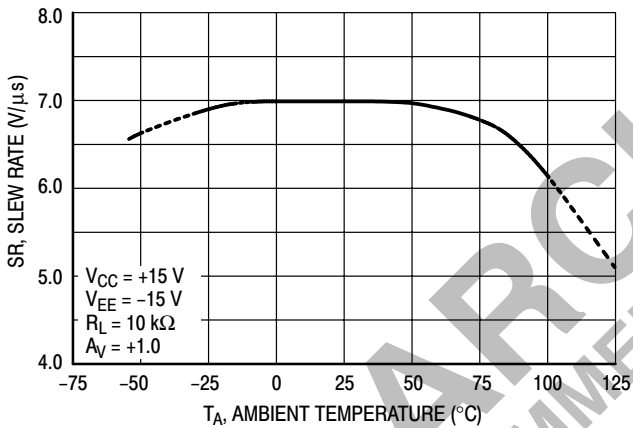


Figure 14. Total Output Distortion versus Frequency

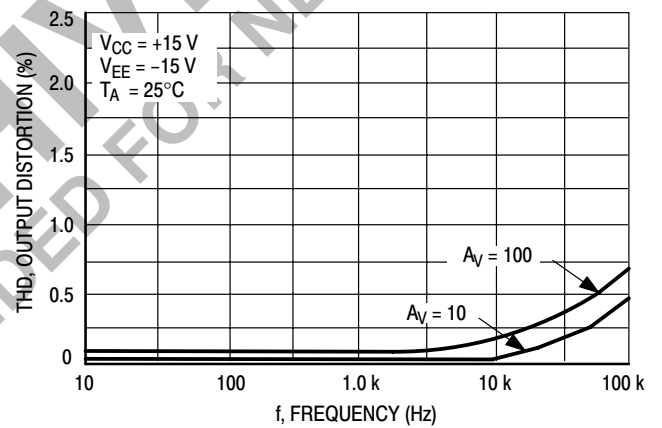


Figure 15. Output Voltage Swing versus Frequency

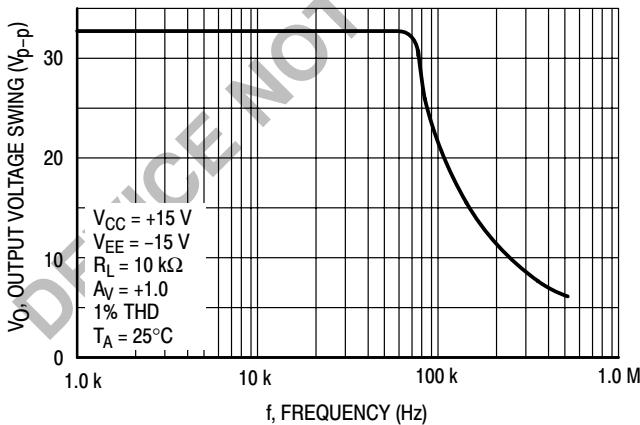


Figure 16. Open Loop Voltage Gain versus Frequency

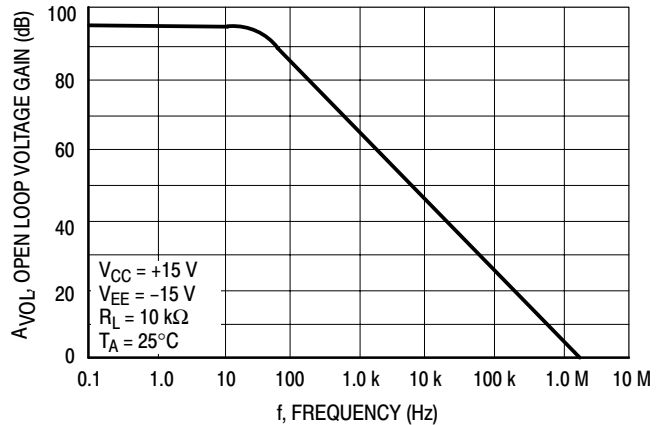


Figure 17. Common Mode Rejection versus Frequency

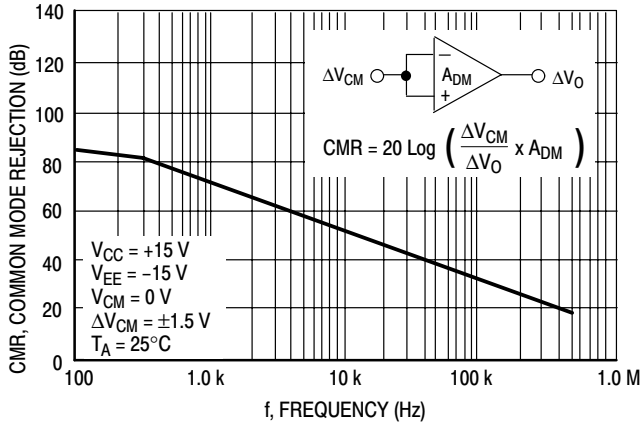


Figure 18. Power Supply Rejection versus Frequency

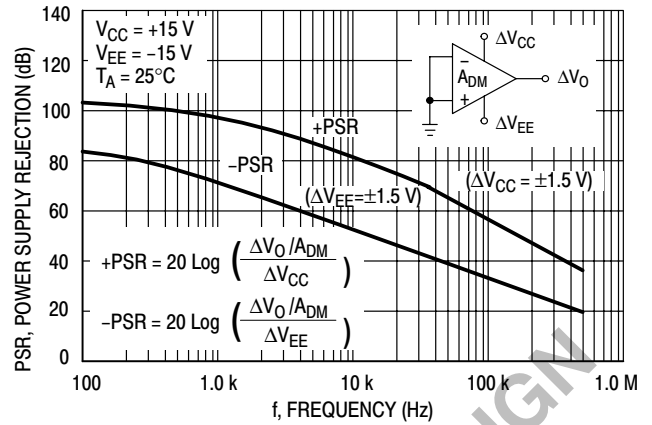


Figure 19. Input Noise Voltage versus Frequency

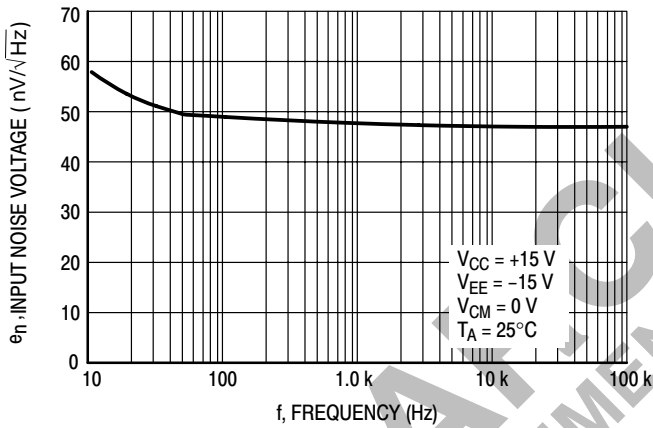


Figure 20. Open Loop Voltage Gain versus Supply Voltage

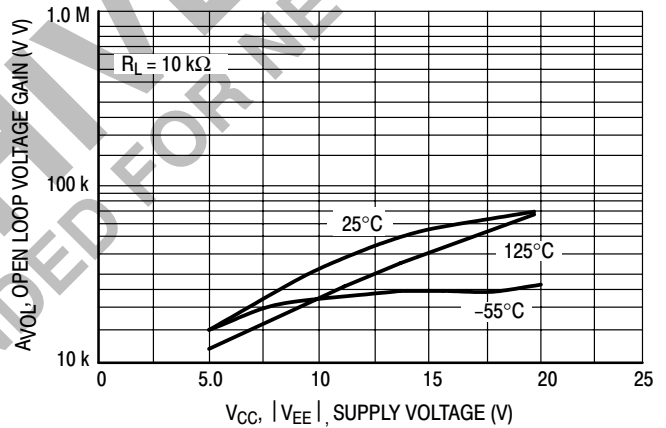


Figure 21. Output Impedance versus Frequency

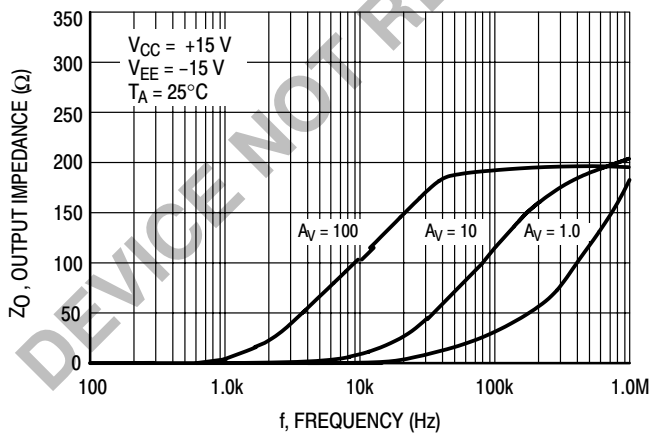
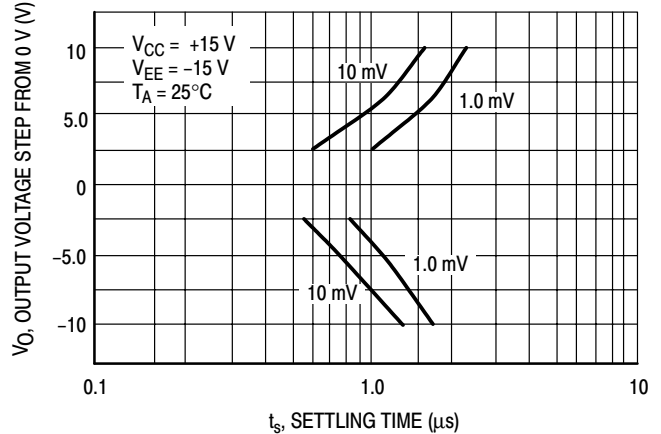


Figure 22. Inverter Settling Time



# LF441C LF442C LF444C

## SMALL SIGNAL RESPONSE

Figure 23. Inverting

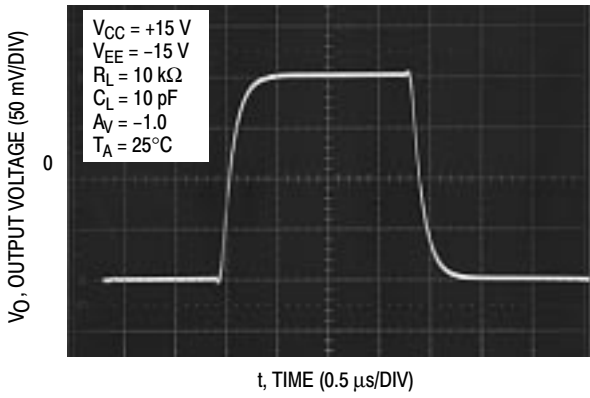
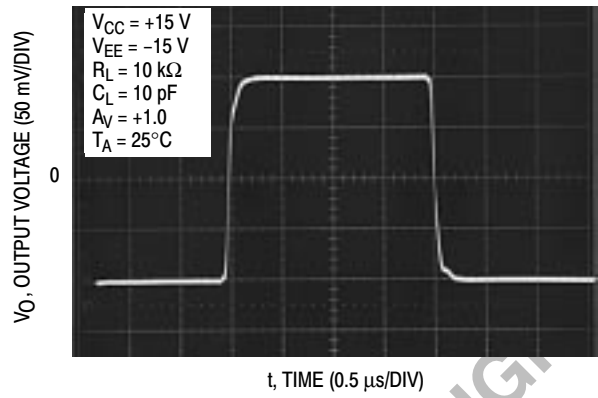


Figure 24. Noninverting



## LARGE SIGNAL RESPONSE

Figure 25. Inverting

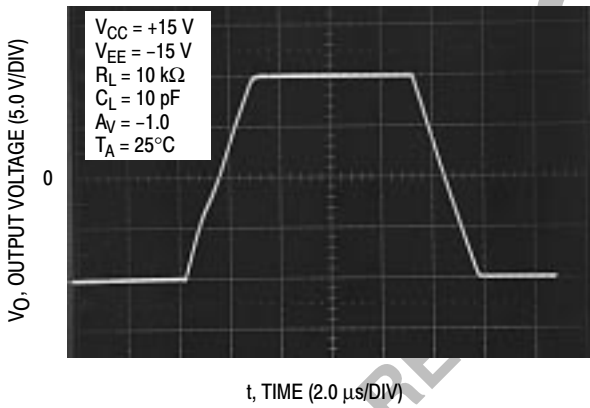
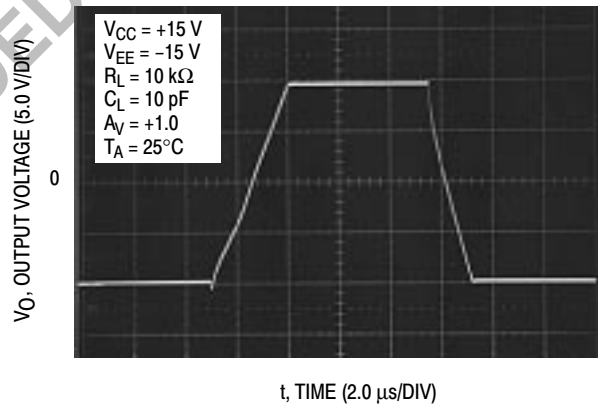


Figure 26. Noninverting



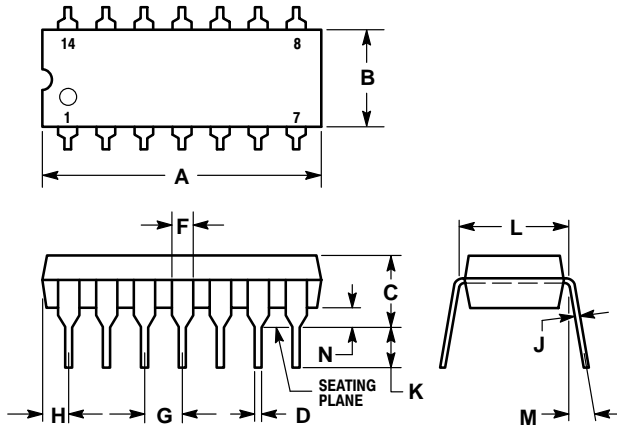




# LF441C LF442C LF444C

## OUTLINE DIMENSIONS

### N SUFFIX PLASTIC PACKAGE CASE 646-06 ISSUE L

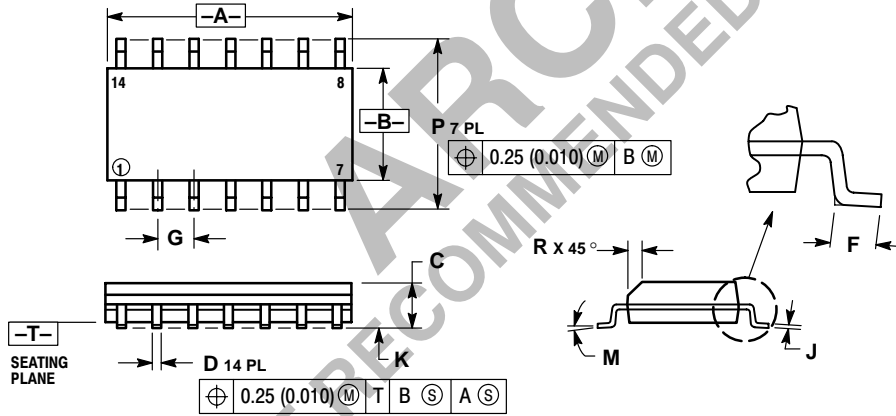


#### NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

### D SUFFIX PLASTIC PACKAGE CASE 751A-03 (SO-14) ISSUE F




#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

ARCHIVE  
RECOMMENDED FOR NEW DESIGN

**ON Semiconductor** is a trademark and  is a registered trademark of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

#### PUBLICATION ORDERING INFORMATION

**Literature Fulfillment:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2700  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.