National Semiconductor

September 1992

LF6197 160 ns Monolithic Sample-and-Hold Amplifier

General Description

The LF6197 is a monolithic sample-and-hold (S/H) amplifier that uses a proprietary "current-multiplexed sample-and-hold" technique to offer extremely high speed while maintaining 12 bits or higher accuracy. The device is built using National's advanced junction-isolated VIP™ (Vertically Integrated PNP) and BI-FET™ process technologies.

The LF6197 acquires a 10V step input to within ±0.01% in 160 ns and has 10 mV hold step error when going from sample to hold mode. The input offset voltage in the sample mode is typically 3 mV. Even at extremely fast acquisition speeds, no compromises are made in the droop rate, which is 0.6 μV/μs. When configured for unity gain, the DC gain error is 0.03%. The feedthrough attenuation in the hold mode is 83 dB at DC and 77 dB at 100 kHz.

The LF6197 can be externally configured for either inverting or non-inverting gains, thus offering additional flexibility to the user. The device includes an internal 10 pF hold capacitor.

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Features

- Operates with supply voltages from ±5V to ±18V
- CMOS, TTL and ECL compatible logic input
- Adjustable inverting or non-inverting gain
- Internal hold capacitor
- High power-supply rejection in both sample and hold modes

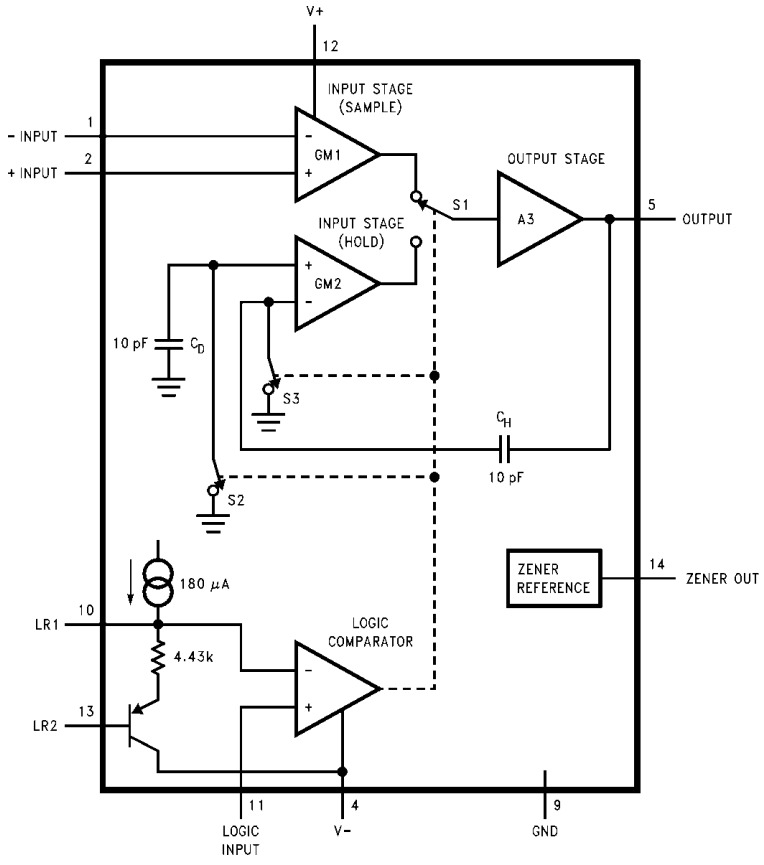
Key Specifications

■ Acquisition time (10V step to 0.01%)	160 ns
■ Hold mode settling time (10V step to 0.01%)	50 ns
■ Droop rate	0.6 μV/μs
■ Hold step	10 mV
■ Aperture jitter	8 ps_{rms}
■ Feedthrough attenuation at DC	83 dB
■ Small signal bandwidth	25 MHz

Applications

- High-speed data acquisition systems
- Automatic test equipment
- High-speed instrumentation
- Replaces expensive hybrid sample-and-hold amplifiers

Block Diagram



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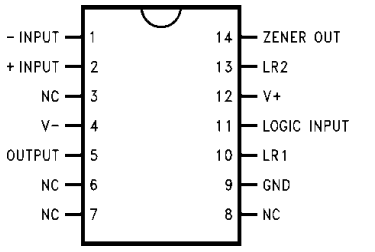
Connection Diagram



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Top View

Ordering Information

Industrial ($0°C < T_A < +70°C$)	Package
LF6197CCJ	J14A Ceramic DIP

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1, 2)

Positive Supply Voltage (V^+)	$+18V$
Negative Supply Voltage (V^-)	$-18V$
Analog Input Voltage	V^+ or V^- or $\pm 12.5V$, whichever is less
Logic Input to LR1 Differential Voltage	$\pm 5V$
Power Dissipation (Note 3)	1.2W
Duration of Output Short Circuit to GND	(Note 4)
ESD Susceptibility	
All Pins except Pin 13 (Note 5)	2000V
Pin 13 only (Note 5)	1500V
Lead Temperature (Soldering, 10 sec.)	
J Package	300°C
Storage Temperature	$-65°C$ to $+150°C$

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF6197CCJ	$0°C \le T_A \le +70°C$
Positive Supply Voltage	$+4.75V \le V^+ \le +15.75V$
Negative Supply Voltage	$-15.75V \le V^- \le -4.75V$

Electrical Characteristics

Unless otherwise specified, the following specifications apply for $V^+ = +15V$, $V^- = -15V$, $-12V \le V_{IN} \le +12V$, $R_L > 1\ k\Omega$, $C_L \le 40$ pF, Logic Reference 2 (LR2) voltage = 0V and Logic Input Voltage < 1.4V threshold, (Unit is in "sample" mode). V_S refers to the supply voltages, V^+ and V^-. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units (Limit)
INPUT CHARACTERISTICS					
V_{OS}	Input Offset Voltage	 $V_S = \pm 5V$, (Note 8)	± 3.0 ± 3.0	$\pm$ **6.0**	mV (max) mV (max)
$\Delta V_{OS}/\Delta T$	Input Offset Drift		15		$\mu V/°C$
$R_{IN,\ com}$	Input Resistance (common mode)		10		$M\Omega$
$R_{IN,\ dif}$	Input Resistance (differential)		300		$k\Omega$
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	100	80	dB (min)
I_{B+}	Positive Input Bias Current		7	17	μA (max)
I_{B-}	Negative Input Bias Current		1	7.5	μA (max)
TRANSFER CHARACTERISTICS					
	DC Open Loop Gain	$V_{OUT} = \pm 12V$, $R_L = 1\ k\Omega$	70	65	dB (min)
	DC Open Loop Gain (Note 8)	$V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$	55	49	dB (min)
	Gain Error (Note 9)		0.03		% (max)
	Gain Linearity Error	$V_{OUT} = \pm 10V$	0.003	0.0045	% (max)
f_u	Gain Bandwidth Product		25	14	MHz (min)
OUTPUT CHARACTERISTICS					
R_{OUT}	Output Resistance		0.02		Ω
SR	Slew Rate		145		$V/\mu s$
	Short Circuit Source Current		-63	-25	mA (min)
	Short Circuit Sink Current		70	25	mA (min)
C_L	Maximum Capacitive Load	No Oscillation	200		pF

Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for $V^+ = +15V$, $V^- = -15V$, $-12V \le V_{IN} \le +12V$, $R_L > 1\ k\Omega$, $C_L \le 40$ pF, Logic Reference 2 (LR2) voltage = 0V and Logic Input Voltage < 1.4V threshold, (Unit is in "sample" mode). V_S refers to the supply voltages, V^+ and V^-. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units (Limit)
SAMPLE/HOLD CHARACTERISTICS					
t_{ACQ}	Acquisition Time				
	to 0.1% (Note 10)	10V step	130		ns
	to 0.01% (Note 10)	+10V step	145	240	ns (max)
				260	ns (max)
		−10V step	160	240	ns (max)
				260	ns (max)
t_{AD}	Aperture Delay Time		4		ns
t_{AJ}	Aperture Jitter		8		ps_{rms}
	Droop Rate		0.6	10	$\mu V/\mu s$ (max)
V_{HS}	Hold Step (Note 11)		±10		mV (max)
t_{HMS}	Hold Mode Settling Time to 0.01%	10V step	50		ns
	Feedthrough Attenuation (Note 12)	f = 1 kHz, V_{IN} = 20 V_{p-p}	83	80	dB (min)
		f = 100 kHz, V_{IN} = 20 V_{p-p}	77		dB
DYNAMIC CHARACTERISTICS					
THD	Total Harmonic Distortion	f = 10 kHz, V_{IN} = 20 V_{p-p}	−83		dB
		f = 150 kHz, V_{IN} = 20 V_{p-p}	−78		dB
FPBW	Full Power Bandwidth (Note 13)	V_{IN} = 20 V_{p-p}	2.3		MHz
	Small Signal Bandwidth		25		MHz
DIGITAL LOGIC CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage			**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage			**0.8**	V (max)
	Logic Input Current		6	**20**	μA (max)
	Logic Reference 2 Input Current		3	**5**	μA (max)
	Differential Logic Threshold		1.4	1.1	V(min)
	(Logic Input to LR1)			1.6	V(max)
POWER SUPPLY CHARACTERISTICS					
I_{S+}	Positive Supply Current		20	**30**	mA (max)
I_{S+}	Positive Supply Current	V_S = ±5V (Note 8)	18.2	**27**	mA (max)
I_{S-}	Negative Supply Current		20	**30**	mA (max)
I_{S-}	Negative Supply Current	V_S = ±5V (Note 8)	17.5	**27**	mA (max)
PSRR	Power Supply Rejection Ratio	V_S = ±12V to ±16V	84	74	dB (min)

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, Θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_D = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$ and $\theta_{JA} = 125°C/W$. The Power Derating Curve shows the safe thermal operating area for this device.

Note 4: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 5: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at $T_A = 25°C$ and represent the most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Operation at ±5V requires that pin 14 be forced to 2.5V.

Note 9: Gain error is calculated from the measured open loop gain.

Note 10: The acquisition time of the LF6197 has been measured when the device has been configured as an inverting amplifier with a gain of −1, feedback resistor of 2 kΩ, feedback capacitor of 1 pF, and a total load resistor of 1 kΩ.

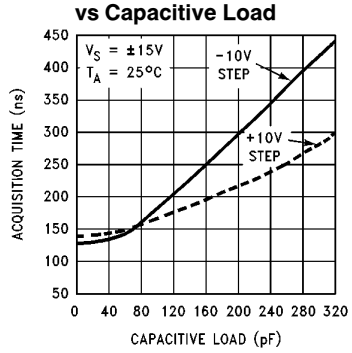
Note 11: Hold step is measured with the LF6197 configured as a unity gain follower and input connected to ground. A TTL pulse with 4 ns rise and fall times is applied to the logic input; the hold step is dependent on the slew rate of the logic input pulse.

Note 12: See test circuit, *Figure 1*.

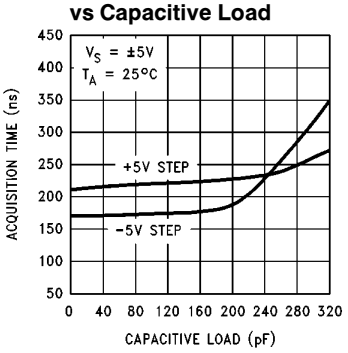
Note 13: Full power bandwidth is calculated using $FPBW = SR/(2\pi V_P)$; where SR is the measured slew rate and V_P is the peak voltage.

Typical Performance Characteristics

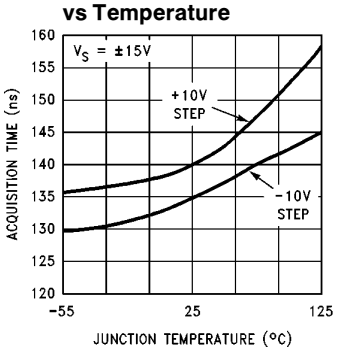
Acquisition Time (to 0.01%) vs Capacitive Load



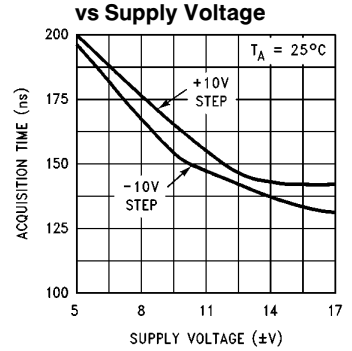
Acquisition Time (to 0.01%) vs Capacitive Load



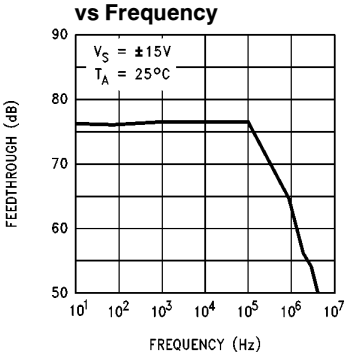
Acquisition Time (to 0.01%) vs Temperature



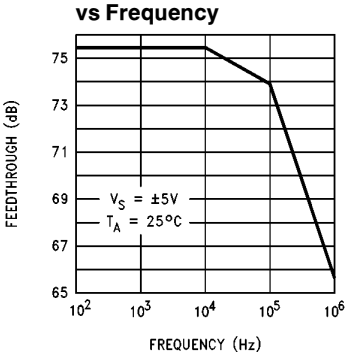
Acquisition Time (to 0.01%) vs Supply Voltage



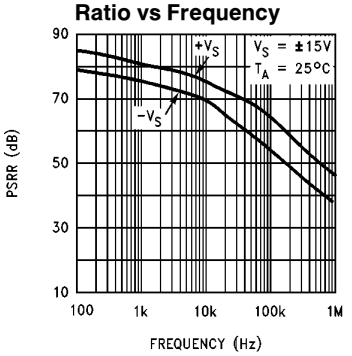
Signal Feedthrough vs Frequency



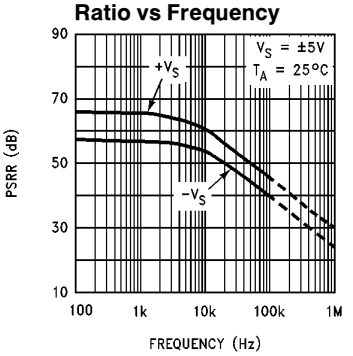
Signal Feedthrough vs Frequency



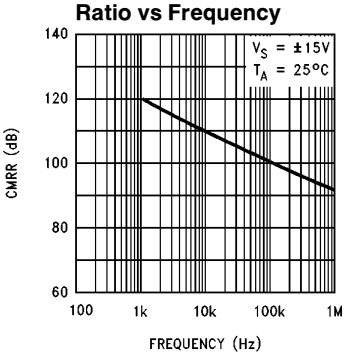
Power Supply Rejection Ratio vs Frequency



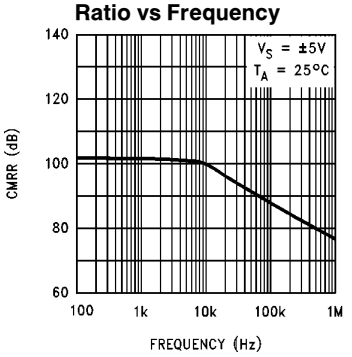
Power Supply Rejection Ratio vs Frequency



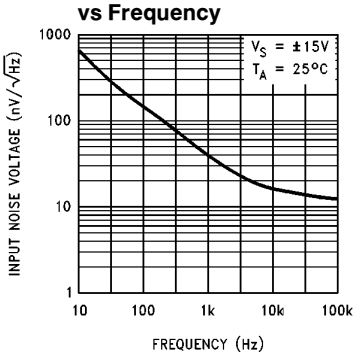
Common Mode Rejection Ratio vs Frequency



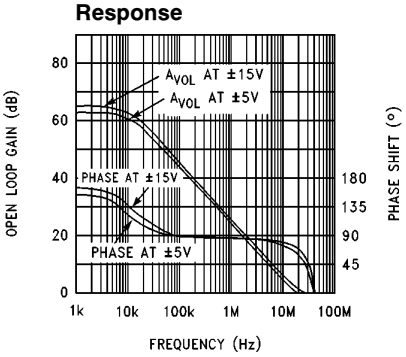
Common Mode Rejection Ratio vs Frequency



Input Noise Voltage vs Frequency



Open Loop Frequency Response



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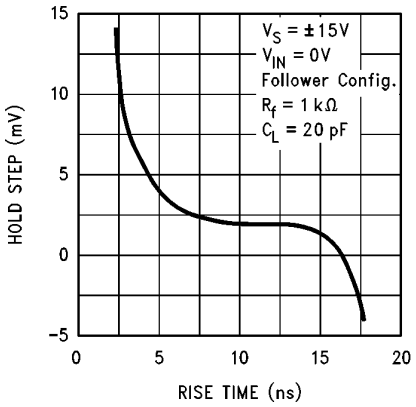
Typical Performance Characteristics (Continued)

Hold Step vs Logic Input Rise Time



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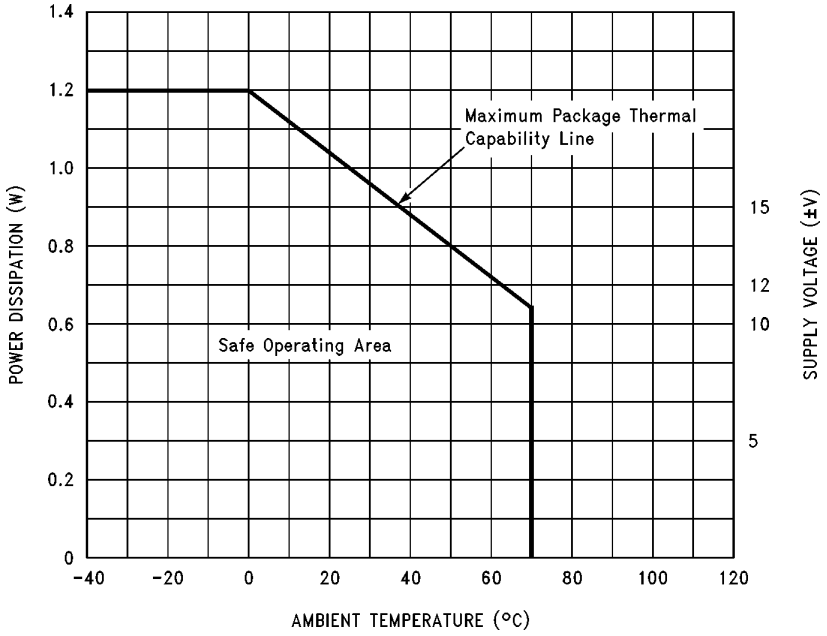
Power Derating Curve



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Test Circuit

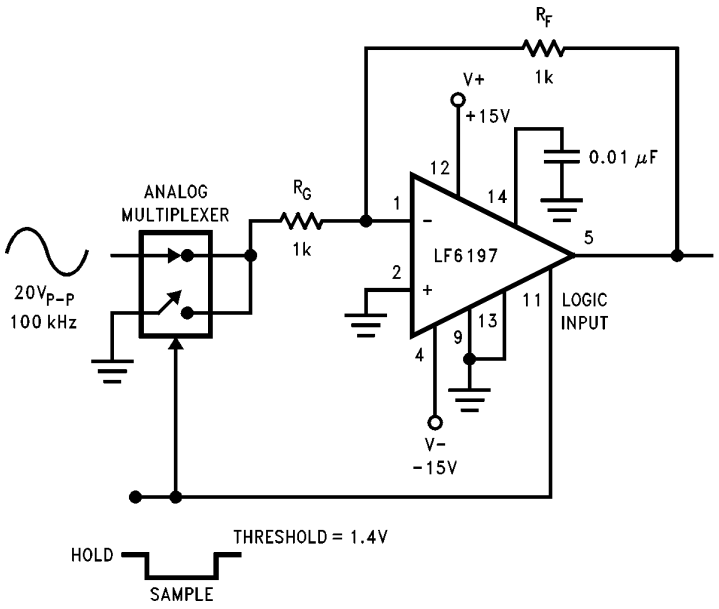

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FIGURE 1. Circuit configuration for the measurement of feedthrough attenuation. Input is connected to ground in sample mode and is connected to 20 V_{PP}, 100 kHz sine wave in hold mode.

Pin Descriptions

V+ (12) This is the positive power supply pin. A +5V to +15V supply voltage should be applied to this pin and bypassed to ground with a 0.1 μF ceramic capacitor in parallel with a 4.7 μF tantalum capacitor.

V− (4) This is the negative power supply pin. A −5V to −15V supply voltage should be applied to this pin and bypassed to ground with a 0.1 μF ceramic capacitor in parallel with a 4.7 μF tantalum capacitor.

GND (9) This is the ground reference pin. All signals are referenced to the potential at this pin.

−Input (1) This is the inverting input of the ''sample'' amplifier. Connecting this pin through a resistor to the output will configure the sample-and-hold amplifier for unity gain. Other inverting and non-inverting gains can be set by applying the familiar op amp feedback topologies. For stability reasons, stray capacitance from the inverting input to ground should be minimized.

+Input (2) This is the non-inverting input of the ''sample'' amplifier. This pin should be driven from a low impedance source.

Output (5) This is the output of the sample-and-hold amplifier.

LR1 (10) This is the Logic Reference 1 input. By applying the appropriate logic threshold at this pin, the sample-and-hold amplifier's logic input can be made either CMOS or ECL compatible. For TTL logic levels, this pin should remain unconnected.

LR2 (13) This is the Logic Reference 2 input. For TTL logic levels, this pin should be connected to ground; this sets the logic threshold at the logic comparator's inverting pin at 1.4V. For CMOS or ECL logic levels this pin should either remain unconnected or connected to pin 10.

Logic Input (11) This is the logic control input pin. A logic low at this pin will configure the amplifier in the ''sample'' mode while a logic high will configure the amplifier in the ''hold'' mode. The TTL, CMOS, or ECL logic compatibility will be determined by the voltage threshold set at the logic comparator's inverting input.

Zener Reference Output (14) For optimum acquisition and settling times, this pin must be bypassed to ground with a 0.01 μF capacitor. Furthermore, for ±5V supply operation, this pin must be biased at 2.5V from a low impedance source.

NC (3,6,7,8) No connection.

Functional Description

The LF6197 uses a proprietary ''current-multiplexed sample-and-hold'' technique as depicted in the simplified block diagram *(Figure 2)*. The amplifier consists of two transconductance input stages g_{m1} and g_{m2} and a common gain and output buffer stage A3. In the sample mode, internal current switching is employed to connect the input stage g_{m1} to the common output stage A3 while input stage g_{m2} is disconnected. Additionally, switches S2 and S3 are closed, thereby shorting the internal dummy capacitor and connecting one end of the hold capacitor to a low impedance ground. Although the simplified schematic shows the switches S1 and S2 connected to ground, the switches are in fact connected to a reference potential which appears as a common mode voltage at the two inputs of g_{m2}.

For unity gain, the inverting input of g_{m1} is externally connected to the output through a resistor, thus closing the loop around the amplifier. Conventional op-amp feedback topologies may be employed to configure the amplifier for inverting and non-inverting gains. In the sample mode, a current booster in the output stage rapidly charges the hold capacitor. A wide-bandwidth amplifier, high-current output stage and fast current-switched hold-to-sample mode selection allows for a slew rate of 145 V/μs and acquisition time of under 200 ns.

When there is a change to the Hold mode, switches S2 and S3 are quickly opened and switch S1 is effectively connected to the output of g_{m2} while input stage g_{m1} is disconnected. The composite amplifier is now comprised of g_{m2} and A3 and the loop around the amplifier is closed by the hold capacitor. Note that the opening of switch S3 causes charge injection into the hold capacitor. However, an equal amount of charge is injected into the dummy capacitor due to the opening of a matched switch S2. The net effect is a differential cancellation of charge and thus the pedestal error (hold step) is greatly reduced. Meanwhile, excellent feedthrough attenuation is achieved because the input signal is isolated from the output by the inactive input stage g_{m1}.

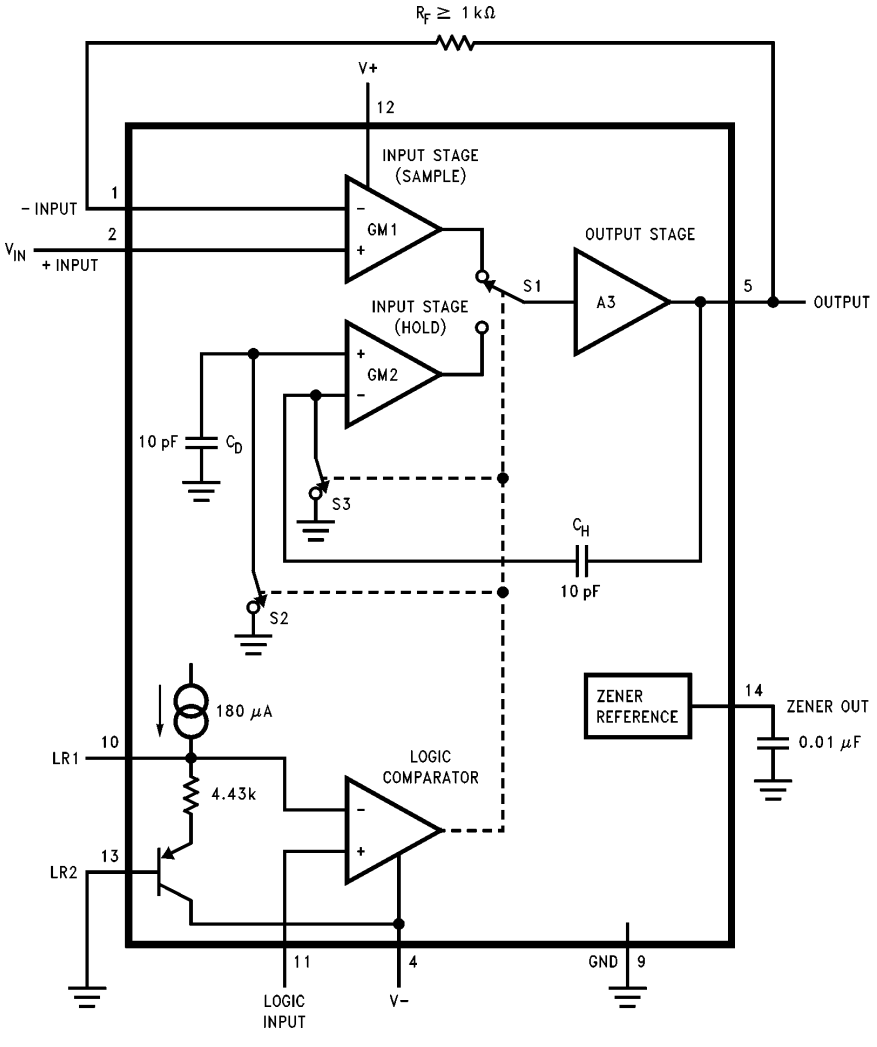

FIGURE 2. Simplified Block Diagram of LF6197 Sample-and-Hold Amplifier, Connected for Unity Gain and TTL Logic

Application Hints

1.0 LOGIC CONFIGURATIONS

The LF6197 can be configured to interface with TTL, CMOS, or ECL logic. The device is configured for the desired logic using the two Logic Reference pins (LR1 and LR2).

1.1 TTL Logic

To configure the device to operate with TTL logic, the LR1 pin should be left open and the LR2 pin should be grounded *(Figure 4)*. This will set the threshold of the logic comparator at 1.4V.

1.2 CMOS Logic

To configure the device to operate with CMOS logic (with a 2.5V threshold at the comparator), several options are available. The LR1 and LR2 pins can be tied together and connected to a 2.5V reference *(Figure 5)*; or LR2 can be set to 1.1V with a resistor diode network and LR1 can be bypassed to ground with a 0.01 μF capacitor *(Figure 6)*.

1.3 ECL Logic

To operate with ECL logic (threshold at -1.3V), set LR2 at -2.7V with a voltage divider from the negative supply and bypass LR1 with a 0.01 μF capacitor *(Figure 7)*.

2.0 ZENER REFERENCE OUTPUT

The LF6197 includes an internal zener diode to bias various sections of the chip. The zener diode output is brought out at pin 14; the voltage at this pin is typically 6.25V when the device is powered from $\pm$15V supplies. For optimum device performance, pin 14 must be bypassed to ground with a 0.01 μF capacitor. If the device is powered from $\pm$5V supplies, then pin 14 must be biased at 2.5V from a low impedance source *(Figure 3)*.

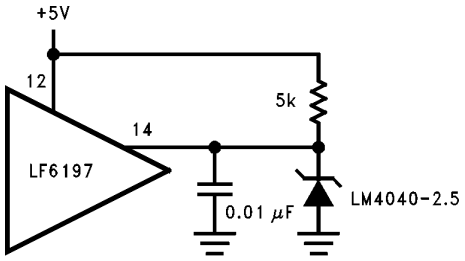

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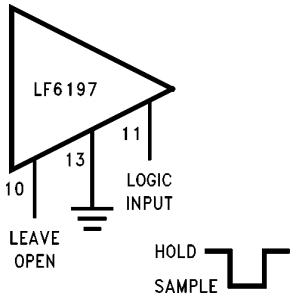
FIGURE 3. Biasing Pin 14 to 2.5V for Operation from $\pm$5V Supplies

3.0 ADJUSTING GAIN

The LF6197 allows the user to amplify as well as to sample-and-hold an input signal. This feature eliminates the need for an amplifier preceding the S/H amplifier in many applications. Familiar op-amp feedback topologies are employed to configure the LF6197 for non-inverting *(Figure 8)* or inverting *(Figure 9)* gains. Note that a feedback resistor of value 1 kΩ or larger must be used for all gain settings, including non-inverting unity gain. The feedback resistor is required to limit the current through LF6197's internal clamp diodes when the device is in the hold mode.

4.0 POWER SUPPLY SEQUENCING

When power supply to the LF6197 is turned on, the negative supply must come on before the positive supply. Meanwhile, when the power supply is turned off, the positive supply must turn off before the negative supply. Improper power supply sequencing may destroy the device. To protect the device against improper power supply sequencing, anti-reversal diodes may be used across the supply pins *(Figure 10)*.



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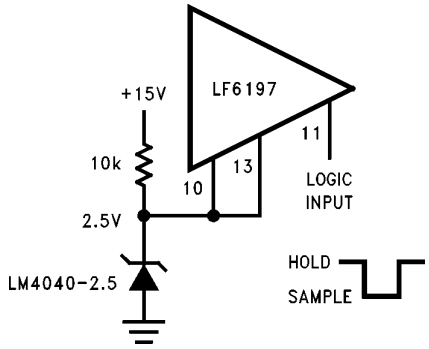
Threshold = 1.4V

FIGURE 4. TTL Logic



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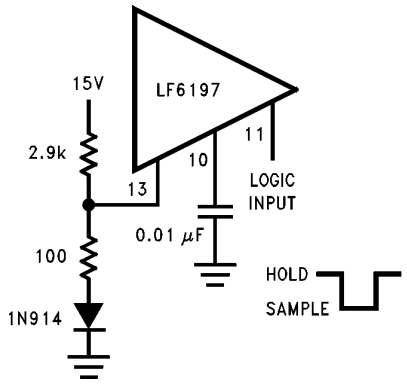
Threshold = 2.5V

FIGURE 5. CMOS Logic

Application Hints (Continued)



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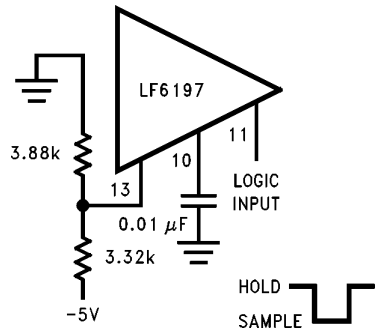
Threshold = 2.5V

FIGURE 6. Another Circuit for CMOS Logic



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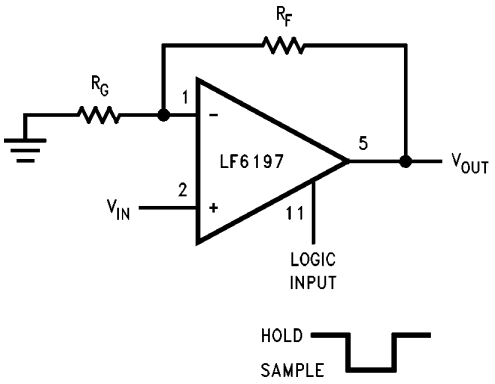
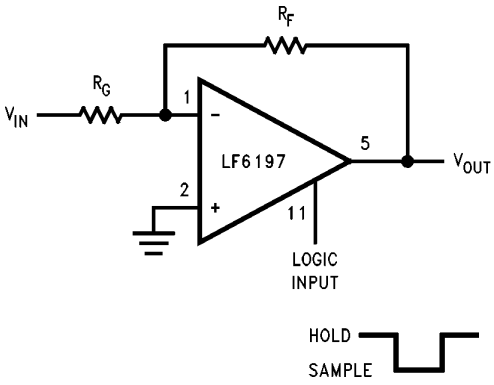
Threshold = 1.3V

FIGURE 7. ECL Logic



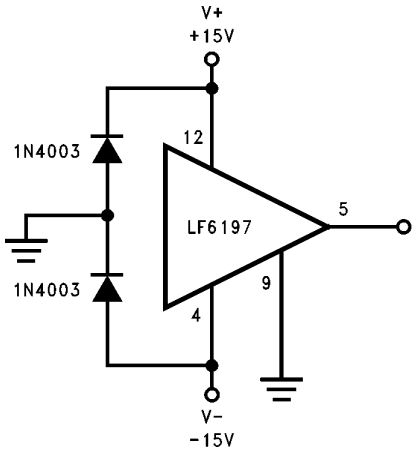
TL/H/11381–12

FIGURE 8. LF6197 with Non-Inverting Gain



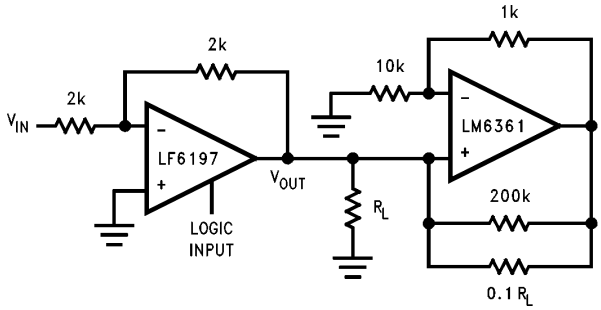
TL/H/11381–13

FIGURE 9. LF6197 with Inverting Gain



TL/H/11381–11

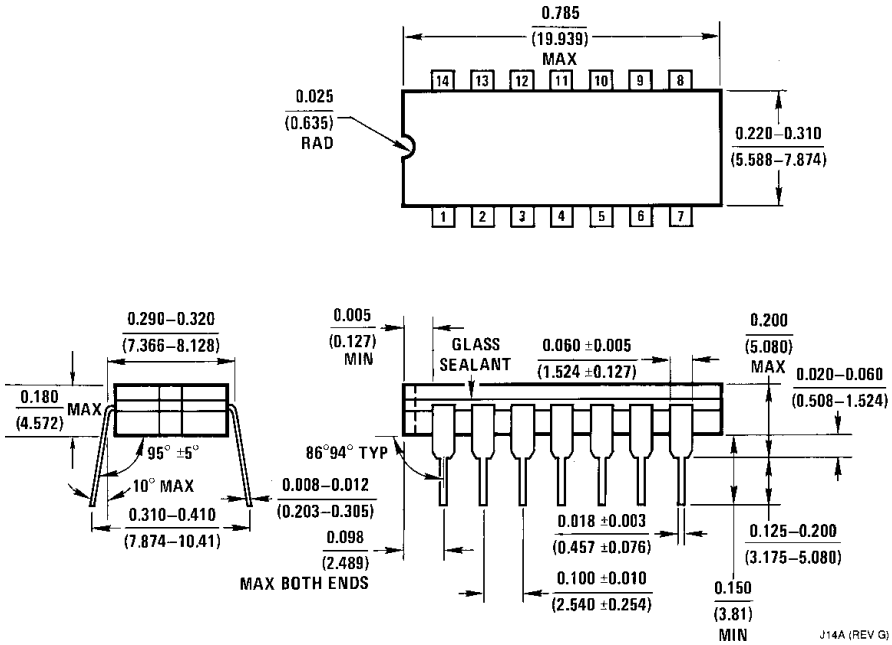
FIGURE 10. Using Anti-Reversal Diodes to Protect LF6197 from Improper Power Supply Sequencing



TL/H/11381–14

FIGURE 11. Increasing Linearity to 16 Bits Using a Negative Impedance Load at the Output of LF6197

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number LF6197CCJ
NS Package Number J14A

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