LGDP4551

720-Channel, 262,144-Color One-Chip Driver with RAM, Power Supply and Gate Circuits for Amorphous TFT-LCD Panels

Ver. 1.00
2008-3-21

Description

The LGDP4551 is a one-chip liquid crystal controller driver LSI, comprising RAM of 240 RGB x 432 dots at maximum, a source driver, a gate driver and a power supply circuit. For effective data transfer, the LGDP4551 supports high-speed 8-/9-/16-/18-bit bus interfaces as a system interface to microcomputer and high-speed RAM write mode.
As a moving picture interface, the LGDP4551 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0).
Also, the LGDP4551 incorporates step-up circuits and voltage follower circuits to generate TFT liquid crystal panel drive voltages.
The LGDP4551's power management functions such as 8-color display and deep standby and so on make this LSI an ideal driver for the medium or small sized portable products with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- A one-chip controller driver incorporating a gate circuit and a power supply circuit for 240RGB x432 dots graphics display on an amorphous TFT panel in 262k colors
- System interface
  - High-speed interfaces via 8-, 9-, 16-, 18-bit parallel ports
  - Serial interface
- Interface for moving picture display
  - 6-, 16-, 18-bit bus RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  - VSYNC interface (System interface + VSYNC)
  - FMARK interface (System interface + FMARK)
- Window address function to specify a rectangular area on the internal RAM to write data
- Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
  - Resizing function (x 1/2, x 1/4)
- Abundant color display and drawing functions
  - Programmable γ -correction function for 262k-color display
  - RGB independent control
  - Partial display function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
  - Standby, Deep standby, sleep function
  - 8-color display function
  - Input power supply voltages: Vcc = 2.5V ~ 3.3 V (logic regulator power supply)
IOVcc = 1.65V ~ 3.3 V (interface I/O power supply)
Vci = 2.5V ~ 3.3 V (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/Vcom power supply: DDVDH-GND = 4.5V ~ 6.0 V
  - Gate drive power supply: VGH-GND = 10.0V ~ 15.0 V
VGL-GND = -4.5V ~ -12.5V
VGH-VGL ≤ 25V
- Liquid crystal power supply startup sequence
- TFT storage capacitance: Cst only (common Vcom formula)
- 233,280-byte internal RAM
- Internal 720-channel source driver and 432-channel gate driver
- Configures a COG module with one chip by arranging gate lines on both sides

Block Diagram

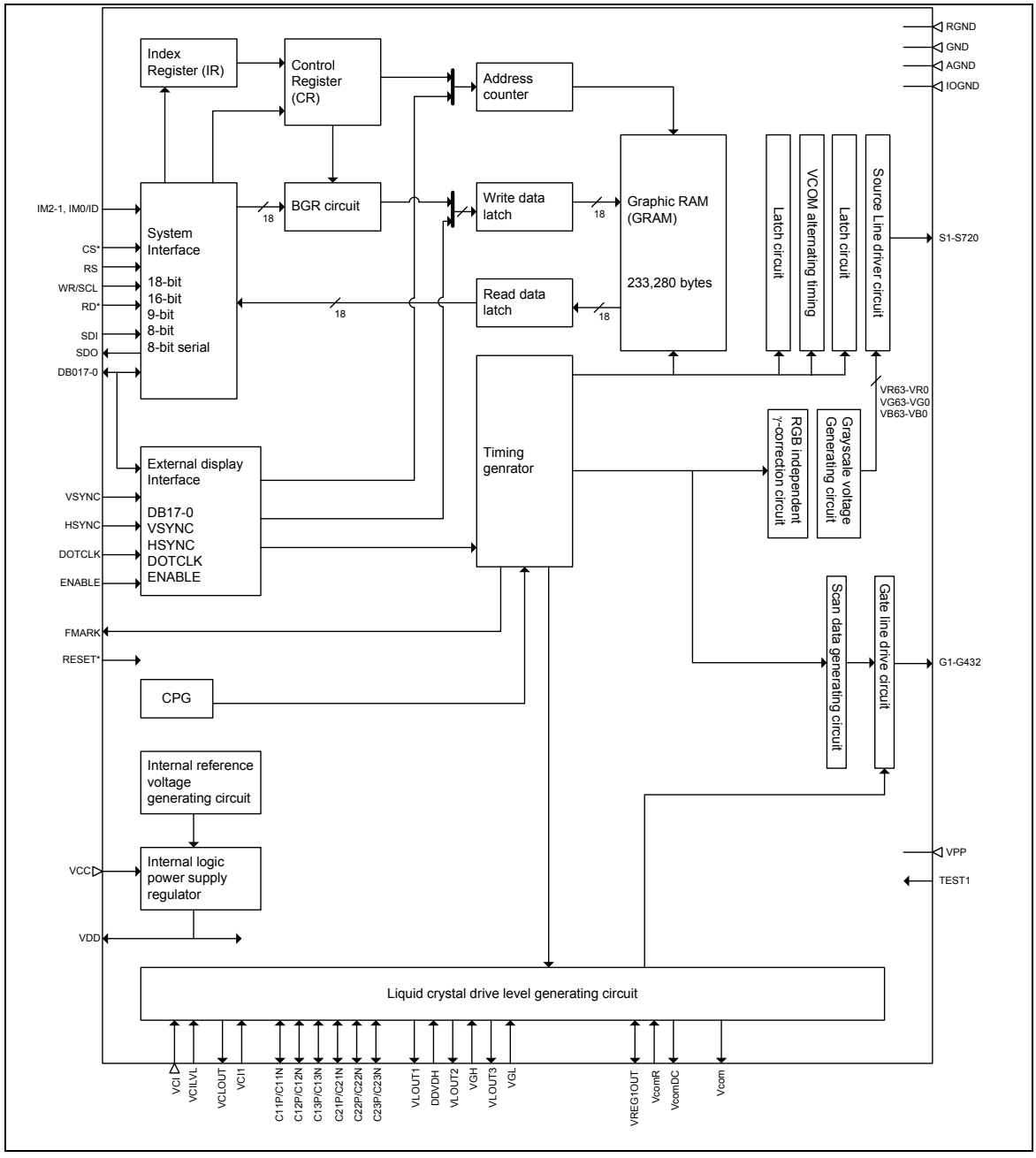


Figure 1

Pin Function

Table 1 Interface Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>IM2-1, IM0/ID</td><td>I</td><td>GND/ IOVCC1</td><td>Select a mode to interface to an MPU. In SPI mode, the IM0 pin is used to set the ID of device code.
<table>
<tr><th>IM[2:0]</th><th>Interface Mode</th><th>DB Pins</th></tr>
<tr><td>000</td><td>80-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>001</td><td>80-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>010</td><td>80-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>011</td><td>80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>11*</td><td>Clock Synchronous serial interface</td><td>SDI, SDO</td></tr>
<tr><td>10*</td><td>Setting disabled</td><td></td></tr>
</table></td></tr>
<tr><td>CS*</td><td>I</td><td>MPU</td><td>A chip select signal. Amplitude: IOVCC1-GND.
Low: LGDP4551 is selected and accessible.
High: LGDP4551 is not selected and not accessible.
Fix to the IOVCC1 level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>A register select signal. Amplitude: IOVCC1-GND.
Low: select the index/status register.
High: select a control register.
In SPI mode, fix to either IOVCC1 or GND level.</td></tr>
<tr><td>WR*/SCL</td><td>I</td><td>MPU</td><td>Outputs a write strobe signal in 80-system bus interface mode and enables an operation to write data when the signal is low.
In SPI mode, a synchronizing clock signal is output.</td></tr>
<tr><td>RD*</td><td>I</td><td>MPU</td><td>Outputs a read strobe signal in 80-system bus interface mode and enables an operation to read data when the signal is low. In SPI mode, fix to either IOVCC1 or GND level.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>A serial data input (SDI) pin in SPI mode. Data are input on the rising edge of the SCL signal. Fix to either IOVCC1 or GND level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU</td><td>A serial data output (SDO) pin in SPI mode. Data are output on the falling edge of the SCL signal. Leave open when not in use.</td></tr>
<tr><td>DB0 ~ DB17</td><td>I/O</td><td>MPU</td><td>An 18-bit parallel bidirectional data bus. Unused pins must be fixed either IOVCC1 or GND level.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU</td><td>A data enable signal in RGB interface mode.
Low: Select (accessible)
High: Not select (inaccessible)
The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVCC1 or GND level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>A frame synchronizing signal.
When VSPL = “0”, it is active low.
When VSPL = “1”, it is active high.
Fix to either IOVCC1 or GND level when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>MPU</td><td>A line synchronizing signal.
When HSPL = “0”, it is active low.
When HSPL = “1”, it is active high.
Fix to either IOVCC1 or GND level when not in use.</td></tr>
</table>

DOTCLK	I	MPU	A dot clock signal. When DPL = “0”, input data on the rising edge of DOTCLK. When DPL = “1”, input data on the falling edge of DOTCLK. Fix to either IOVCC1 or GND level when not in use.
RESET*	I	MPU or External RC circuit	A reset pin. Initializes the LGDP4551 with a low input. Be sure to execute a power-on reset after supplying power.
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal GRAM. Leave open when not in use.

Table 2 Power Supply Pins

Signal	I/O	Connected to	Function
VCC	-	Power supply	Power supply to internal logic regulator circuit: Vcc =2.5V ~ 3.3 V, Vcc ≥ IOVcc
VCI	-	Power supply	Power supply to liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
VCILVL	-	Power supply	VCILVL must be at the same electrical potential as VCI. Be sure to connect VCILVL with VCI on the FPC to prevent noise.
IOVCC1	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. Vcc ≥ IOVcc. . In case of COG, connect to VCC on the FPC if IOVCC1=VCC to prevent nosie.
VDD VDDOUT	O	Stabilizing capacitor	Internal logic regulator output to be used as a power supply to internal logic. Connect a stabilizing capacitor.
GND	-	Power supply	Internal logic GND : GND = 0V
RGND	-	Power supply	Internal RAM GND : RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
AGND	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
IOGND2	-	Power supply	GND for the interface pins : RESET*, CS*, WR*, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOGND2 = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VPP2	-	Power supply	Power supply pin for EPROM write operation. Connect to GND or open when EPROM is not used.

Table 3 Step-Up Circuit

Signal	I/O	Connected to	Function
VCIOUT	O	Stabilizing capactor, Vci1	Internal reference voltage generated between Vci and GND. The output level is set by instruction (VC).

VCI1	I	VciOUT or Vci	Reference voltage for the step-up circuit 1. Vci1 must be set to a level, which will generate the VLOUT1, VLOUT2 and VLOUT3 levels within the respective setting ranges.
VLOUT1	O	Stabilizing capacitor, DDVDH	Output from the step-up circuit 1, generated from Vci1. The step-up factor for the VLOUT1 level is set by instruction (BT). VLOUT1 = 4.5V ~ 6.0V
DDVDH	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and Vcom drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V
VLOUT2	O	Stabilizing capacitor, VGH	Output from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor for VLOUT2 is set by instruction (BT). VLOUT2 = max 15.0V
VGH	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.
VLOUT3	O	Stabilizing capacitor, VGL	Output from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor for VLOUT2 is set by instruction (BT). VLOUT3 = min –12.5V
VGL	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.
VLOUT4	O	Stabilizing capacitor, VCL	A voltage level of Vci1 x (-1) generated in the step=ip circuit 2. Connect to a stabilizing capacitor when using the VLOUT4 output.
VCL	I	VLOUT4	Power supply for operating VCOML. Vci1 is multiplied by 1 and output by internal step-up circuit 2. VCL = 0 to -3.3(V)
C11P, C11N C12P, C12N	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 1.
C13P, C13N C21P, C21N C22P, C22N C23P, C23N	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.

Table 4 LCD Drive

Signal	I/O	Connected to	Function
VREG1OUT	O	Stabilizing capacitor	Output generated from a reference voltage VciLVL by amplifying by the factor, which is set by instruction (VRH). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor when it is in use. VREG1OUT = 3.0V ~ (DDVDH – 0.5)V
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. Output AC voltage with the amplitude VCOMH and VCOML. The alternating cycle is changeable by register setting. Also Vcom output can be started and halted by register setting.
VCOMH	O	Stabilizing capacitor	Output for the high level of VCOM. This output voltage is adjusted by an instruction (VCM) setting. VCOMH = 3.0 to (DDVDH -0.5) (V)
VCOML	O	Stabilizing capacitor	Output for the low level of VCOM. This output voltage is adjusted by an instruction (VDV) setting or fixed to GND by a register (VCOMG) setting. In this case, a capacitor for stabilization is not necessary. VCOML = (VCL +0.5)to 1 (V)

VCOMR	I	Variable resistor or open	If a variable resistor is used to adjust VCOMH, it is attached to this pin. In this case, use an instruction (VCM) setting to stop the internal digital potentiometer circuit of VCOMH, and insert the variable resistor for use in adjustment of VCOM between VREG1OUT. Leave it open or connect to GND when not in use.
VGS	I	GND	Reference level for grayscale voltage generating circuit.
S1 ~ S720	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal outputs, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S720.
G1 ~ G432	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level

Table 5 Others (Test, Dummy Pins)

Signal	I/O	Connected to	Function
TEST1	I	GND	Test pin. Connect to GND.
TSC	-	-	Test pin. Connect to IOVCC1, GND or open when not in use.
TEST2-3	-	-	Test pins. Connect to IOVCC1, GND or open when not in use.
TESTO1-18	-	-	Test pins. Connect to GND or open when not in use.
V0T, V31T	-	-	Test pins. Connect to GND or open when not in use.
VTEST	-	-	Test pin. Connect to GND or open when not in use.
VREF	-	-	Test pin. Connect to GND or open when not in use.
VREFD	-	-	Test pin. Connect to GND or open when not in use.
VMON	-	-	Test pin. Connect to GND or open when not in use.
VDDTEST	-	-	Test pin. Connect to GND or open when not in use.
VREFC	-	-	Test pin. Connect to GND or open when not in use.
VIREG	-	-	Test pin. Connect to GND or open when not in use.
TESTA5	-	-	Test pin. Connect ot GND or open when not in use.
VCCDUM1	-	-	Test pin. Leave open.
VGLDMY 1-4	-	-	Dummy pins. Leave open.
IOVCC1DU M1-2	-	-	Output the IOVCC1 voltage level. These pins are internally shorted to IOVCC1. Use it to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave open.
GNDDUM1-21	-	-	Output the GND voltage level. These pins are internally shorted to GND. Use it to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave open.
AGNDDUM 1-5	-	-	Output the GND voltage level. These pins are internally shorted to GND.
IOGND2DU M1-8			Output the GND voltage level. These pins are internally shorted to GND.

DUMMYR 1-2, 5-10	-	-	Dummy pins. Leave open.
DUMMYR 3-4	-	-	DUMMYR3 and DUMMYR4 are short-circuited within the chip for COG contact resistance measurement.
VPP1	-	-	Test pin. Connect to GND or open when not in use.
VPP3A, 3B	-	-	Test pins. Connect to GND or open when not in use.
IOVCC2	-	-	Test pin. Connect to IOVCC1, GND or open when not in use.
MDDI_DATA_P_B, MDDI_DATA_M_B	-	-	Test pins. Connect to GND or open when not in use.
MDDI_STB_P_B, MDDI_STB_M_B	-	-	Test pins. Connect to GND or open when not in use.

PAD Arrangement

- Chip size : 21.46mm x 0.91mm
- Chip thickness : 320um
- PAD Coordination : PAD center
- Coordination origin : Chip center

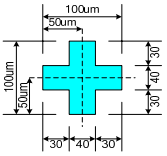
- Au BUMP size
(1) 50.00um x 80.00um
No.1 - No.299

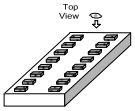
(2) 18.00um x 110.00um
No.300 - No.1467

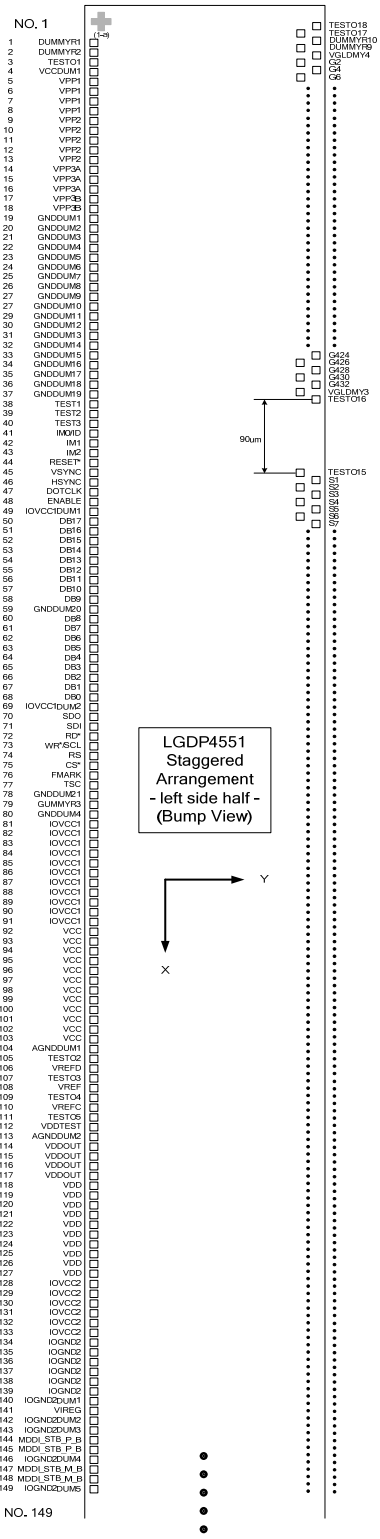
- Au BUMP pitch : see PAD coordination Table
- Au BUMP height : 15um(typ.)
- No. in the figure corresponds to No. in the PAD coordination Table

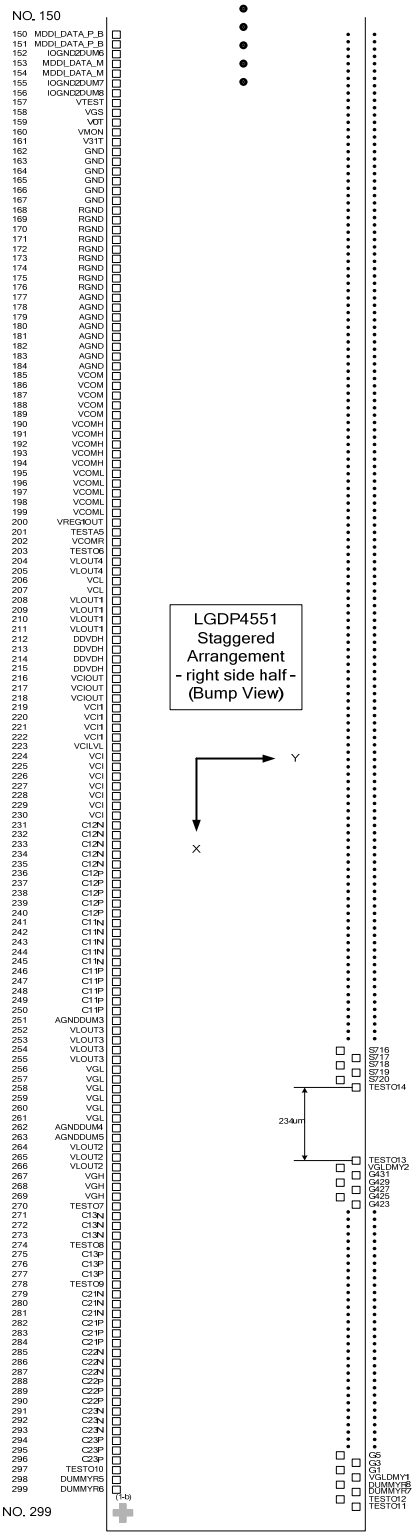
- Alignment mark

Alignment mark	X	Y
1-a	-10655	-333
1-b	10655	-333









PAD Coordinate

Pad No.	Pad Name	X	Y
1	DUMMYR1	-10430.0	-359.0
2	DUMMYR2	-10360.0	-359.0
3	TESTO1	-10290.0	-359.0
4	VCCDUM1	-10220.0	-359.0
5	VPP1	-10150.0	-359.0
6	VPP1	-10080.0	-359.0
7	VPP1	-10010.0	-359.0
8	VPP1	-9940.0	-359.0
9	VPP2	-9870.0	-359.0
10	VPP2	-9800.0	-359.0
11	VPP2	-9730.0	-359.0
12	VPP2	-9660.0	-359.0
13	VPP2	-9590.0	-359.0
14	VPP3A	-9520.0	-359.0
15	VPP3A	-9450.0	-359.0
16	VPP3A	-9380.0	-359.0
17	VPP3B	-9310.0	-359.0
18	VPP3B	-9240.0	-359.0
19	GNDDUM1	-9170.0	-359.0
20	GNDDUM2	-9100.0	-359.0
21	GNDDUM3	-9030.0	-359.0
22	GNDDUM4	-8960.0	-359.0
23	GNDDUM5	-8890.0	-359.0
24	GNDDUM6	-8820.0	-359.0
25	GNDDUM7	-8750.0	-359.0
26	GNDDUM8	-8680.0	-359.0
27	GNDDUM9	-8610.0	-359.0
28	GNDDUM10	-8540.0	-359.0
29	GNDDUM11	-8470.0	-359.0
30	GNDDUM12	-8400.0	-359.0
31	GNDDUM13	-8330.0	-359.0
32	GNDDUM14	-8260.0	-359.0
33	GNDDUM15	-8190.0	-359.0
34	GNDDUM16	-8120.0	-359.0
35	GNDDUM17	-8050.0	-359.0
36	GNDDUM18	-7980.0	-359.0
37	GNDDUM19	-7910.0	-359.0
38	TEST1	-7840.0	-359.0
39	TEST2	-7770.0	-359.0
40	TEST3	-7700.0	-359.0
41	IM0/ID	-7630.0	-359.0
42	IM1	-7560.0	-359.0
43	IM2	-7490.0	-359.0
44	RESET*	-7420.0	-359.0
45	VSYNC	-7350.0	-359.0
46	HSYNC	-7280.0	-359.0
47	DOTCLK	-7210.0	-359.0
48	ENABLE	-7140.0	-359.0
49	IOVCC1DUM1	-7070.0	-359.0
50	DB17	-7000.0	-359.0
51	DB16	-6930.0	-359.0
52	DB15	-6860.0	-359.0
53	DB14	-6790.0	-359.0
54	DB13	-6720.0	-359.0
55	DB12	-6650.0	-359.0
56	DB11	-6580.0	-359.0
57	DB10	-6510.0	-359.0
58	DB9	-6440.0	-359.0
59	GNDDUM20	-6370.0	-359.0
60	DB8	-6300.0	-359.0

Pad No.	Pad Name	X	Y
61	DB7	-6230.0	-359.0
62	DB6	-6160.0	-359.0
63	DB5	-6090.0	-359.0
64	DB4	-6020.0	-359.0
65	DB3	-5950.0	-359.0
66	DB2	-5880.0	-359.0
67	DB1	-5810.0	-359.0
68	DB0	-5740.0	-359.0
69	IOVCC1DUM2	-5670.0	-359.0
70	SDO	-5600.0	-359.0
71	SDI	-5530.0	-359.0
72	RD*	-5460.0	-359.0
73	WR*/SCL	-5390.0	-359.0
74	RS	-5320.0	-359.0
75	CS*	-5250.0	-359.0
76	FMARK	-5180.0	-359.0
77	TSC	-5110.0	-359.0
78	GNDDUM21	-5040.0	-359.0
79	DUMMYR3	-4970.0	-359.0
80	DUMMYR4	-4900.0	-359.0
81	IOVCC1	-4830.0	-359.0
82	IOVCC1	-4760.0	-359.0
83	IOVCC1	-4690.0	-359.0
84	IOVCC1	-4620.0	-359.0
85	IOVCC1	-4550.0	-359.0
86	IOVCC1	-4480.0	-359.0
87	IOVCC1	-4410.0	-359.0
88	IOVCC1	-4340.0	-359.0
89	IOVCC1	-4270.0	-359.0
90	IOVCC1	-4200.0	-359.0
91	IOVCC1	-4130.0	-359.0
92	VCC	-4060.0	-359.0
93	VCC	-3990.0	-359.0
94	VCC	-3920.0	-359.0
95	VCC	-3850.0	-359.0
96	VCC	-3780.0	-359.0
97	VCC	-3710.0	-359.0
98	VCC	-3640.0	-359.0
99	VCC	-3570.0	-359.0
100	VCC	-3500.0	-359.0
101	VCC	-3430.0	-359.0
102	VCC	-3360.0	-359.0
103	VCC	-3290.0	-359.0
104	AGNDDUM1	-3220.0	-359.0
105	TESTO2	-3150.0	-359.0
106	VREFD	-3080.0	-359.0
107	TESTO3	-3010.0	-359.0
108	VREF	-2940.0	-359.0
109	TESTO4	-2870.0	-359.0
110	VREFC	-2800.0	-359.0
111	TESTO5	-2730.0	-359.0
112	VDDTEST	-2660.0	-359.0
113	AGNDDUM2	-2590.0	-359.0
114	VDDOUT	-2520.0	-359.0
115	VDDOUT	-2450.0	-359.0
116	VDDOUT	-2380.0	-359.0
117	VDDOUT	-2310.0	-359.0
118	VDD	-2240.0	-359.0
119	VDD	-2170.0	-359.0
120	VDD	-2100.0	-359.0

Pad No.	Pad Name	X	Y
121	VDD	-2030.0	-359.0
122	VDD	-1960.0	-359.0
123	VDD	-1890.0	-359.0
124	VDD	-1820.0	-359.0
125	VDD	-1750.0	-359.0
126	VDD	-1680.0	-359.0
127	VDD	-1610.0	-359.0
128	IOVCC2	-1540.0	-359.0
129	IOVCC2	-1470.0	-359.0
130	IOVCC2	-1400.0	-359.0
131	IOVCC2	-1330.0	-359.0
132	IOVCC2	-1260.0	-359.0
133	IOVCC2	-1190.0	-359.0
134	IOGND2	-1120.0	-359.0
135	IOGND2	-1050.0	-359.0
136	IOGND2	-980.0	-359.0
137	IOGND2	-910.0	-359.0
138	IOGND2	-840.0	-359.0
139	IOGND2	-770.0	-359.0
140	IOGND2DUM1	-700.0	-359.0
141	VIREG	-630.0	-359.0
142	IOGND2DUM2	-560.0	-359.0
143	IOGND2DUM3	-490.0	-359.0
144	MDDI_STB_P_B	-420.0	-359.0
145	MDDI_STB_P_B	-350.0	-359.0
146	IOGND2DUM4	-280.0	-359.0
147	MDDI_STB_M_B	-210.0	-359.0
148	MDDI_STB_M_B	-140.0	-359.0
149	IOGND2DUM5	-70.0	-359.0
150	MDDI_DATA_P_B	0.0	-359.0
151	MDDI_DATA_P_B	70.0	-359.0
152	IOGND2DUM6	140.0	-359.0
153	MDDI_DATA_M	210.0	-359.0
154	MDDI_DATA_M	280.0	-359.0
155	IOGND2DUM7	350.0	-359.0
156	IOGND2DUM8	420.0	-359.0
157	VTEST	490.0	-359.0
158	VGS	560.0	-359.0
159	V0T	630.0	-359.0
160	VMON	700.0	-359.0
161	V31T	770.0	-359.0
162	GND	840.0	-359.0
163	GND	910.0	-359.0
164	GND	980.0	-359.0
165	GND	1050.0	-359.0
166	GND	1120.0	-359.0
167	GND	1190.0	-359.0
168	RGND	1260.0	-359.0
169	RGND	1330.0	-359.0
170	RGND	1400.0	-359.0
171	RGND	1470.0	-359.0
172	RGND	1540.0	-359.0
173	RGND	1610.0	-359.0
174	RGND	1680.0	-359.0
175	RGND	1750.0	-359.0
176	RGND	1820.0	-359.0
177	AGND	1890.0	-359.0
178	AGND	1960.0	-359.0
179	AGND	2030.0	-359.0
180	AGND	2100.0	-359.0

Pad No.	Pad Name	X	Y
181	AGND	2170.0	-359.0
182	AGND	2240.0	-359.0
183	AGND	2310.0	-359.0
184	AGND	2380.0	-359.0
185	VCOM	2450.0	-359.0
186	VCOM	2520.0	-359.0
187	VCOM	2590.0	-359.0
188	VCOM	2660.0	-359.0
189	VCOM	2730.0	-359.0
190	VCOMH	2800.0	-359.0
191	VCOMH	2870.0	-359.0
192	VCOMH	2940.0	-359.0
193	VCOMH	3010.0	-359.0
194	VCOMH	3080.0	-359.0
195	VCOML	3150.0	-359.0
196	VCOML	3220.0	-359.0
197	VCOML	3290.0	-359.0
198	VCOML	3360.0	-359.0
199	VCOML	3430.0	-359.0
200	VREG1OUT	3500.0	-359.0
201	TESTA5	3570.0	-359.0
202	VCOMR	3640.0	-359.0
203	TESTO6	3710.0	-359.0
204	VLOUT4	3780.0	-359.0
205	VLOUT4	3850.0	-359.0
206	VCL	3920.0	-359.0
207	VCL	3990.0	-359.0
208	VLOUT1	4060.0	-359.0
209	VLOUT1	4130.0	-359.0
210	VLOUT1	4200.0	-359.0
211	VLOUT1	4270.0	-359.0
212	DDVDH	4340.0	-359.0
213	DDVDH	4410.0	-359.0
214	DDVDH	4480.0	-359.0
215	DDVDH	4550.0	-359.0
216	VCIOUT	4620.0	-359.0
217	VCIOUT	4690.0	-359.0
218	VCIOUT	4760.0	-359.0
219	VCI1	4830.0	-359.0
220	VCI1	4900.0	-359.0
221	VCI1	4970.0	-359.0
222	VCI1	5040.0	-359.0
223	VCILVL	5110.0	-359.0
224	VCI	5180.0	-359.0
225	VCI	5250.0	-359.0
226	VCI	5320.0	-359.0
227	VCI	5390.0	-359.0
228	VCI	5460.0	-359.0
229	VCI	5530.0	-359.0
230	VCI	5600.0	-359.0
231	C12N	5670.0	-359.0
232	C12N	5740.0	-359.0
233	C12N	5810.0	-359.0
234	C12N	5880.0	-359.0
235	C12N	5950.0	-359.0
236	C12P	6020.0	-359.0
237	C12P	6090.0	-359.0
238	C12P	6160.0	-359.0
239	C12P	6230.0	-359.0
240	C12P	6300.0	-359.0

Pad No.	Pad Name	X	Y
241	C11N	6370.0	-359.0
242	C11N	6440.0	-359.0
243	C11N	6510.0	-359.0
244	C11N	6580.0	-359.0
245	C11N	6650.0	-359.0
246	C11P	6720.0	-359.0
247	C11P	6790.0	-359.0
248	C11P	6860.0	-359.0
249	C11P	6930.0	-359.0
250	C11P	7000.0	-359.0
251	AGNDDUM3	7070.0	-359.0
252	VLOUT3	7140.0	-359.0
253	VLOUT3	7210.0	-359.0
254	VLOUT3	7280.0	-359.0
255	VLOUT3	7350.0	-359.0
256	VGL	7420.0	-359.0
257	VGL	7490.0	-359.0
258	VGL	7560.0	-359.0
259	VGL	7630.0	-359.0
260	VGL	7700.0	-359.0
261	VGL	7770.0	-359.0
262	AGNDDUM4	7840.0	-359.0
263	AGNDDUM5	7910.0	-359.0
264	VLOUT2	7980.0	-359.0
265	VLOUT2	8050.0	-359.0
266	VLOUT2	8120.0	-359.0
267	VGH	8190.0	-359.0
268	VGH	8260.0	-359.0
269	VGH	8330.0	-359.0
270	TESTO7	8400.0	-359.0
271	C13N	8470.0	-359.0
272	C13N	8540.0	-359.0
273	C13N	8610.0	-359.0
274	TESTO8	8680.0	-359.0
275	C13P	8750.0	-359.0
276	C13P	8820.0	-359.0
277	C13P	8890.0	-359.0
278	TESTO9	8960.0	-359.0
279	C21N	9030.0	-359.0
280	C21N	9100.0	-359.0
281	C21N	9170.0	-359.0
282	C21P	9240.0	-359.0
283	C21P	9310.0	-359.0
284	C21P	9380.0	-359.0
285	C22N	9450.0	-359.0
286	C22N	9520.0	-359.0
287	C22N	9590.0	-359.0
288	C22P	9660.0	-359.0
289	C22P	9730.0	-359.0
290	C22P	9800.0	-359.0
291	C23N	9870.0	-359.0
292	C23N	9940.0	-359.0
293	C23N	10010.0	-359.0
294	C23P	10080.0	-359.0
295	C23P	10150.0	-359.0
296	C23P	10220.0	-359.0
297	TESTO10	10290.0	-359.0
298	DUMMYR5	10360.0	-359.0
299	DUMMYR6	10430.0	-359.0
300	TESTO11	10647.0	340.0

Pad No.	Pad Name	X	Y
301	TESTO12	10629.0	205.0
302	DUMMYR7	10611.0	340.0
303	DUMMYR8	10593.0	205.0
304	VGLDMY1	10575.0	340.0
305	G1	10557.0	205.0
306	G3	10539.0	340.0
307	G5	10521.0	205.0
308	G7	10503.0	340.0
309	G9	10485.0	205.0
310	G11	10467.0	340.0
311	G13	10449.0	205.0
312	G15	10431.0	340.0
313	G17	10413.0	205.0
314	G19	10395.0	340.0
315	G21	10377.0	205.0
316	G23	10359.0	340.0
317	G25	10341.0	205.0
318	G27	10323.0	340.0
319	G29	10305.0	205.0
320	G31	10287.0	340.0
321	G33	10269.0	205.0
322	G35	10251.0	340.0
323	G37	10233.0	205.0
324	G39	10215.0	340.0
325	G41	10197.0	205.0
326	G43	10179.0	340.0
327	G45	10161.0	205.0
328	G47	10143.0	340.0
329	G49	10125.0	205.0
330	G51	10107.0	340.0
331	G53	10089.0	205.0
332	G55	10071.0	340.0
333	G57	10053.0	205.0
334	G59	10035.0	340.0
335	G61	10017.0	205.0
336	G63	9999.0	340.0
337	G65	9981.0	205.0
338	G67	9963.0	340.0
339	G69	9945.0	205.0
340	G71	9927.0	340.0
341	G73	9909.0	205.0
342	G75	9891.0	340.0
343	G77	9873.0	205.0
344	G79	9855.0	340.0
345	G81	9837.0	205.0
346	G83	9819.0	340.0
347	G85	9801.0	205.0
348	G87	9783.0	340.0
349	G89	9765.0	205.0
350	G91	9747.0	340.0
351	G93	9729.0	205.0
352	G95	9711.0	340.0
353	G97	9693.0	205.0
354	G99	9675.0	340.0
355	G101	9657.0	205.0
356	G103	9639.0	340.0
357	G105	9621.0	205.0
358	G107	9603.0	340.0
359	G109	9585.0	205.0
360	G111	9567.0	340.0

Pad No.	Pad Name	X	Y
361	G113	9549.0	205.0
362	G115	9531.0	340.0
363	G117	9513.0	205.0
364	G119	9495.0	340.0
365	G121	9477.0	205.0
366	G123	9459.0	340.0
367	G125	9441.0	205.0
368	G127	9423.0	340.0
369	G129	9405.0	205.0
370	G131	9387.0	340.0
371	G133	9369.0	205.0
372	G135	9351.0	340.0
373	G137	9333.0	205.0
374	G139	9315.0	340.0
375	G141	9297.0	205.0
376	G143	9279.0	340.0
377	G145	9261.0	205.0
378	G147	9243.0	340.0
379	G149	9225.0	205.0
380	G151	9207.0	340.0
381	G153	9189.0	205.0
382	G155	9171.0	340.0
383	G157	9153.0	205.0
384	G159	9135.0	340.0
385	G161	9117.0	205.0
386	G163	9099.0	340.0
387	G165	9081.0	205.0
388	G167	9063.0	340.0
389	G169	9045.0	205.0
390	G171	9027.0	340.0
391	G173	9009.0	205.0
392	G175	8991.0	340.0
393	G177	8973.0	205.0
394	G179	8955.0	340.0
395	G181	8937.0	205.0
396	G183	8919.0	340.0
397	G185	8901.0	205.0
398	G187	8883.0	340.0
399	G189	8865.0	205.0
400	G191	8847.0	340.0
401	G193	8829.0	205.0
402	G195	8811.0	340.0
403	G197	8793.0	205.0
404	G199	8775.0	340.0
405	G201	8757.0	205.0
406	G203	8739.0	340.0
407	G205	8721.0	205.0
408	G207	8703.0	340.0
409	G209	8685.0	205.0
410	G211	8667.0	340.0
411	G213	8649.0	205.0
412	G215	8631.0	340.0
413	G217	8613.0	205.0
414	G219	8595.0	340.0
415	G221	8577.0	205.0
416	G223	8559.0	340.0
417	G225	8541.0	205.0
418	G227	8523.0	340.0
419	G229	8505.0	205.0
420	G231	8487.0	340.0

Pad No.	Pad Name	X	Y
421	G233	8469.0	205.0
422	G235	8451.0	340.0
423	G237	8433.0	205.0
424	G239	8415.0	340.0
425	G241	8397.0	205.0
426	G243	8379.0	340.0
427	G245	8361.0	205.0
428	G247	8343.0	340.0
429	G249	8325.0	205.0
430	G251	8307.0	340.0
431	G253	8289.0	205.0
432	G255	8271.0	340.0
433	G257	8253.0	205.0
434	G259	8235.0	340.0
435	G261	8217.0	205.0
436	G263	8199.0	340.0
437	G265	8181.0	205.0
438	G267	8163.0	340.0
439	G269	8145.0	205.0
440	G271	8127.0	340.0
441	G273	8109.0	205.0
442	G275	8091.0	340.0
443	G277	8073.0	205.0
444	G279	8055.0	340.0
445	G281	8037.0	205.0
446	G283	8019.0	340.0
447	G285	8001.0	205.0
448	G287	7983.0	340.0
449	G289	7965.0	205.0
450	G291	7947.0	340.0
451	G293	7929.0	205.0
452	G295	7911.0	340.0
453	G297	7893.0	205.0
454	G299	7875.0	340.0
455	G301	7857.0	205.0
456	G303	7839.0	340.0
457	G305	7821.0	205.0
458	G307	7803.0	340.0
459	G309	7785.0	205.0
460	G311	7767.0	340.0
461	G313	7749.0	205.0
462	G315	7731.0	340.0
463	G317	7713.0	205.0
464	G319	7695.0	340.0
465	G321	7677.0	205.0
466	G323	7659.0	340.0
467	G325	7641.0	205.0
468	G327	7623.0	340.0
469	G329	7605.0	205.0
470	G331	7587.0	340.0
471	G333	7569.0	205.0
472	G335	7551.0	340.0
473	G337	7533.0	205.0
474	G339	7515.0	340.0
475	G341	7497.0	205.0
476	G343	7479.0	340.0
477	G345	7461.0	205.0
478	G347	7443.0	340.0
479	G349	7425.0	205.0
480	G351	7407.0	340.0

Pad No.	Pad Name	X	Y
481	G353	7389.0	205.0
482	G355	7371.0	340.0
483	G357	7353.0	205.0
484	G359	7335.0	340.0
485	G361	7317.0	205.0
486	G363	7299.0	340.0
487	G365	7281.0	205.0
488	G367	7263.0	340.0
489	G369	7245.0	205.0
490	G371	7227.0	340.0
491	G373	7209.0	205.0
492	G375	7191.0	340.0
493	G377	7173.0	205.0
494	G379	7155.0	340.0
495	G381	7137.0	205.0
496	G383	7119.0	340.0
497	G385	7101.0	205.0
498	G387	7083.0	340.0
499	G389	7065.0	205.0
500	G391	7047.0	340.0
501	G393	7029.0	205.0
502	G395	7011.0	340.0
503	G397	6993.0	205.0
504	G399	6975.0	340.0
505	G401	6957.0	205.0
506	G403	6939.0	340.0
507	G405	6921.0	205.0
508	G407	6903.0	340.0
509	G409	6885.0	205.0
510	G411	6867.0	340.0
511	G413	6849.0	205.0
512	G415	6831.0	340.0
513	G417	6813.0	205.0
514	G419	6795.0	340.0
515	G421	6777.0	205.0
516	G423	6759.0	340.0
517	G425	6741.0	205.0
518	G427	6723.0	340.0
519	G429	6705.0	205.0
520	G431	6687.0	340.0
521	VGLDMY2	6669.0	205.0
522	TESTO13	6651.0	340.0
523	TESTO14	6417.0	340.0
524	S720	6399.0	205.0
525	S719	6381.0	340.0
526	S718	6363.0	205.0
527	S717	6345.0	340.0
528	S716	6327.0	205.0
529	S715	6309.0	340.0
530	S714	6291.0	205.0
531	S713	6273.0	340.0
532	S712	6255.0	205.0
533	S711	6237.0	340.0
534	S710	6219.0	205.0
535	S709	6201.0	340.0
536	S708	6183.0	205.0
537	S707	6165.0	340.0
538	S706	6147.0	205.0
539	S705	6129.0	340.0
540	S704	6111.0	205.0

Pad No.	Pad Name	X	Y
541	S703	6093.0	340.0
542	S702	6075.0	205.0
543	S701	6057.0	340.0
544	S700	6039.0	205.0
545	S699	6021.0	340.0
546	S698	6003.0	205.0
547	S697	5985.0	340.0
548	S696	5967.0	205.0
549	S695	5949.0	340.0
550	S694	5931.0	205.0
551	S693	5913.0	340.0
552	S692	5895.0	205.0
553	S691	5877.0	340.0
554	S690	5859.0	205.0
555	S689	5841.0	340.0
556	S688	5823.0	205.0
557	S687	5805.0	340.0
558	S686	5787.0	205.0
559	S685	5769.0	340.0
560	S684	5751.0	205.0
561	S683	5733.0	340.0
562	S682	5715.0	205.0
563	S681	5697.0	340.0
564	S680	5679.0	205.0
565	S679	5661.0	340.0
566	S678	5643.0	205.0
567	S677	5625.0	340.0
568	S676	5607.0	205.0
569	S675	5589.0	340.0
570	S674	5571.0	205.0
571	S673	5553.0	340.0
572	S672	5535.0	205.0
573	S671	5517.0	340.0
574	S670	5499.0	205.0
575	S669	5481.0	340.0
576	S668	5463.0	205.0
577	S667	5445.0	340.0
578	S666	5427.0	205.0
579	S665	5409.0	340.0
580	S664	5391.0	205.0
581	S663	5373.0	340.0
582	S662	5355.0	205.0
583	S661	5337.0	340.0
584	S660	5319.0	205.0
585	S659	5301.0	340.0
586	S658	5283.0	205.0
587	S657	5265.0	340.0
588	S656	5247.0	205.0
589	S655	5229.0	340.0
590	S654	5211.0	205.0
591	S653	5193.0	340.0
592	S652	5175.0	205.0
593	S651	5157.0	340.0
594	S650	5139.0	205.0
595	S649	5121.0	340.0
596	S648	5103.0	205.0
597	S647	5085.0	340.0
598	S646	5067.0	205.0
599	S645	5049.0	340.0
600	S644	5031.0	205.0

Pad No.	Pad Name	X	Y
601	S643	5013.0	340.0
602	S642	4995.0	205.0
603	S641	4977.0	340.0
604	S640	4959.0	205.0
605	S639	4941.0	340.0
606	S638	4923.0	205.0
607	S637	4905.0	340.0
608	S636	4887.0	205.0
609	S635	4869.0	340.0
610	S634	4851.0	205.0
611	S633	4833.0	340.0
612	S632	4815.0	205.0
613	S631	4797.0	340.0
614	S630	4779.0	205.0
615	S629	4761.0	340.0
616	S628	4743.0	205.0
617	S627	4725.0	340.0
618	S626	4707.0	205.0
619	S625	4689.0	340.0
620	S624	4671.0	205.0
621	S623	4653.0	340.0
622	S622	4635.0	205.0
623	S621	4617.0	340.0
624	S620	4599.0	205.0
625	S619	4581.0	340.0
626	S618	4563.0	205.0
627	S617	4545.0	340.0
628	S616	4527.0	205.0
629	S615	4509.0	340.0
630	S614	4491.0	205.0
631	S613	4473.0	340.0
632	S612	4455.0	205.0
633	S611	4437.0	340.0
634	S610	4419.0	205.0
635	S609	4401.0	340.0
636	S608	4383.0	205.0
637	S607	4365.0	340.0
638	S606	4347.0	205.0
639	S605	4329.0	340.0
640	S604	4311.0	205.0
641	S603	4293.0	340.0
642	S602	4275.0	205.0
643	S601	4257.0	340.0
644	S600	4239.0	205.0
645	S599	4221.0	340.0
646	S598	4203.0	205.0
647	S597	4185.0	340.0
648	S596	4167.0	205.0
649	S595	4149.0	340.0
650	S594	4131.0	205.0
651	S593	4113.0	340.0
652	S592	4095.0	205.0
653	S591	4077.0	340.0
654	S590	4059.0	205.0
655	S589	4041.0	340.0
656	S588	4023.0	205.0
657	S587	4005.0	340.0
658	S586	3987.0	205.0
659	S585	3969.0	340.0
660	S584	3951.0	205.0

Pad No.	Pad Name	X	Y
661	S583	3933.0	340.0
662	S582	3915.0	205.0
663	S581	3897.0	340.0
664	S580	3879.0	205.0
665	S579	3861.0	340.0
666	S578	3843.0	205.0
667	S577	3825.0	340.0
668	S576	3807.0	205.0
669	S575	3789.0	340.0
670	S574	3771.0	205.0
671	S573	3753.0	340.0
672	S572	3735.0	205.0
673	S571	3717.0	340.0
674	S570	3699.0	205.0
675	S569	3681.0	340.0
676	S568	3663.0	205.0
677	S567	3645.0	340.0
678	S566	3627.0	205.0
679	S565	3609.0	340.0
680	S564	3591.0	205.0
681	S563	3573.0	340.0
682	S562	3555.0	205.0
683	S561	3537.0	340.0
684	S560	3519.0	205.0
685	S559	3501.0	340.0
686	S558	3483.0	205.0
687	S557	3465.0	340.0
688	S556	3447.0	205.0
689	S555	3429.0	340.0
690	S554	3411.0	205.0
691	S553	3393.0	340.0
692	S552	3375.0	205.0
693	S551	3357.0	340.0
694	S550	3339.0	205.0
695	S549	3321.0	340.0
696	S548	3303.0	205.0
697	S547	3285.0	340.0
698	S546	3267.0	205.0
699	S545	3249.0	340.0
700	S544	3231.0	205.0
701	S543	3213.0	340.0
702	S542	3195.0	205.0
703	S541	3177.0	340.0
704	S540	3159.0	205.0
705	S539	3141.0	340.0
706	S538	3123.0	205.0
707	S537	3105.0	340.0
708	S536	3087.0	205.0
709	S535	3069.0	340.0
710	S534	3051.0	205.0
711	S533	3033.0	340.0
712	S532	3015.0	205.0
713	S531	2997.0	340.0
714	S530	2979.0	205.0
715	S529	2961.0	340.0
716	S528	2943.0	205.0
717	S527	2925.0	340.0
718	S526	2907.0	205.0
719	S525	2889.0	340.0
720	S524	2871.0	205.0

Pad No.	Pad Name	X	Y
721	S523	2853.0	340.0
722	S522	2835.0	205.0
723	S521	2817.0	340.0
724	S520	2799.0	205.0
725	S519	2781.0	340.0
726	S518	2763.0	205.0
727	S517	2745.0	340.0
728	S516	2727.0	205.0
729	S515	2709.0	340.0
730	S514	2691.0	205.0
731	S513	2673.0	340.0
732	S512	2655.0	205.0
733	S511	2637.0	340.0
734	S510	2619.0	205.0
735	S509	2601.0	340.0
736	S508	2583.0	205.0
737	S507	2565.0	340.0
738	S506	2547.0	205.0
739	S505	2529.0	340.0
740	S504	2511.0	205.0
741	S503	2493.0	340.0
742	S502	2475.0	205.0
743	S501	2457.0	340.0
744	S500	2439.0	205.0
745	S499	2421.0	340.0
746	S498	2403.0	205.0
747	S497	2385.0	340.0
748	S496	2367.0	205.0
749	S495	2349.0	340.0
750	S494	2331.0	205.0
751	S493	2313.0	340.0
752	S492	2295.0	205.0
753	S491	2277.0	340.0
754	S490	2259.0	205.0
755	S489	2241.0	340.0
756	S488	2223.0	205.0
757	S487	2205.0	340.0
758	S486	2187.0	205.0
759	S485	2169.0	340.0
760	S484	2151.0	205.0
761	S483	2133.0	340.0
762	S482	2115.0	205.0
763	S481	2097.0	340.0
764	S480	2079.0	205.0
765	S479	2061.0	340.0
766	S478	2043.0	205.0
767	S477	2025.0	340.0
768	S476	2007.0	205.0
769	S475	1989.0	340.0
770	S474	1971.0	205.0
771	S473	1953.0	340.0
772	S472	1935.0	205.0
773	S471	1917.0	340.0
774	S470	1899.0	205.0
775	S469	1881.0	340.0
776	S468	1863.0	205.0
777	S467	1845.0	340.0
778	S466	1827.0	205.0
779	S465	1809.0	340.0
780	S464	1791.0	205.0

Pad No.	Pad Name	X	Y
781	S463	1773.0	340.0
782	S462	1755.0	205.0
783	S461	1737.0	340.0
784	S460	1719.0	205.0
785	S459	1701.0	340.0
786	S458	1683.0	205.0
787	S457	1665.0	340.0
788	S456	1647.0	205.0
789	S455	1629.0	340.0
790	S454	1611.0	205.0
791	S453	1593.0	340.0
792	S452	1575.0	205.0
793	S451	1557.0	340.0
794	S450	1539.0	205.0
795	S449	1521.0	340.0
796	S448	1503.0	205.0
797	S447	1485.0	340.0
798	S446	1467.0	205.0
799	S445	1449.0	340.0
800	S444	1431.0	205.0
801	S443	1413.0	340.0
802	S442	1395.0	205.0
803	S441	1377.0	340.0
804	S440	1359.0	205.0
805	S439	1341.0	340.0
806	S438	1323.0	205.0
807	S437	1305.0	340.0
808	S436	1287.0	205.0
809	S435	1269.0	340.0
810	S434	1251.0	205.0
811	S433	1233.0	340.0
812	S432	1215.0	205.0
813	S431	1197.0	340.0
814	S430	1179.0	205.0
815	S429	1161.0	340.0
816	S428	1143.0	205.0
817	S427	1125.0	340.0
818	S426	1107.0	205.0
819	S425	1089.0	340.0
820	S424	1071.0	205.0
821	S423	1053.0	340.0
822	S422	1035.0	205.0
823	S421	1017.0	340.0
824	S420	999.0	205.0
825	S419	981.0	340.0
826	S418	963.0	205.0
827	S417	945.0	340.0
828	S416	927.0	205.0
829	S415	909.0	340.0
830	S414	891.0	205.0
831	S413	873.0	340.0
832	S412	855.0	205.0
833	S411	837.0	340.0
834	S410	819.0	205.0
835	S409	801.0	340.0
836	S408	783.0	205.0
837	S407	765.0	340.0
838	S406	747.0	205.0
839	S405	729.0	340.0
840	S404	711.0	205.0

Pad No.	Pad Name	X	Y
841	S403	693.0	340.0
842	S402	675.0	205.0
843	S401	657.0	340.0
844	S400	639.0	205.0
845	S399	621.0	340.0
846	S398	603.0	205.0
847	S397	585.0	340.0
848	S396	567.0	205.0
849	S395	549.0	340.0
850	S394	531.0	205.0
851	S393	513.0	340.0
852	S392	495.0	205.0
853	S391	477.0	340.0
854	S390	459.0	205.0
855	S389	441.0	340.0
856	S388	423.0	205.0
857	S387	405.0	340.0
858	S386	387.0	205.0
859	S385	369.0	340.0
860	S384	351.0	205.0
861	S383	333.0	340.0
862	S382	315.0	205.0
863	S381	297.0	340.0
864	S380	279.0	205.0
865	S379	261.0	340.0
866	S378	243.0	205.0
867	S377	225.0	340.0
868	S376	207.0	205.0
869	S375	189.0	340.0
870	S374	171.0	205.0
871	S373	153.0	340.0
872	S372	135.0	205.0
873	S371	117.0	340.0
874	S370	99.0	205.0
875	S369	81.0	340.0
876	S368	63.0	205.0
877	S367	45.0	340.0
878	S366	27.0	205.0
879	S365	9.0	340.0
880	S364	-9.0	205.0
881	S363	-27.0	340.0
882	S362	-45.0	205.0
883	S361	-63.0	340.0
884	S360	-81.0	205.0
885	S359	-99.0	340.0
886	S358	-117.0	205.0
887	S357	-135.0	340.0
888	S356	-153.0	205.0
889	S355	-171.0	340.0
890	S354	-189.0	205.0
891	S353	-207.0	340.0
892	S352	-225.0	205.0
893	S351	-243.0	340.0
894	S350	-261.0	205.0
895	S349	-279.0	340.0
896	S348	-297.0	205.0
897	S347	-315.0	340.0
898	S346	-333.0	205.0
899	S345	-351.0	340.0
900	S344	-369.0	205.0

Pad No.	Pad Name	X	Y
901	S343	-387.0	340.0
902	S342	-405.0	205.0
903	S341	-423.0	340.0
904	S340	-441.0	205.0
905	S339	-459.0	340.0
906	S338	-477.0	205.0
907	S337	-495.0	340.0
908	S336	-513.0	205.0
909	S335	-531.0	340.0
910	S334	-549.0	205.0
911	S333	-567.0	340.0
912	S332	-585.0	205.0
913	S331	-603.0	340.0
914	S330	-621.0	205.0
915	S329	-639.0	340.0
916	S328	-657.0	205.0
917	S327	-675.0	340.0
918	S326	-693.0	205.0
919	S325	-711.0	340.0
920	S324	-729.0	205.0
921	S323	-747.0	340.0
922	S322	-765.0	205.0
923	S321	-783.0	340.0
924	S320	-801.0	205.0
925	S319	-819.0	340.0
926	S318	-837.0	205.0
927	S317	-855.0	340.0
928	S316	-873.0	205.0
929	S315	-891.0	340.0
930	S314	-909.0	205.0
931	S313	-927.0	340.0
932	S312	-945.0	205.0
933	S311	-963.0	340.0
934	S310	-981.0	205.0
935	S309	-999.0	340.0
936	S308	-1017.0	205.0
937	S307	-1035.0	340.0
938	S306	-1053.0	205.0
939	S305	-1071.0	340.0
940	S304	-1089.0	205.0
941	S303	-1107.0	340.0
942	S302	-1125.0	205.0
943	S301	-1143.0	340.0
944	S300	-1161.0	205.0
945	S299	-1179.0	340.0
946	S298	-1197.0	205.0
947	S297	-1215.0	340.0
948	S296	-1233.0	205.0
949	S295	-1251.0	340.0
950	S294	-1269.0	205.0
951	S293	-1287.0	340.0
952	S292	-1305.0	205.0
953	S291	-1323.0	340.0
954	S290	-1341.0	205.0
955	S289	-1359.0	340.0
956	S288	-1377.0	205.0
957	S287	-1395.0	340.0
958	S286	-1413.0	205.0
959	S285	-1431.0	340.0
960	S284	-1449.0	205.0

Pad No.	Pad Name	X	Y
961	S283	-1467.0	340.0
962	S282	-1485.0	205.0
963	S281	-1503.0	340.0
964	S280	-1521.0	205.0
965	S279	-1539.0	340.0
966	S278	-1557.0	205.0
967	S277	-1575.0	340.0
968	S276	-1593.0	205.0
969	S275	-1611.0	340.0
970	S274	-1629.0	205.0
971	S273	-1647.0	340.0
972	S272	-1665.0	205.0
973	S271	-1683.0	340.0
974	S270	-1701.0	205.0
975	S269	-1719.0	340.0
976	S268	-1737.0	205.0
977	S267	-1755.0	340.0
978	S266	-1773.0	205.0
979	S265	-1791.0	340.0
980	S264	-1809.0	205.0
981	S263	-1827.0	340.0
982	S262	-1845.0	205.0
983	S261	-1863.0	340.0
984	S260	-1881.0	205.0
985	S259	-1899.0	340.0
986	S258	-1917.0	205.0
987	S257	-1935.0	340.0
988	S256	-1953.0	205.0
989	S255	-1971.0	340.0
990	S254	-1989.0	205.0
991	S253	-2007.0	340.0
992	S252	-2025.0	205.0
993	S251	-2043.0	340.0
994	S250	-2061.0	205.0
995	S249	-2079.0	340.0
996	S248	-2097.0	205.0
997	S247	-2115.0	340.0
998	S246	-2133.0	205.0
999	S245	-2151.0	340.0
1000	S244	-2169.0	205.0
1001	S243	-2187.0	340.0
1002	S242	-2205.0	205.0
1003	S241	-2223.0	340.0
1004	S240	-2241.0	205.0
1005	S239	-2259.0	340.0
1006	S238	-2277.0	205.0
1007	S237	-2295.0	340.0
1008	S236	-2313.0	205.0
1009	S235	-2331.0	340.0
1010	S234	-2349.0	205.0
1011	S233	-2367.0	340.0
1012	S232	-2385.0	205.0
1013	S231	-2403.0	340.0
1014	S230	-2421.0	205.0
1015	S229	-2439.0	340.0
1016	S228	-2457.0	205.0
1017	S227	-2475.0	340.0
1018	S226	-2493.0	205.0
1019	S225	-2511.0	340.0
1020	S224	-2529.0	205.0

Pad No.	Pad Name	X	Y
1021	S223	-2547.0	340.0
1022	S222	-2565.0	205.0
1023	S221	-2583.0	340.0
1024	S220	-2601.0	205.0
1025	S219	-2619.0	340.0
1026	S218	-2637.0	205.0
1027	S217	-2655.0	340.0
1028	S216	-2673.0	205.0
1029	S215	-2691.0	340.0
1030	S214	-2709.0	205.0
1031	S213	-2727.0	340.0
1032	S212	-2745.0	205.0
1033	S211	-2763.0	340.0
1034	S210	-2781.0	205.0
1035	S209	-2799.0	340.0
1036	S208	-2817.0	205.0
1037	S207	-2835.0	340.0
1038	S206	-2853.0	205.0
1039	S205	-2871.0	340.0
1040	S204	-2889.0	205.0
1041	S203	-2907.0	340.0
1042	S202	-2925.0	205.0
1043	S201	-2943.0	340.0
1044	S200	-2961.0	205.0
1045	S199	-2979.0	340.0
1046	S198	-2997.0	205.0
1047	S197	-3015.0	340.0
1048	S196	-3033.0	205.0
1049	S195	-3051.0	340.0
1050	S194	-3069.0	205.0
1051	S193	-3087.0	340.0
1052	S192	-3105.0	205.0
1053	S191	-3123.0	340.0
1054	S190	-3141.0	205.0
1055	S189	-3159.0	340.0
1056	S188	-3177.0	205.0
1057	S187	-3195.0	340.0
1058	S186	-3213.0	205.0
1059	S185	-3231.0	340.0
1060	S184	-3249.0	205.0
1061	S183	-3267.0	340.0
1062	S182	-3285.0	205.0
1063	S181	-3303.0	340.0
1064	S180	-3321.0	205.0
1065	S179	-3339.0	340.0
1066	S178	-3357.0	205.0
1067	S177	-3375.0	340.0
1068	S176	-3393.0	205.0
1069	S175	-3411.0	340.0
1070	S174	-3429.0	205.0
1071	S173	-3447.0	340.0
1072	S172	-3465.0	205.0
1073	S171	-3483.0	340.0
1074	S170	-3501.0	205.0
1075	S169	-3519.0	340.0
1076	S168	-3537.0	205.0
1077	S167	-3555.0	340.0
1078	S166	-3573.0	205.0
1079	S165	-3591.0	340.0
1080	S164	-3609.0	205.0

Pad No.	Pad Name	X	Y
1081	S163	-3627.0	340.0
1082	S162	-3645.0	205.0
1083	S161	-3663.0	340.0
1084	S160	-3681.0	205.0
1085	S159	-3699.0	340.0
1086	S158	-3717.0	205.0
1087	S157	-3735.0	340.0
1088	S156	-3753.0	205.0
1089	S155	-3771.0	340.0
1090	S154	-3789.0	205.0
1091	S153	-3807.0	340.0
1092	S152	-3825.0	205.0
1093	S151	-3843.0	340.0
1094	S150	-3861.0	205.0
1095	S149	-3879.0	340.0
1096	S148	-3897.0	205.0
1097	S147	-3915.0	340.0
1098	S146	-3933.0	205.0
1099	S145	-3951.0	340.0
1100	S144	-3969.0	205.0
1101	S143	-3987.0	340.0
1102	S142	-4005.0	205.0
1103	S141	-4023.0	340.0
1104	S140	-4041.0	205.0
1105	S139	-4059.0	340.0
1106	S138	-4077.0	205.0
1107	S137	-4095.0	340.0
1108	S136	-4113.0	205.0
1109	S135	-4131.0	340.0
1110	S134	-4149.0	205.0
1111	S133	-4167.0	340.0
1112	S132	-4185.0	205.0
1113	S131	-4203.0	340.0
1114	S130	-4221.0	205.0
1115	S129	-4239.0	340.0
1116	S128	-4257.0	205.0
1117	S127	-4275.0	340.0
1118	S126	-4293.0	205.0
1119	S125	-4311.0	340.0
1120	S124	-4329.0	205.0
1121	S123	-4347.0	340.0
1122	S122	-4365.0	205.0
1123	S121	-4383.0	340.0
1124	S120	-4401.0	205.0
1125	S119	-4419.0	340.0
1126	S118	-4437.0	205.0
1127	S117	-4455.0	340.0
1128	S116	-4473.0	205.0
1129	S115	-4491.0	340.0
1130	S114	-4509.0	205.0
1131	S113	-4527.0	340.0
1132	S112	-4545.0	205.0
1133	S111	-4563.0	340.0
1134	S110	-4581.0	205.0
1135	S109	-4599.0	340.0
1136	S108	-4617.0	205.0
1137	S107	-4635.0	340.0
1138	S106	-4653.0	205.0
1139	S105	-4671.0	340.0
1140	S104	-4689.0	205.0

Pad No.	Pad Name	X	Y
1141	S103	-4707.0	340.0
1142	S102	-4725.0	205.0
1143	S101	-4743.0	340.0
1144	S100	-4761.0	205.0
1145	S99	-4779.0	340.0
1146	S98	-4797.0	205.0
1147	S97	-4815.0	340.0
1148	S96	-4833.0	205.0
1149	S95	-4851.0	340.0
1150	S94	-4869.0	205.0
1151	S93	-4887.0	340.0
1152	S92	-4905.0	205.0
1153	S91	-4923.0	340.0
1154	S90	-4941.0	205.0
1155	S89	-4959.0	340.0
1156	S88	-4977.0	205.0
1157	S87	-4995.0	340.0
1158	S86	-5013.0	205.0
1159	S85	-5031.0	340.0
1160	S84	-5049.0	205.0
1161	S83	-5067.0	340.0
1162	S82	-5085.0	205.0
1163	S81	-5103.0	340.0
1164	S80	-5121.0	205.0
1165	S79	-5139.0	340.0
1166	S78	-5157.0	205.0
1167	S77	-5175.0	340.0
1168	S76	-5193.0	205.0
1169	S75	-5211.0	340.0
1170	S74	-5229.0	205.0
1171	S73	-5247.0	340.0
1172	S72	-5265.0	205.0
1173	S71	-5283.0	340.0
1174	S70	-5301.0	205.0
1175	S69	-5319.0	340.0
1176	S68	-5337.0	205.0
1177	S67	-5355.0	340.0
1178	S66	-5373.0	205.0
1179	S65	-5391.0	340.0
1180	S64	-5409.0	205.0
1181	S63	-5427.0	340.0
1182	S62	-5445.0	205.0
1183	S61	-5463.0	340.0
1184	S60	-5481.0	205.0
1185	S59	-5499.0	340.0
1186	S58	-5517.0	205.0
1187	S57	-5535.0	340.0
1188	S56	-5553.0	205.0
1189	S55	-5571.0	340.0
1190	S54	-5589.0	205.0
1191	S53	-5607.0	340.0
1192	S52	-5625.0	205.0
1193	S51	-5643.0	340.0
1194	S50	-5661.0	205.0
1195	S49	-5679.0	340.0
1196	S48	-5697.0	205.0
1197	S47	-5715.0	340.0
1198	S46	-5733.0	205.0
1199	S45	-5751.0	340.0
1200	S44	-5769.0	205.0

Pad No.	Pad Name	X	Y
1201	S43	-5787.0	340.0
1202	S42	-5805.0	205.0
1203	S41	-5823.0	340.0
1204	S40	-5841.0	205.0
1205	S39	-5859.0	340.0
1206	S38	-5877.0	205.0
1207	S37	-5895.0	340.0
1208	S36	-5913.0	205.0
1209	S35	-5931.0	340.0
1210	S34	-5949.0	205.0
1211	S33	-5967.0	340.0
1212	S32	-5985.0	205.0
1213	S31	-6003.0	340.0
1214	S30	-6021.0	205.0
1215	S29	-6039.0	340.0
1216	S28	-6057.0	205.0
1217	S27	-6075.0	340.0
1218	S26	-6093.0	205.0
1219	S25	-6111.0	340.0
1220	S24	-6129.0	205.0
1221	S23	-6147.0	340.0
1222	S22	-6165.0	205.0
1223	S21	-6183.0	340.0
1224	S20	-6201.0	205.0
1225	S19	-6219.0	340.0
1226	S18	-6237.0	205.0
1227	S17	-6255.0	340.0
1228	S16	-6273.0	205.0
1229	S15	-6291.0	340.0
1230	S14	-6309.0	205.0
1231	S13	-6327.0	340.0
1232	S12	-6345.0	205.0
1233	S11	-6363.0	340.0
1234	S10	-6381.0	205.0
1235	S9	-6399.0	340.0
1236	S8	-6417.0	205.0
1237	S7	-6435.0	340.0
1238	S6	-6453.0	205.0
1239	S5	-6471.0	340.0
1240	S4	-6489.0	205.0
1241	S3	-6507.0	340.0
1242	S2	-6525.0	205.0
1243	S1	-6543.0	340.0
1244	TESTO15	-6561.0	205.0
1245	TESTO16	-6651.0	340.0
1246	VGLDMY3	-6669.0	205.0
1247	G432	-6687.0	340.0
1248	G430	-6705.0	205.0
1249	G428	-6723.0	340.0
1250	G426	-6741.0	205.0
1251	G424	-6759.0	340.0
1252	G422	-6777.0	205.0
1253	G420	-6795.0	340.0
1254	G418	-6813.0	205.0
1255	G416	-6831.0	340.0
1256	G414	-6849.0	205.0
1257	G412	-6867.0	340.0
1258	G410	-6885.0	205.0
1259	G408	-6903.0	340.0
1260	G406	-6921.0	205.0

Pad No.	Pad Name	X	Y
1261	G404	-6939.0	340.0
1262	G402	-6957.0	205.0
1263	G400	-6975.0	340.0
1264	G398	-6993.0	205.0
1265	G396	-7011.0	340.0
1266	G394	-7029.0	205.0
1267	G392	-7047.0	340.0
1268	G390	-7065.0	205.0
1269	G388	-7083.0	340.0
1270	G386	-7101.0	205.0
1271	G384	-7119.0	340.0
1272	G382	-7137.0	205.0
1273	G380	-7155.0	340.0
1274	G378	-7173.0	205.0
1275	G376	-7191.0	340.0
1276	G374	-7209.0	205.0
1277	G372	-7227.0	340.0
1278	G370	-7245.0	205.0
1279	G368	-7263.0	340.0
1280	G366	-7281.0	205.0
1281	G364	-7299.0	340.0
1282	G362	-7317.0	205.0
1283	G360	-7335.0	340.0
1284	G358	-7353.0	205.0
1285	G356	-7371.0	340.0
1286	G354	-7389.0	205.0
1287	G352	-7407.0	340.0
1288	G350	-7425.0	205.0
1289	G348	-7443.0	340.0
1290	G346	-7461.0	205.0
1291	G344	-7479.0	340.0
1292	G342	-7497.0	205.0
1293	G340	-7515.0	340.0
1294	G338	-7533.0	205.0
1295	G336	-7551.0	340.0
1296	G334	-7569.0	205.0
1297	G332	-7587.0	340.0
1298	G330	-7605.0	205.0
1299	G328	-7623.0	340.0
1300	G326	-7641.0	205.0
1301	G324	-7659.0	340.0
1302	G322	-7677.0	205.0
1303	G320	-7695.0	340.0
1304	G318	-7713.0	205.0
1305	G316	-7731.0	340.0
1306	G314	-7749.0	205.0
1307	G312	-7767.0	340.0
1308	G310	-7785.0	205.0
1309	G308	-7803.0	340.0
1310	G306	-7821.0	205.0
1311	G304	-7839.0	340.0
1312	G302	-7857.0	205.0
1313	G300	-7875.0	340.0
1314	G298	-7893.0	205.0
1315	G296	-7911.0	340.0
1316	G294	-7929.0	205.0
1317	G292	-7947.0	340.0
1318	G290	-7965.0	205.0
1319	G288	-7983.0	340.0
1320	G286	-8001.0	205.0

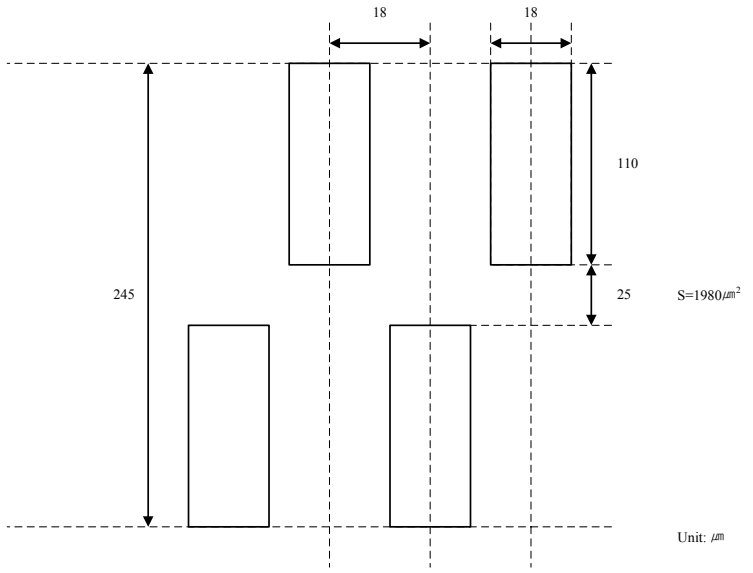
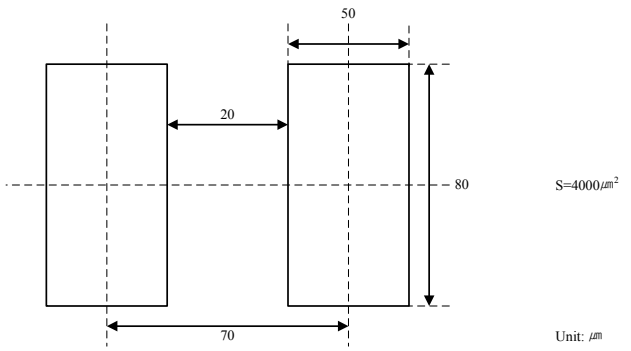
Pad No.	Pad Name	X	Y
1321	G284	-8019.0	340.0
1322	G282	-8037.0	205.0
1323	G280	-8055.0	340.0
1324	G278	-8073.0	205.0
1325	G276	-8091.0	340.0
1326	G274	-8109.0	205.0
1327	G272	-8127.0	340.0
1328	G270	-8145.0	205.0
1329	G268	-8163.0	340.0
1330	G266	-8181.0	205.0
1331	G264	-8199.0	340.0
1332	G262	-8217.0	205.0
1333	G260	-8235.0	340.0
1334	G258	-8253.0	205.0
1335	G256	-8271.0	340.0
1336	G254	-8289.0	205.0
1337	G252	-8307.0	340.0
1338	G250	-8325.0	205.0
1339	G248	-8343.0	340.0
1340	G246	-8361.0	205.0
1341	G244	-8379.0	340.0
1342	G242	-8397.0	205.0
1343	G240	-8415.0	340.0
1344	G238	-8433.0	205.0
1345	G236	-8451.0	340.0
1346	G234	-8469.0	205.0
1347	G232	-8487.0	340.0
1348	G230	-8505.0	205.0
1349	G228	-8523.0	340.0
1350	G226	-8541.0	205.0
1351	G224	-8559.0	340.0
1352	G222	-8577.0	205.0
1353	G220	-8595.0	340.0
1354	G218	-8613.0	205.0
1355	G216	-8631.0	340.0
1356	G214	-8649.0	205.0
1357	G212	-8667.0	340.0
1358	G210	-8685.0	205.0
1359	G208	-8703.0	340.0
1360	G206	-8721.0	205.0
1361	G204	-8739.0	340.0
1362	G202	-8757.0	205.0
1363	G200	-8775.0	340.0
1364	G198	-8793.0	205.0
1365	G196	-8811.0	340.0
1366	G194	-8829.0	205.0
1367	G192	-8847.0	340.0
1368	G190	-8865.0	205.0
1369	G188	-8883.0	340.0
1370	G186	-8901.0	205.0
1371	G184	-8919.0	340.0
1372	G182	-8937.0	205.0
1373	G180	-8955.0	340.0
1374	G178	-8973.0	205.0
1375	G176	-8991.0	340.0
1376	G174	-9009.0	205.0
1377	G172	-9027.0	340.0
1378	G170	-9045.0	205.0
1379	G168	-9063.0	340.0
1380	G166	-9081.0	205.0

Pad No.	Pad Name	X	Y
1381	G164	-9099.0	340.0
1382	G162	-9117.0	205.0
1383	G160	-9135.0	340.0
1384	G158	-9153.0	205.0
1385	G156	-9171.0	340.0
1386	G154	-9189.0	205.0
1387	G152	-9207.0	340.0
1388	G150	-9225.0	205.0
1389	G148	-9243.0	340.0
1390	G146	-9261.0	205.0
1391	G144	-9279.0	340.0
1392	G142	-9297.0	205.0
1393	G140	-9315.0	340.0
1394	G138	-9333.0	205.0
1395	G136	-9351.0	340.0
1396	G134	-9369.0	205.0
1397	G132	-9387.0	340.0
1398	G130	-9405.0	205.0
1399	G128	-9423.0	340.0
1400	G126	-9441.0	205.0
1401	G124	-9459.0	340.0
1402	G122	-9477.0	205.0
1403	G120	-9495.0	340.0
1404	G118	-9513.0	205.0
1405	G116	-9531.0	340.0
1406	G114	-9549.0	205.0
1407	G112	-9567.0	340.0
1408	G110	-9585.0	205.0
1409	G108	-9603.0	340.0
1410	G106	-9621.0	205.0
1411	G104	-9639.0	340.0
1412	G102	-9657.0	205.0
1413	G100	-9675.0	340.0
1414	G98	-9693.0	205.0
1415	G96	-9711.0	340.0
1416	G94	-9729.0	205.0
1417	G92	-9747.0	340.0
1418	G90	-9765.0	205.0
1419	G88	-9783.0	340.0
1420	G86	-9801.0	205.0
1421	G84	-9819.0	340.0
1422	G82	-9837.0	205.0
1423	G80	-9855.0	340.0
1424	G78	-9873.0	205.0
1425	G76	-9891.0	340.0
1426	G74	-9909.0	205.0
1427	G72	-9927.0	340.0
1428	G70	-9945.0	205.0
1429	G68	-9963.0	340.0
1430	G66	-9981.0	205.0
1431	G64	-9999.0	340.0
1432	G62	-10017.0	205.0
1433	G60	-10035.0	340.0
1434	G58	-10053.0	205.0
1435	G56	-10071.0	340.0
1436	G54	-10089.0	205.0
1437	G52	-10107.0	340.0
1438	G50	-10125.0	205.0
1439	G48	-10143.0	340.0
1440	G46	-10161.0	205.0

1446	G34	-10269.0	205.0
1447	G32	-10287.0	340.0
1448	G30	-10305.0	205.0
1449	G28	-10323.0	340.0
1450	G26	-10341.0	205.0
1451	G24	-10359.0	340.0
1452	G22	-10377.0	205.0
1453	G20	-10395.0	340.0
1454	G18	-10413.0	205.0
1455	G16	-10431.0	340.0
1456	G14	-10449.0	205.0
1457	G12	-10467.0	340.0
1458	G10	-10485.0	205.0
1459	G8	-10503.0	340.0
1460	G6	-10521.0	205.0
1461	G4	-10539.0	340.0
1462	G2	-10557.0	205.0
1463	VGLDMY4	-10575.0	340.0
1464	DUMMYR9	-10593.0	205.0
1465	DUMMYR10	-10611.0	340.0
1466	TESTO17	-10629.0	205.0
1467	TESTO18	-10647.0	340.0

Alignment mark	X	Y
1-a	-10655.0	-333.0
1-b	10655.0	-333.0

Bump Arrangement

S1 ~ S720 G1 ~ G432 DUMMYR7 ~ 10 TESTO11 ~ 18 VGLDMY1 ~ 4 (No. 300 ~ No. 1467)	
I/O PINS (No. 1 ~ No. 299)	

Block Function

System Interface

The LGDP4551 supports 2-system high-speed interfaces: 80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and a Serial Peripheral Interface (SPI). The interface mode is selected by setting the IM[2:0] pins.

The LGDP4551 has a 16-bit index register (IR); an 18-bit write-data register (WDR); and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the LGDP4551 read the first data from the internal GRAM. Valid data are read out after the LGDP4551 performs the second read operation.

Instructions are written consecutively as the instruction execution time except starting oscillator takes 0 clock cycle.

Table 6 Register Selection (80-system 8-/9-/16-/18-bit Parallel Interface)

80-system I/F			**Function**
WR*	**RD***	**RS**	
0	1	0	Write an index to IR
1	0	0	Read an internal status
0	1	1	Write to control registers or the internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 7 Register Selection (Serial Peripheral Interface)

Start Byte (SPI)		**Function**
R/W	**RS**	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

External Display Interface

The LGDP4551 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB[17:0]) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section.

The LGDP4551 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 233,280 (240 x 432x 18bit) bytes, using 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Register" section.

Timing Generator

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

LGDP4551 generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

LCD Driver Circuit

The LCD driver circuit of the LGDP4551 consists of a 720-output source driver (S1 ~ S720) and a 240-output gate driver (G1~G432). Display pattern data are latched when the 720th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

Internal logic power supply regulator

The internal logic power supply regulator generates internal logic power supply VDD.

GRAM Address MAP

Table 8 GRAM address and display panel position (SS = “0”, BGR = “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	…	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G432	“00000”H			“00001”H			“00002”H			“00003”H			…	“000EC”H			“000ED”H			“000EE”H			“000EF”H		
G2	G431	“00100”H			“00101”H			“00102”H			“00103”H			…	“001EC”H			“001ED”H			“001EE”H			“001EF”H		
G3	G430	“00200”H			“00201”H			“00202”H			“00203”H			…	“002EC”H			“002ED”H			“002EE”H			“002EF”H		
G4	G429	“00300”H			“00301”H			“00302”H			“00303”H			…	“003EC”H			“003ED”H			“003EE”H			“003EF”H		
G5	G428	“00400”H			“00401”H			“00402”H			“00403”H			…	“004EC”H			“004ED”H			“004EE”H			“004EF”H		
G6	G427	“00500”H			“00501”H			“00502”H			“00503”H			…	“005EC”H			“005ED”H			“005EE”H			“005EF”H		
G7	G426	“00600”H			“00601”H			“00602”H			“00603”H			…	“006EC”H			“006ED”H			“006EE”H			“006EF”H		
G8	G425	“00700”H			“00701”H			“00702”H			“00703”H			…	“007EC”H			“007ED”H			“007EE”H			“007EF”H		
G9	G424	“00800”H			“00801”H			“00802”H			“00803”H			…	“008EC”H			“008ED”H			“008EE”H			“008EF”H		
G10	G423	“00900”H			“00901”H			“00902”H			“00903”H			…	“009EC”H			“009ED”H			“009EE”H			“009EF”H		
G11	G422	“00A00”H			“00A01”H			“00A02”H			“00A03”H			…	“00AEC”H			“00AED”H			“00AEE”H			“00AEF”H		
G12	G421	“00B00”H			“00B01”H			“00B02”H			“00B03”H			…	“00BEC”H			“00BED”H			“00BEE”H			“00BEF”H		
G13	G420	“00C00”H			“00C01”H			“00C02”H			“00C03”H			…	“00CEC”H			“00CED”H			“00CEE”H			“00CEF”H		
G14	G419	“00D00”H			“00D01”H			“00D02”H			“00D03”H			…	“00DEC”H			“00DED”H			“00DEE”H			“00DEF”H		
G15	G418	“00E00”H			“00E01”H			“00E02”H			“00E03”H			…	“00EEC”H			“00EED”H			“00EEE”H			“00EEF”H		
G16	G417	“00F00”H			“00F01”H			“00F02”H			“00F03”H			…	“00FEC”H			“00FED”H			“00FEE”H			“00FEF”H		
G17	G416	“01000”H			“01001”H			“01002”H			“01003”H			…	“010EC”H			“010ED”H			“010EE”H			“010EF”H		
G18	G415	“01100”H			“01101”H			“01102”H			“01103”H			…	“011EC”H			“011ED”H			“011EE”H			“011EF”H		
G19	G414	“01200”H			“01201”H			“01202”H			“01203”H			…	“012EC”H			“012ED”H			“012EE”H			“012EF”H		
G20	G413	“01300”H			“01301”H			“1302”H			“01303”H			…	“013EC”H			“013ED”H			“013EE”H			“013EF”H		
:	:	:			:			:			:			…	:			:			:			:		
:	:	:			:			:			:			…	:			:			:			:		
G425	G8	“1A800”H			“1A801”H			“1A802”H			“1A803”H			…	“1A8EC”H			“1A8ED”H			“1A8EE”H			“1A8EF”H		
G426	G7	“1A900”H			“1A901”H			“1A902”H			“1A903”H			…	“1A9EC”H			“1A9ED”H			“1A9EE”H			“1A9EF”H		
G427	G6	“1AA00”H			“1AA01”H			“1AA02”H			“1AA03”H			…	“1AAEC”H			“1AAED”H			“1AAEE”H			“1AAEF”H		
G428	G5	“1AB00”H			“1AB01”H			“1AB02”H			“1AB03”H			…	“1ABEC”H			“1ABED”H			“1ABEE”H			“1ABEF”H		
G429	G4	“1AC00”H			“1AC01”H			“1AC02”H			“1AC03”H			…	“1ACEC”H			“1ACED”H			“1ACEE”H			“1ACEF”H		
G430	G3	“1AD00”H			“1AD01”H			“1AD02”H			“1AD03”H			…	“1ADEC”H			“1ADED”H			“1ADEE”H			“1ADEF”H		
G431	G2	“1AE00”H			“1AE01”H			“1AE02”H			“1AE03”H			…	“1AEEC”H			“1AEED”H			“1AEEE”H			“1AEEF”H		
G432	G1	“1AF00”H			“1AF01”H			“1AF02”H			“1AF03”H			…	“1AFEC”H			“1AFED”H			“1AFEE”H			“1AFEF”H		

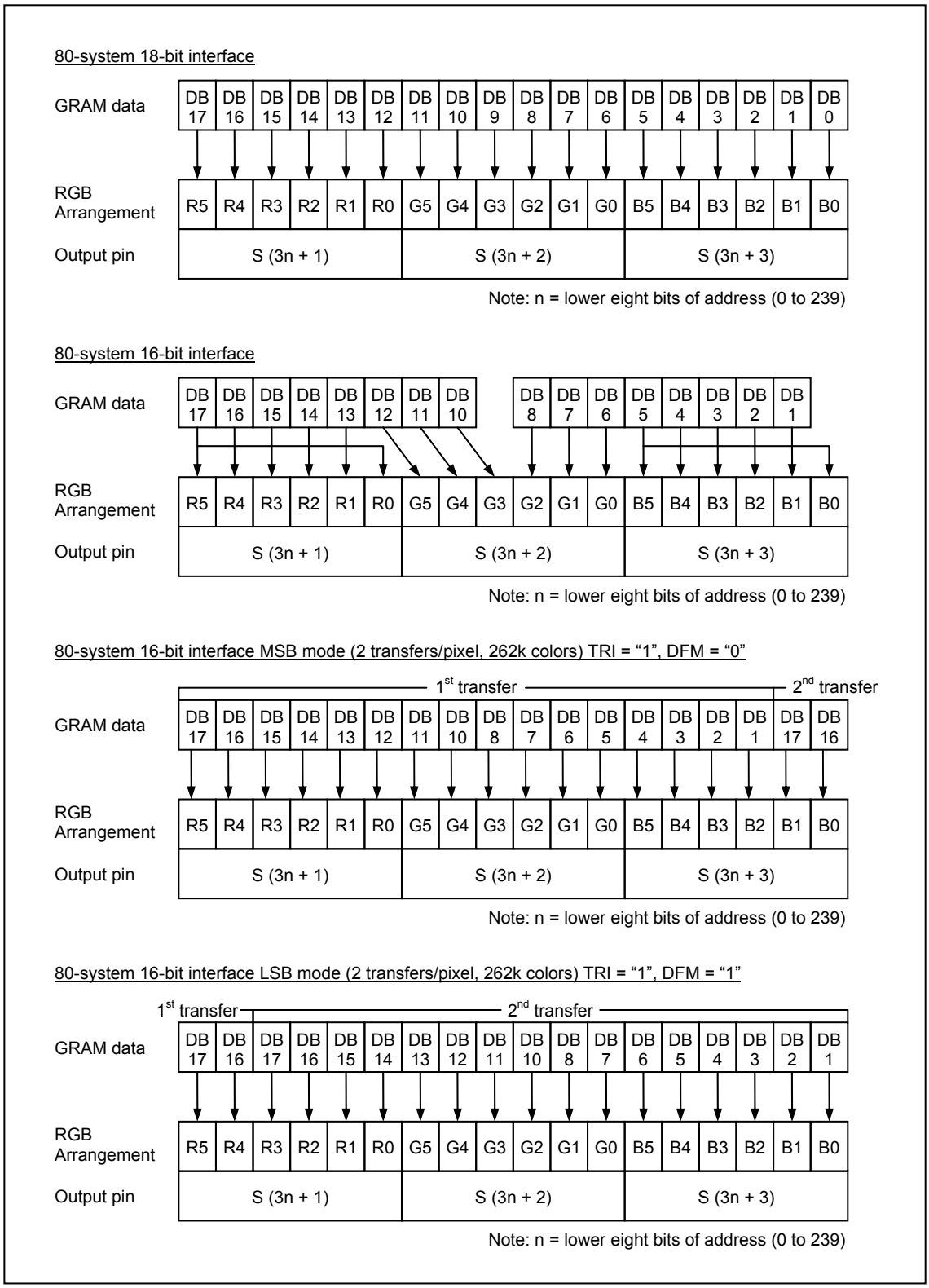
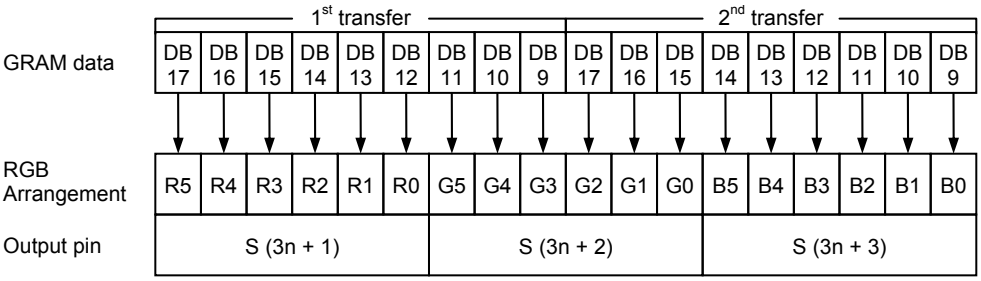


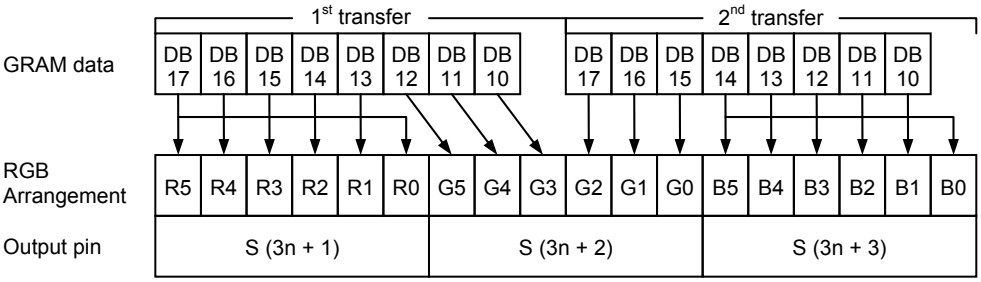
Figure 2 GRAM data and display data: system interface (SS = "0", BGR = "0")

80-system 9-bit interface (2 transfers, 262k colors)



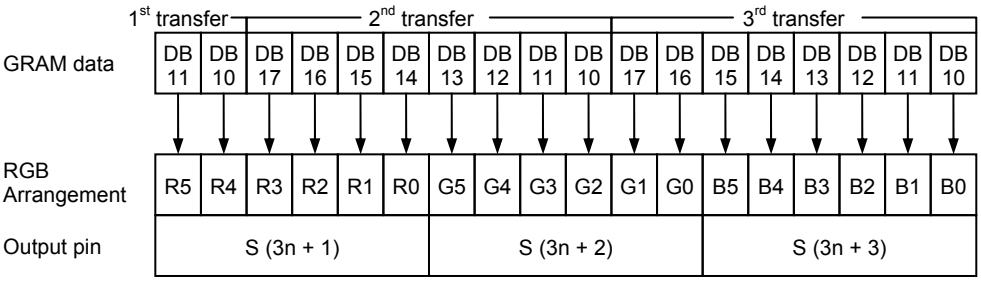
Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface or SPI (2 transfers, 65k colors) TRI = "0"



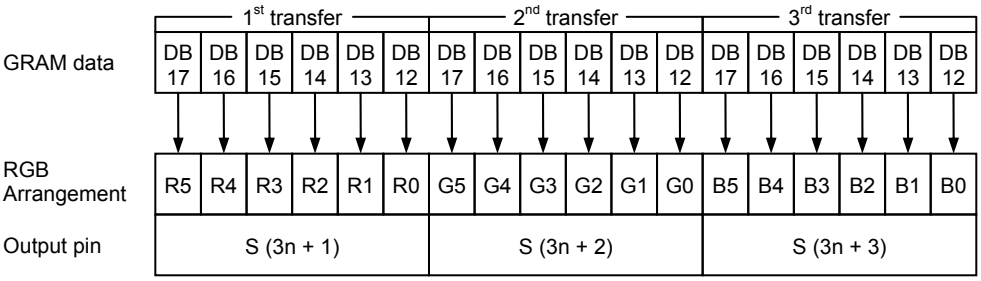
Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface (3 transfers/pixel, 262k colors) TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface (3 transfers/pixel, 262k colors) TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 239)

Figure 3 GRAM data and isplay data: system interface (SS = "0", BGR = "0")

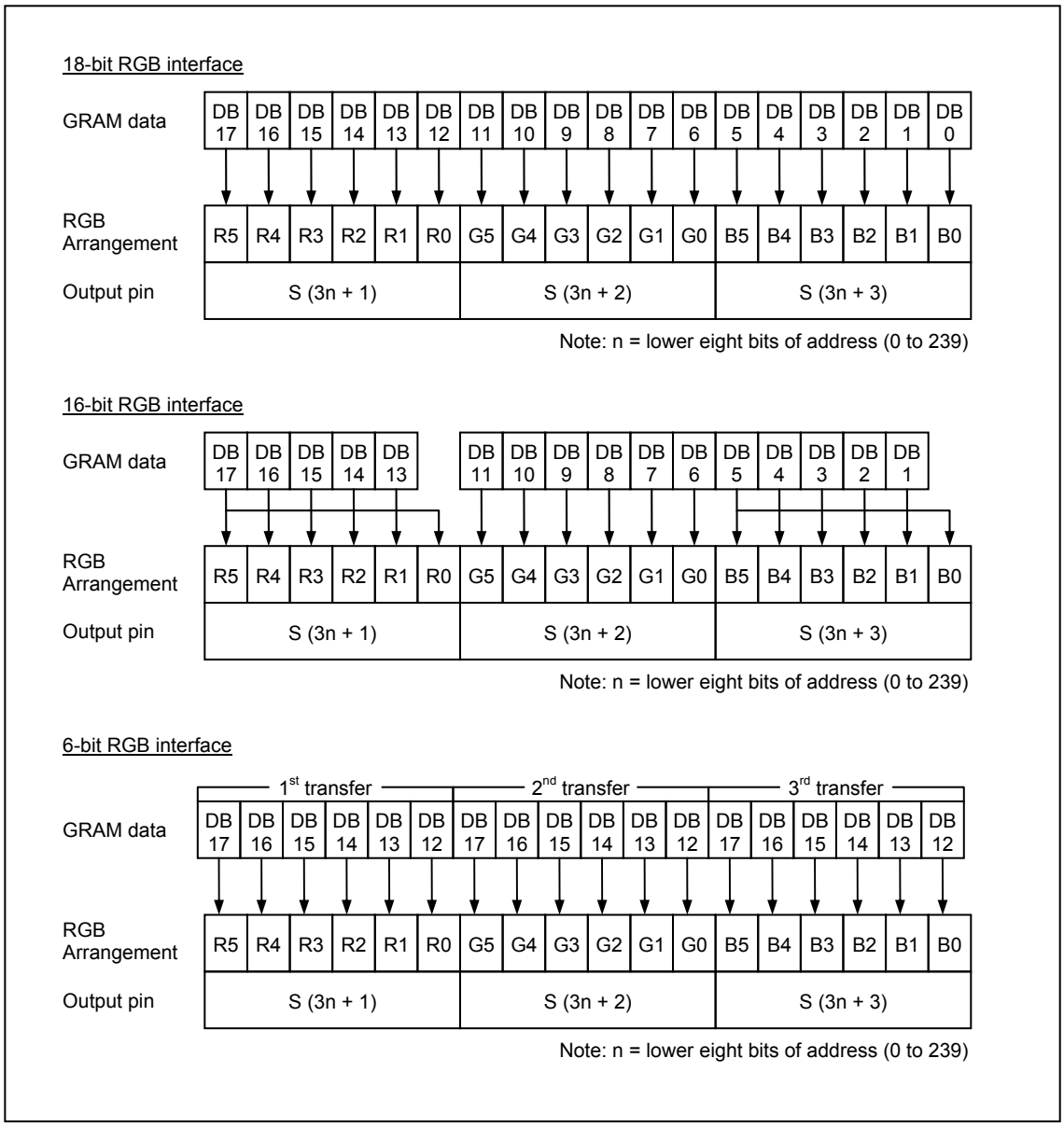


Figure 4 GRAM data and display data: system interface (SS = "0", BGR = "0")

Table 9 GRAM address and display panel position (SS = "1", BGR = "1")

S/G pin		S720	S719	S718	S717	S716	S715	S714	S713	S712	S711	S710	S709	…	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G432	"00000"H			"00001"H			"00002"H			"00003"H			…	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G431	"00100"H			"00101"H			"00102"H			"00103"H			…	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G430	"00200"H			"00201"H			"00202"H			"00203"H			…	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G429	"00300"H			"00301"H			"00302"H			"00303"H			…	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G428	"00400"H			"00401"H			"00402"H			"00403"H			…	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G427	"00500"H			"00501"H			"00502"H			"00503"H			…	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G426	"00600"H			"00601"H			"00602"H			"00603"H			…	"006EC"H			"006ED"H			"006EE"H			"006EF"H		
G8	G425	"00700"H			"00701"H			"00702"H			"00703"H			…	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G424	"00800"H			"00801"H			"00802"H			"00803"H			…	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G423	"00900"H			"00901"H			"00902"H			"00903"H			…	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G422	"00A00"H			"00A01"H			"00A02"H			"00A03"H			…	"00AEC"H			"00AED"H			"00AEE"H			"00AEF"H		
G12	G421	"00B00"H			"00B01"H			"00B02"H			"00B03"H			…	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G420	"00C00"H			"00C01"H			"00C02"H			"00C03"H			…	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G419	"00D00"H			"00D01"H			"00D02"H			"00D03"H			…	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G418	"00E00"H			"00E01"H			"00E02"H			"00E03"H			…	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G417	"00F00"H			"00F01"H			"00F02"H			"00F03"H			…	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G416	"01000"H			"01001"H			"01002"H			"01003"H			…	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G415	"01100"H			"01101"H			"01102"H			"01103"H			…	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G414	"01200"H			"01201"H			"01202"H			"01203"H			…	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G413	"01300"H			"01301"H			"1302"H			"01303"H			…	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
:	:	:			:			:			:			…	:			:			:			:		
:	:	:			:			:			:			…	:			:			:			:		
G425	G8	"1A800"H			"1A801"H			"1A802"H			"1A803"H			…	"1A8EC"H			"1A8ED"H			"1A8EE"H			"1A8EF"H		
G426	G7	"1A900"H			"1A901"H			"1A902"H			"1A903"H			…	"1A9EC"H			"1A9ED"H			"1A9EE"H			"1A9EF"H		
G427	G6	"1AA00"H			"1AA01"H			"1AA02"H			"1AA03"H			…	"1AAEC"H			"1AAED"H			"1AAEE"H			"1AAEF"H		
G428	G5	"1AB00"H			"1AB01"H			"1AB02"H			"1AB03"H			…	"1ABEC"H			"1ABED"H			"1ABEE"H			"1ABEF"H		
G429	G4	"1AC00"H			"1AC01"H			"1AC02"H			"1AC03"H			…	"1ACEC"H			"1ACED"H			"1ACEE"H			"1ACEF"H		
G430	G3	"1AD00"H			"1AD01"H			"1AD02"H			"1AD03"H			…	"1ADEC"H			"1ADED"H			"1ADEE"H			"1ADEF"H		
G431	G2	"1AE00"H			"1AE01"H			"1AE02"H			"1AE03"H			…	"1AEEC"H			"1AEED"H			"1AEEE"H			"1AEEF"H		
G432	G1	"1AF00"H			"1AF01"H			"1AF02"H			"1AF03"H			…	"1AFEC"H			"1AFED"H			"1AFEE"H			"1AFEF"H		

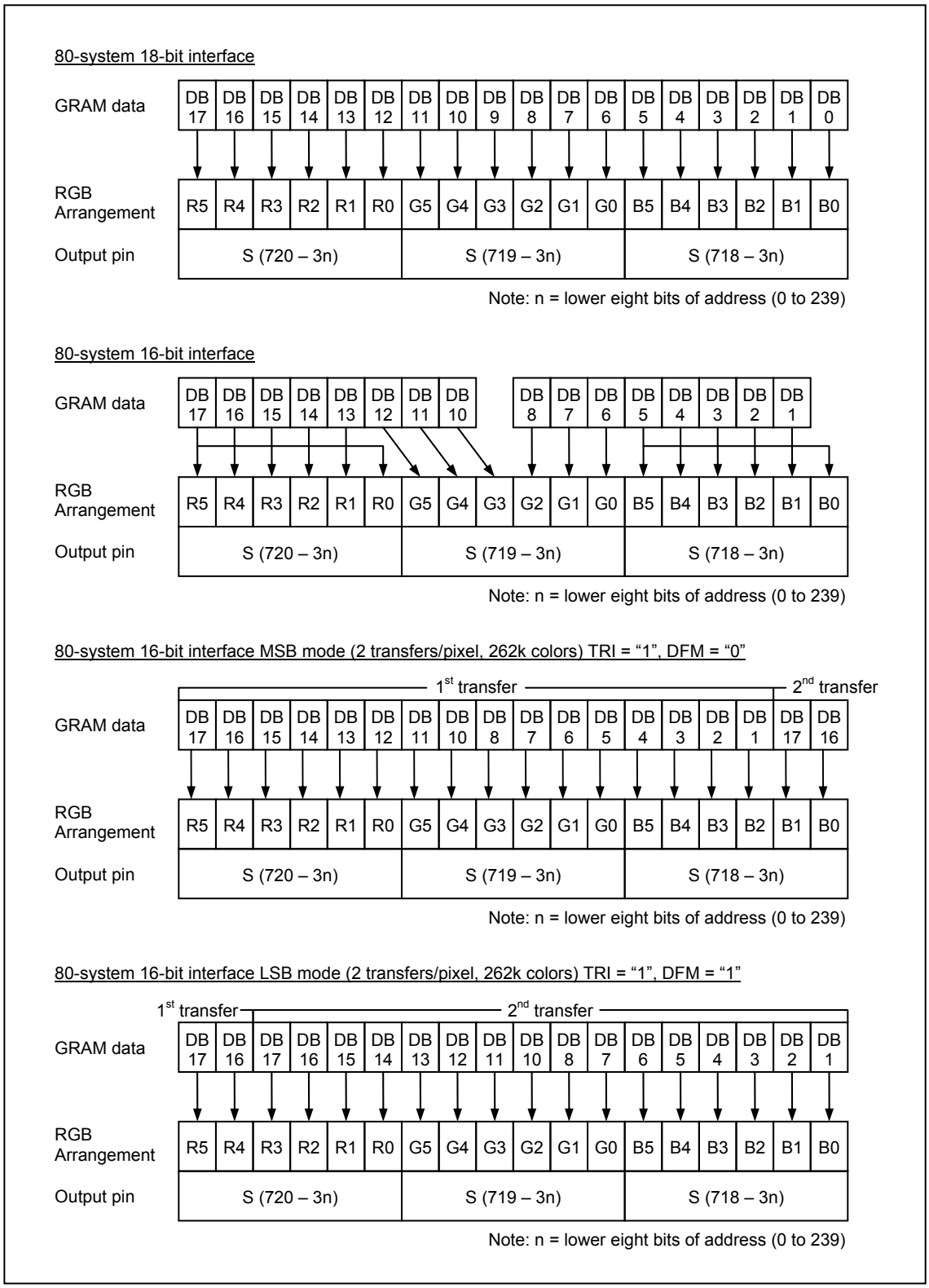
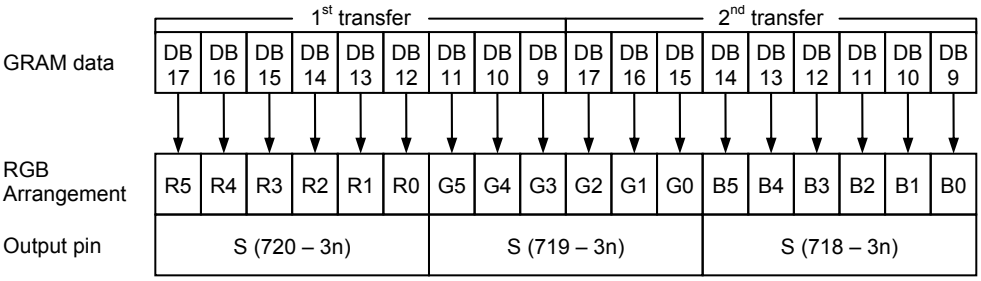


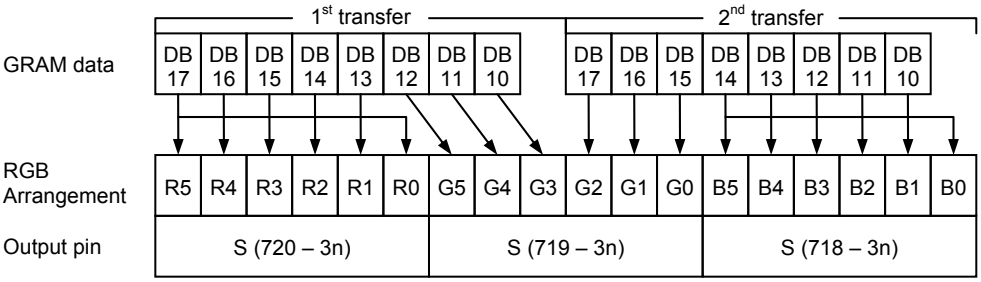
Figure 5 GRAM data and display data: system interface (SS = "1", BGR = "1")

80-system 9-bit interface (2 transfers, 262k colors)



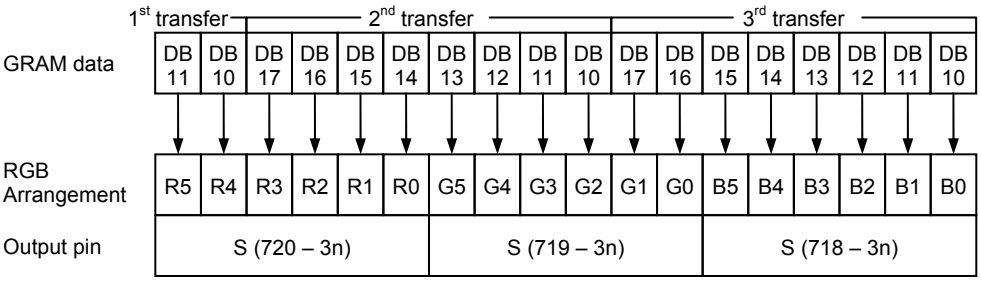
Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface or SPI (2 transfers, 65k colors) TRI = "0"



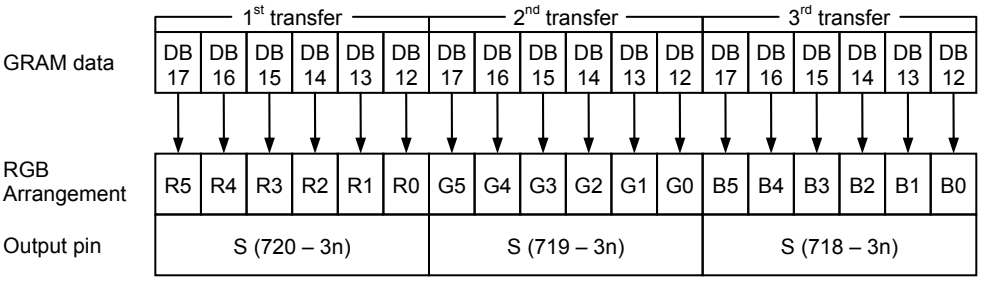
Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface (3 transfers/pixel, 262k colors) TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface (3 transfers/pixel, 262k colors) TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 239)

Figure 6 GRAM data and display data: system interface (SS = "1", BGR = "1")

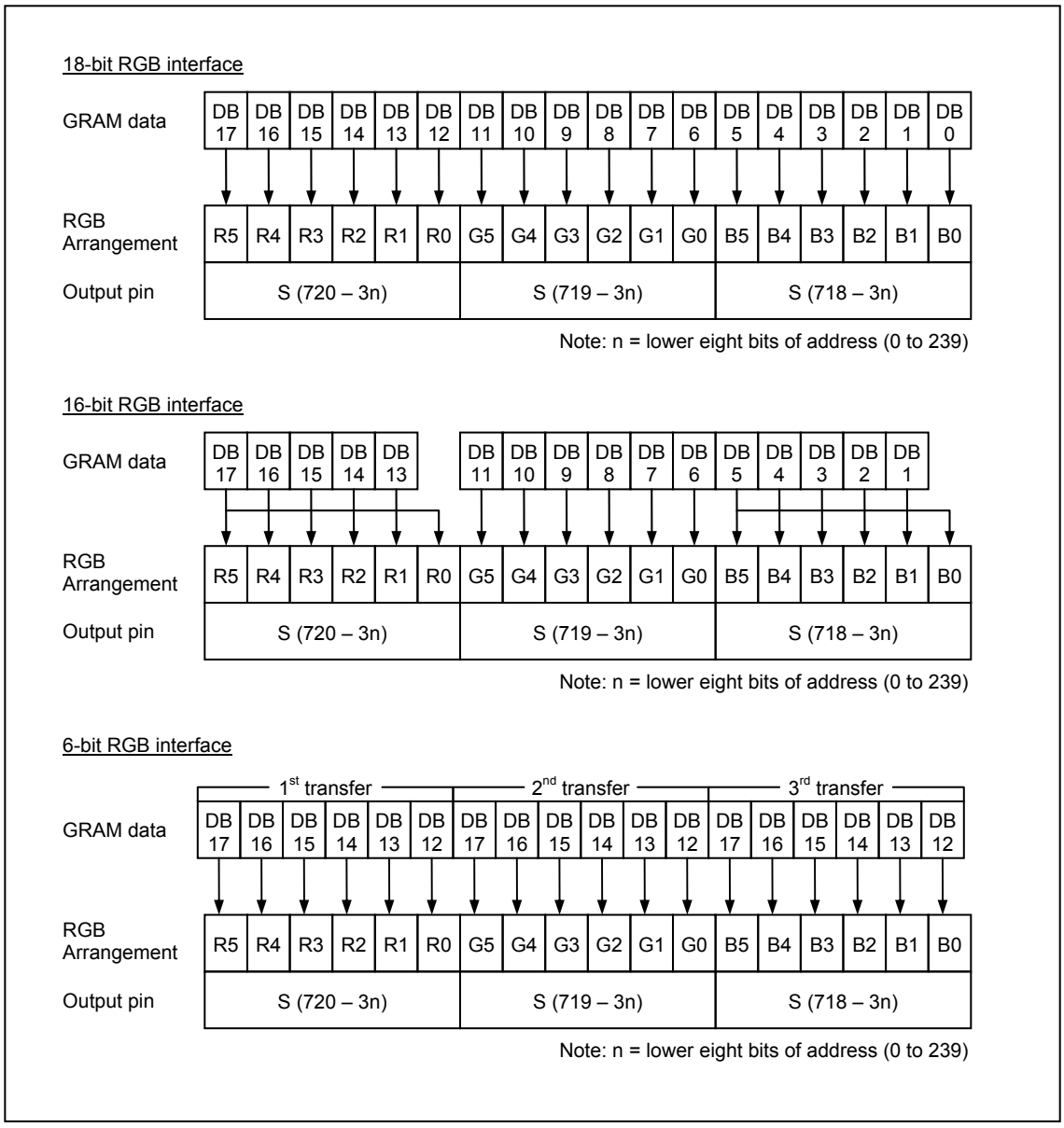


Figure 7 GRAM data and display data: system interface (SS = "1", BGR = "1")

Instructions

Outline

The LGDP4551 adopts 18-bit bus architecture to interface to a high-performance microcomputer. The LGDP4551 starts internal processing after storing control information of externally sent 18-, 16-, 9-, 8-bit data in the instruction register (IR) and the data register (DR). Since internal operations of the LGDP4551 are controlled by the signals sent from the microcomputer, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 to IB0) are called instructions. The LGDP4551 use the 18-bit format internally for operations involving internal GRAM access. The instructions of the LGDP4551 are categorized into the following groups.

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

Normally, the instruction for writing data to the internal GRAM is used the most often. Since the LGDP4551 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there is less load on the program in the microcomputer. Since instructions are executed in 0 cycles, it is possible to write instructions consecutively.

Instruction Data Format

Note that as the following figure shows, the assignment of 16 instruction bits(IB15-0) to the data bus differs in different interface operations. Write instruction according to the data transfer format of the interface in use.

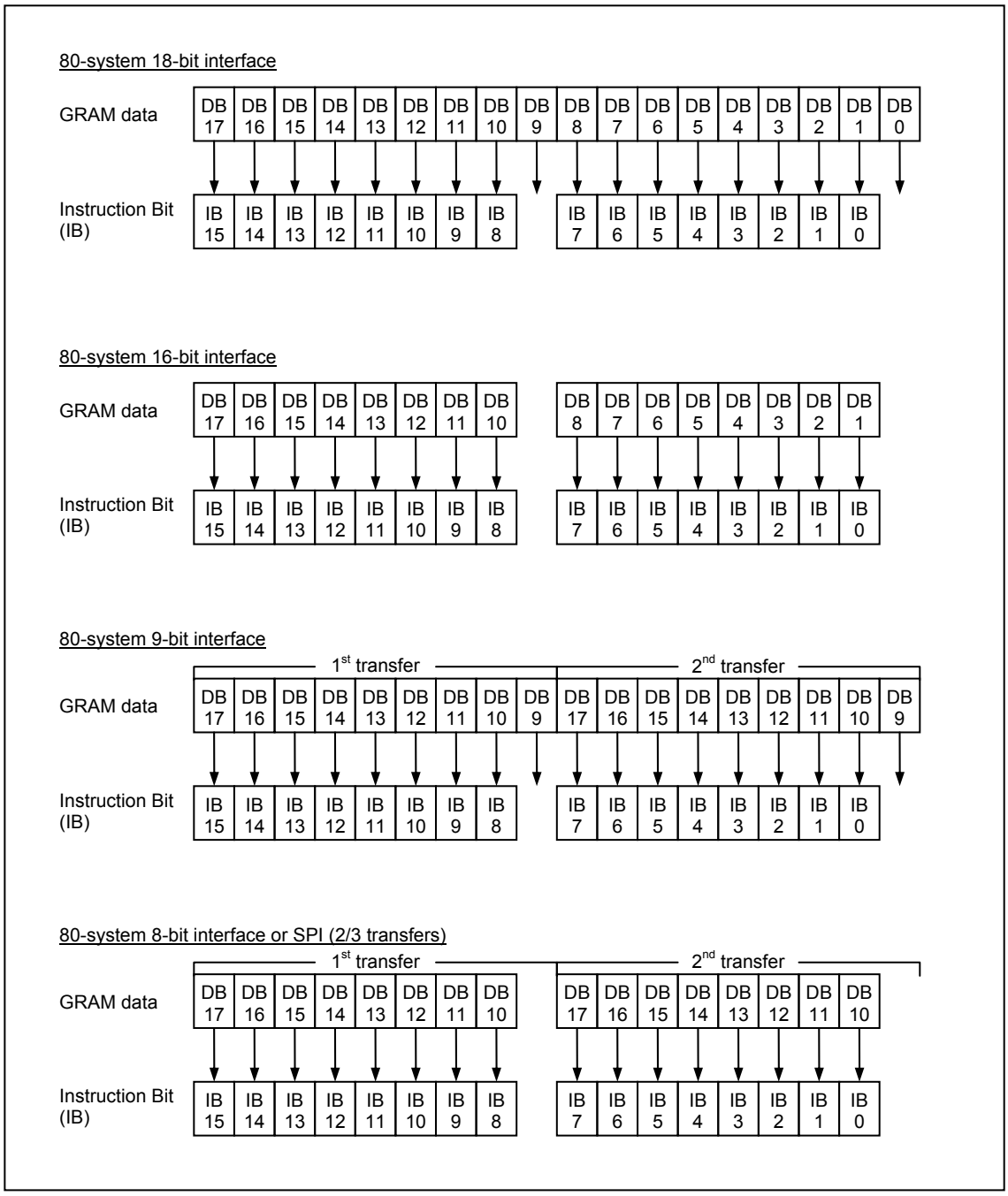


Figure 8 Instruction bits

Instruction Description

The following are detailed explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h - RFFh) of a control register or RAM control to be accessed using binary numbers “0000_0000” to “1111_1111”. An access to the register as well as instruction bits contained in it is disabled unless its index is represented in this register.

Device code read (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	0	1

The device code “4551”H is read out when reading out this register forcibly.

Driver output control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS – Selects the shift direction of outputs from the source pins.

If SS = “0”, the source pins output from S1 to S720.
If SS = “1”, the source pins output from S720 to S1.

The combination of SS and BGR bits controls the order of assigning RGB dots to the source driver pins S1 to S720.

If SS = “0” and BGR = “0”, RGB dots are assigned interchangeably from S1 to S720.
If SS = “1” and BGR = “1”, RGB dots are assigned interchangeably from S720 to S1.

When changing SS or BGR bits, RAM data must be rewritten.

SM – Sets gate driver assignment in combination with the GS bit according to the LC module. See “Scan mode setting”.

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	BC0	EOR	0	0	NW[5:0]					

NW[5:0] – Specify n, the number of raster-rows from 1 to 64, where alternations occurs every n+1 raster-rows when C-pattern waveform is generatd(BC0=1).

EOR – When EOR=1, alternation occured by applying EOR(Exclusive OR) operatin to an odd/even frame selecting signal and n-raster-row inversion signal while a C-patten waveform is generated(BC0=1).

This instruction is used when liquid crystal alternation drive is not available due to combination of numbers of LCD raster-rows and the value of "x n". For details, see n-raster-row Inversion Alternating Drive.

BC0 – Selects the liquid crystal drive waveform VCOM. See "Line Inversion AC Drive" for details.
BC0 = 0: frame inversion waveform is selected.
BC0 = 1: Line inversion waveform is selected.
In either liquid crystal drive method, the polarity inversion is halted in blank periods (back and front porch periods).

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D[1:0]		AM	0	EPF[1:0]	

The LGDP4551 modifies data sent from a microcomputer before writing them to the internal GRAM in order to write the GRAM data in high speed and reduce software processing load on the microcomputer. See "Graphics Operation Function" for details.

TRI – Selects the RAM data transfer mode in 80-system 8-bit/16-bit bus interface operation.
In 8-bit interface operation,
TRI = 0: 16-bit RAM data is transferred in two transfers.
TRI = 1: 18-bit RAM data is transferred in three transfers.
In 16-bit bus interface operation,
TRI = 0: 16-bit RAM data is transferred in one transfer.
TRI = 1: 18-bit RAM data is transferred in two transfers.
Make sure TRI = 0 when not using either 16-bit or 8-bit interface. Also, set TRI = 0 during read operation.

DFM – Sets the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.

Table 10

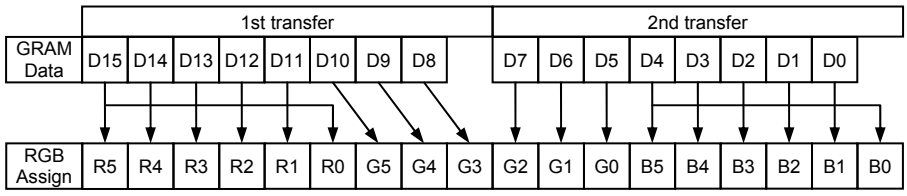
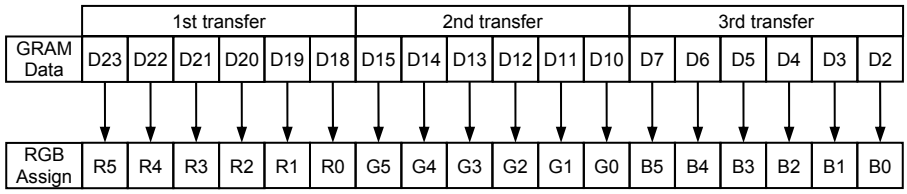
<table>
<tr><th>TRI</th><th>DFM</th><th>RAM write data transfer via serial peripheral interface (SPI)</th></tr>
<tr><td>0</td><td>*</td><td>SPI (2 transfers/pixel) – 65k colors available
 
</td></tr>
<tr><td>1</td><td>0</td><td>SPI (3 transfers/pixel) – 262k colors available
 
</td></tr>
<tr><td>1</td><td>1</td><td>Setting disabled</td></tr>
</table>

Table 11

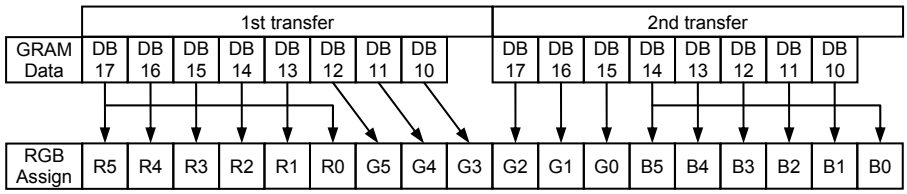
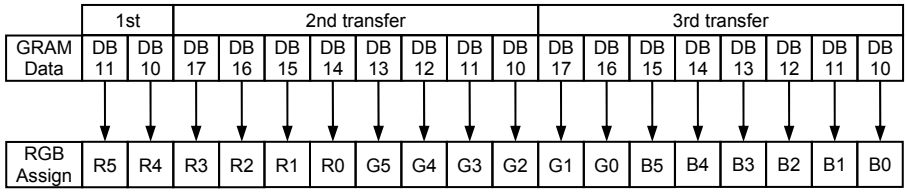
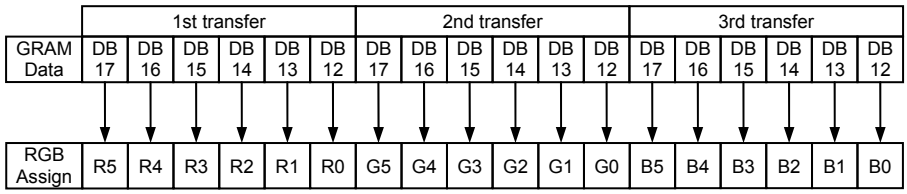
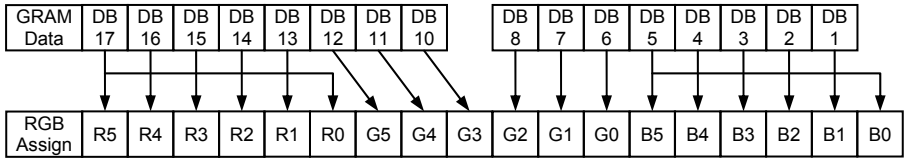
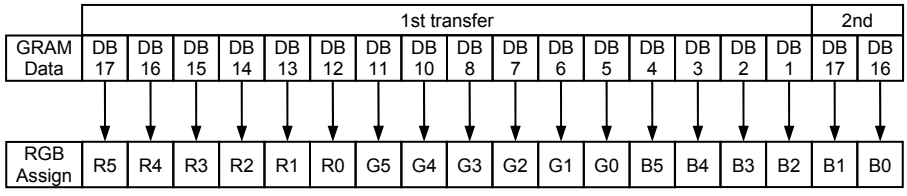
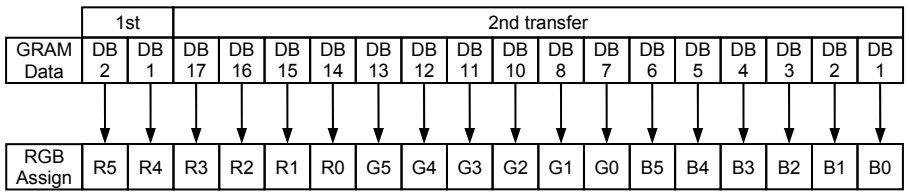
TRI	DFM	RAM write data transfer via 8-bit interface
0	*	80-system 8-bit interface (2 transfers/pixel) – 65k colors 
1	0	80-system 8-bit interface (3 transfers/pixel) – 262k colors 
1	1	80-system 8-bit interface (3 transfers/pixel) – 262k colors 

Table 12

TRI	DFM	RAM write data transfer via 16-bit interface
0	*	80-system 16-bit interface (1 transfers/pixel) – 65k colors 
1	0	80-system 16-bit interface MSB mode(2 transfers/pixel) – 262k colors available 
1	1	80-system 16-bit interface LSB mode(2 transfers/pixel) – 262k colors available 

BGR – Reverses the order of RGB dots to BGR when writing 18-bit pixel data to the internal GRAM.
BGR = 0 : Write source data in order of R-G-B.
BGR = 1 : Change the order with B-G-R.

ORG – Moves the origin of a window address area in combination with the ID setting. This function is enabled when writing data within the window address area.

I/D[1:0] – The address counter is automatically incremented by 1 as writing data to the internal GRAM when I/D[1:0] = "1". The address counter is automatically decremented by 1 as writing data to the internal GRAM when I/D[1:0] = "0". The increment/decrement can be set separately to each upper (AD[15:8]) / lower (AD[7:0]) byte of address. The transition direction of address (vertical/horizontal) when writing data to the internal GRAM is set with the AM bit.

AM – Sets the direction of automatically updating address for writing data to the internal RAM in the address counter (AC). When AM = "0", the address is updated in horizontal writing direction. When AM = "1", the address is updated in vertical writing direction. When a window address area is set, data are written only to the GRAM area specified with window address in the writing direction set with I/D[1:0] and AM bits.

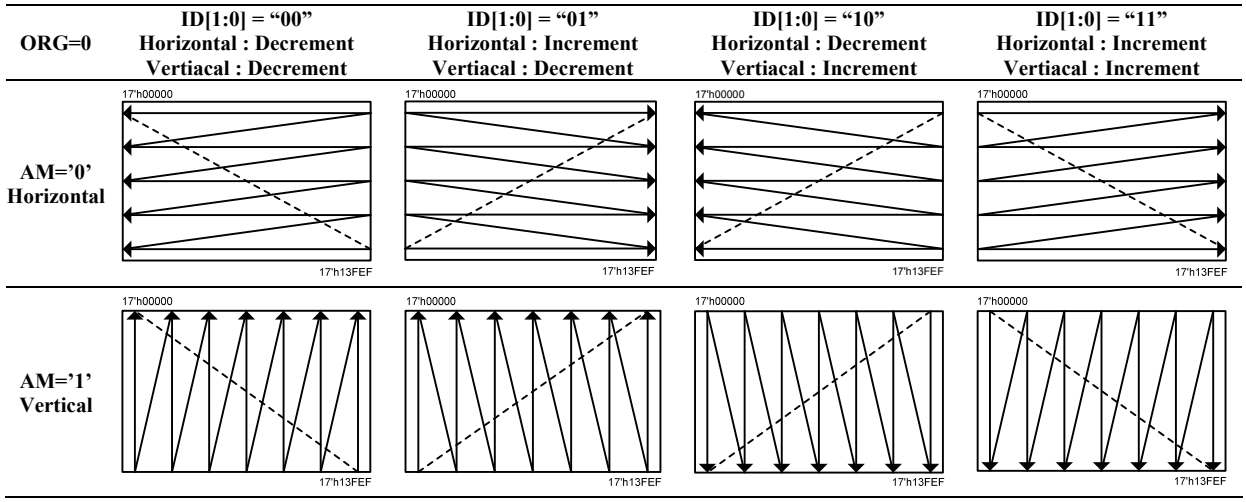


Figure 9 Automatic address update (ORG=0, AM, ID)

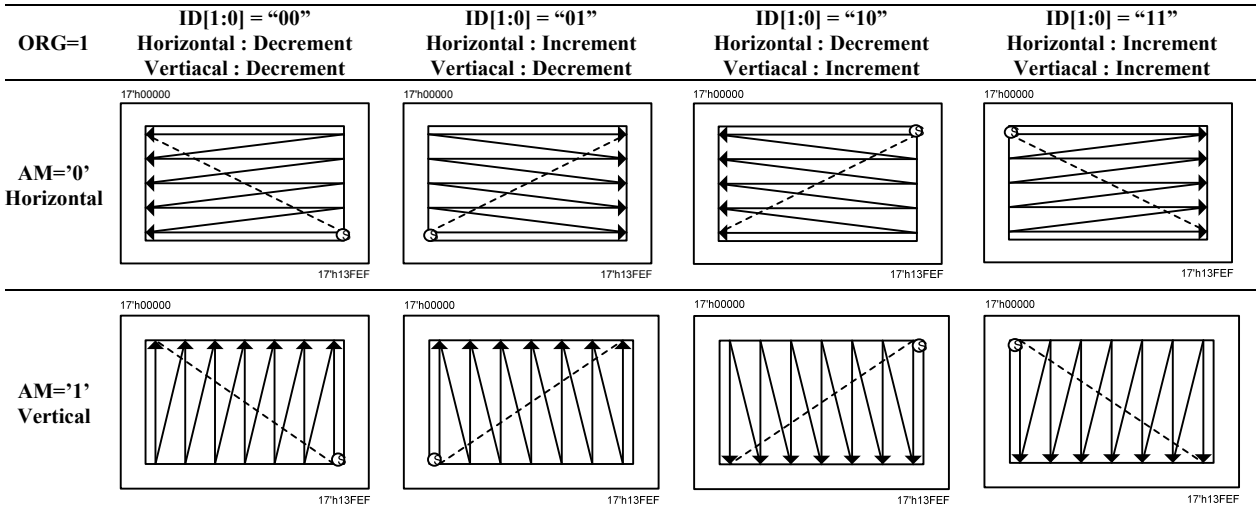


Figure 10 Automatic address update (ORG=1, AM, ID)

EPF[1:0] – Set the data format when 16bpp(R,G and B) to 18bpp(r, g and b) is stored in internal RAM. EPF settings are effective when :

1. 80-system 16-bit interface, TRI = 0
2. 80-system 8-bit interface, TRI = 0
3. Clock synchronous serial interface

Table 13

EPF	Expand 16bpp(R,G,B) to 18bpp(r,g,b)
2'h0	Same vaule as MSB is inputted to LSB of R and B r[5:0] = {R[4:0], R[4]} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], B[4]}
2'h1	"0" is inputted to LSB of r and b r[5:0] = {R[4:0], 1'b0} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 1'b0} Except. R[4:0], B[4:0] = 5'h1F -> r,b[5:0] = 6'h3F G[5:0] = 6'h3F -> g[5:0] = 6'h3F
2'h2	"1" is inputted to LSB of r and b r[5:0] = {R[4:0], 1'b1} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 1'b1} Except. R[4:0], B[4:0] = 5'h00 -> r,b[5:0] = 6'h00 G[5:0] = 6'h00 -> g[5:0] = 6'h00
2'h3	Setting disabed

Resizing Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV[1:0]		0	0	RCH[1:0]		0	0	RSZ[1:0]	

RSZ[1:0] – Sets the resizing factor. When the RSZ bits are set for resizing, the LGDP4551 writes the data of the resized image in both horizontal and vertical directions according to the resizing factor on the internal GRAM. See "Resizing fuction".

RCH[1:0] – Sets the number of pixels made as the remainder in horizontal direction as a result of resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ=2'h0) or there are no remainder pixels.

RCV[1:0] – Sets the number of pixels made as the remainder in vertical direction as a result of resizing a picture. By specifying the number of remainder pixels with RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ=2'h0) or there are no remainder pixels.

Table 14

RSZ[1:0]	Resizing scale
2'h0	No resizing (x1)

2'h1	x 1/2
2'h2	Setting disabled
2'h3	x 1/4

Table 15

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Table 16

RCV[1:0]	Number of remainder Pixels in Vertical Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE[1:0]		0	0	0	BASEE	0	0	GON	DTE	COL	0	D[1:0]	

D[1:0] – A graphics display appears on the screen when D[1] = "1", and is turned off upon setting D[1] = "0". When setting D[1] = "0", the graphics display data are retained in the internal GRAM and the display appears instantly on the screen upon setting D[1] to "1". When the D[1] bit is "0", i.e. while no display is shown on the screen, all source outputs are at the GND level to reduce charging/discharging current on liquid crystal cells, which is generated during liquid crystal AC drive.

When the display is turned off by setting D[1:0] = 2'h1, the LGDP4551 continues internal display operation. When the display is turned off by setting D[1:0] = 2'h0, the LGDP4551's internal display operation is halted completely. In combination with GON bit, the D[1:0] bits control ON/OFF of graphics display. For details, see "Instruction setting".

Table 17

D[1:0]	BASEE	Source Output (S1-720)	FMARK signal	Internal Operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-display	Operation	Operation
2'h3	0	Non-display	Operation	Operation
	1	Base-image display	Operation	Operation

Notes: 1. The data write operation from the microcomputer is not affected by the setting in the D[1:0] bits.
2. The PTS bits set the source output level for "non-lit display"

COL – When COL = "1", the 8-color display mode is selected. For details, see the "8-color Display Mode" section. The 8-color display mode is not available in external interface mode.

Table 18

COL	Operating amplifier	Display color
1'h0	64	262,144
1'h1	2	8

Note: When COL=1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

GON, DTE – The combination of settings in GON and DTE bits sets the output level form gate lines(G1-G432). When GON=0, the Vcom output level becomes the GND level.

Table 19

GON	DTE	G1-G432
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

BASEE – Base image display enable bit.

BASEE = 0 : No base image is displayed. The LGDP4551 drives liquid crystal at no-display level or shows only partial images on the screen.

BASEE = 1 : A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE[1:0] – PTDE[0] is the display enable bit of partial image 1. PTDE[1] is the display enable bit of partial image 2. When PTDE[1]/[0]=0, the partial image is turned off and only base image is displayed on the screen. When PTDE[1]/[0]= 1, the partial image is displayed on the screen. In this case, turn off the base image by setting BASEE = 0.

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	FP[7:0]								BP[7:0]							

FP[7:0]/BP[7:0] – Sets the blank period made at the beginning and the end of a display (front porch and back porch, respectively). The FP[7:0] and BP[7:0] bits specify the number of lines for the front and back porch periods, respectively. In setting, be sure:

FP ≥ 2 lines
BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal.

Table 20

FP[7:0]/BP[7:0]	Number of lines for the front/back porches
8'h00	Setting disabled
8'h01	Setting disabled
8'h02	2 lines
8'h03	3 lines
8'h04	4 lines
8'h05	5 lines
8'h06	6 lines
8'h07	7 lines
8'h08	8 lines
8'h09	9 lines
8'h0A	10 lines
8'h0B	11 lines
:	:
8'hED	253 lines
8'hFE	254 lines
8'hFF	255 lines

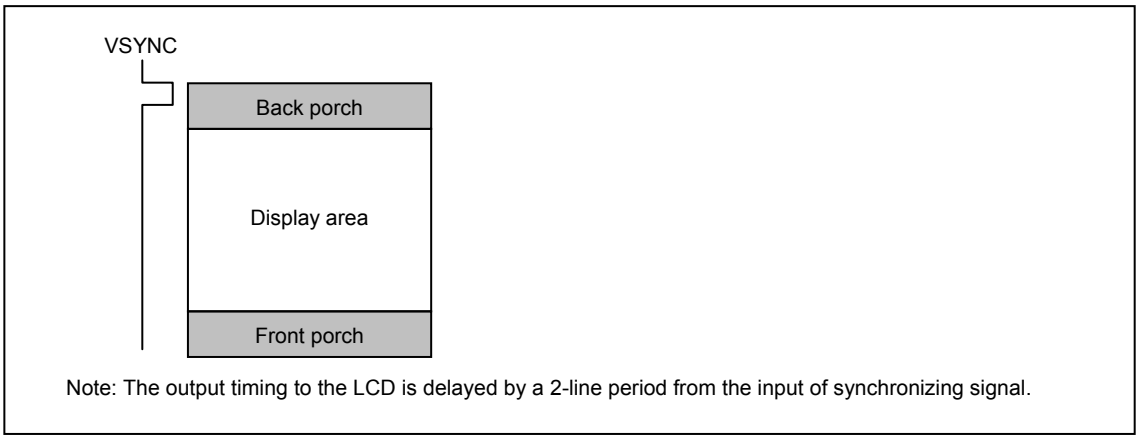


Figure 11 Back/front porches

Set the BP[7:0], FP[7:0] bits as follows in each operation mode.

Table 21

Internal clock operation	BP ≥ 2 lines	FP ≥ 2 lines	
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS[2:0]			0	0	PTG[1:0]		ISC[3:0]			

ISC[3:0] – Set the interval of scan when PTG[1:0] sets the interval scan. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal is inverted in the same cycle as the interval scan.

Table 22

ISC[3:0]	Scan cycle	Time for interval when(fFLM)=60Hz
4'h0	Setting disabled	-
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTG[1:0] – Set the scan mode in non-display area, which is made between partial display periods of the first and the second images, or turning off both base and partial images(full-screen non display). The setting is commonly applied to all non-display drive period.

Table 23

PTG[1:0]	Gate drive operation In non-display area	Source output level In non-display area	Vcom output
2'h0	Normal scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h1	Setting disabled	-	-
2'h2	Interval scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h3	Setting disabled	-	-

Note: Select frame-inversion AC drive when setting interval scan.

PTS[2:0] – Set the source output in non-display drive period.

Table 24

PTS[2:0]	Source output level		Grayscale amplifier In operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3h0	V63	V0	V0 to V63	Register setting(DC0,DC1)
3h1	Setting disabled	Setting disabled	-	-
3h2	GND	GND	V0 to V63	Register setting(DC0,DC1)
3h3	Hi-Z	Hi-Z	V0 to V63	Register setting(DC0,DC1)
3'h4	V63	V0	V0 and V63	1/2 the frequency set with DC0,DC1
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0 and V63	1/2 the frequency set with DC0,DC1
3'h7	Hi-Z	Hi-Z	V0 and V63	1/2 the frequency set with DC0,DC1

Notes: 1.The gate output level in non-display drive period is controlled by the PTG setting(off-scan mode).

Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI[2:0]		

FMI[2:0] – Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE – When FMARKOE=1, the LGDP4551 starts outputting FMARK signal from the FMARK pin in the output interval set with the FMI[2:0] bits. See “FMARK” for details.

Table 25

FMI[2:0]	Output interval
3’h0	1 frame
3’h1	2frame
3’h3	4 frame
3’h5	6 frame
Others settings	Setting disabled

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	ENC[2:0]			0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	

ENC[2:0] – Sets the RAM data write cycle in RGB interface mode.

Table 26 ENC[2:0] bits

ENC[2:0]	RAM data write cycle (frame periods)
3’h0	1 frame
3’h1	
3’h2	
3’h3	

RM – Selects the interface to access the LGDP4551’s internal GRAM. The RAM access is possible only via the interface selected with the RM bit. Set RM to “1” when writing display data via the RGB interface. The LGDP4551 allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = “0” even while display operations are performed via the RGB interface.

Table 27 RM bit

RM	Interface for RAM access
1’h0	System interface/VSYNC interface
1’h1	RGB interface

RIM[1:0] – Selects one of the following RGB interface modes when the RGB interface mode is selected with the RM and DM bits. Make this setting before display operation via external display interface. Do not make changes to the setting during display operation.

Table 28 RIM[1:0] bits

RIM[1:0]	RGB interface mode
2'h00	18-bit RGB interface (1 transfer/pixel)
2'h01	16-bit RGB interface (1 transfer/pixel)
2'h10	6-bit RGB interface (3 transfers/pixel)
2'h11	Setting disabled

DM[1:0] – Sets the display operation mode. By setting DM[1:0] as follows, it is possible to switch between the internal clock operation mode and the external display interface mode. Do not switch between different external interface modes (RGB interface and VSYNC interface).

Table 29 DM[1:0] bits

DM[1:0]	Display operation mode
2'h00	Internal clock operation
2'h01	RGB interface
2'h10	VSYNC interface
2'h11	Setting disabled

Notes:

1. Instructions are set only via the system interface.
2. Be sure that data transfer and dot clock input are performed in units of RGB dots in 6-bit RGB interface mode.

As the following table, the optimum interface for the state of display can be selected by setting the external display interface mode.

Table 30

Display State	Operation mode	RAM access (RM)	Display mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 01)
Rewrite still picture area while display moving pictures	RGB interface (2)	System interface (RM = 0)	RGB interface (DM = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM = 10)

Notes:

1. Instructions are set only via the system interface.
2. The RGB-I/F and the VSYNC-I/F are not used simultaneously.
3. Do not make changes to the RGB-I/F mode setting (RIM) while the RGB I/F is in operation.
4. See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.

Internal clock operation mode

All display operations are synchronized with the signals generated from the internal operating clock in this mode. None of inputs via the external display interface are valid. The internal RAM is accessible only via the system interface.

RGB interface mode (1)

In RGB interface mode, display operations are synchronized with the frame synchronizing signal (VSYNC), the line synchronizing signal (HSYNC), and the dot clock (DOTCLK). These signals must be supplied through a display period using the RGB interface.

Display data are transferred in units of pixels via the DB[17:0] pins. All display data are stored in the internal RAM. The combined use of the high-speed RAM write mode and the widow address function enables not only displaying data in moving picture area and data in the internal RAM in other than the moving picture area at a time but also minimizing data transfer by transferring data only when rewriting screen.

The front porch (FP) and back porch (BP) periods, and the display duration period (NL) are automatically calculated inside the LGDP4551 by internally counting the number of line synchronizing signal clocks (HSYNC) from the falling edge of the frame synchronizing signal (VSYNC). Take this into consideration when transferring RGB data via the DB[17:0] pins.

RGB interface mode (2)

The LGDP4551 enables rewriting RAM data via the system interface while the RGB interface is selected for display operation. In this case, Be sure to write RAM data while display data are not being transferred via the RGB interface (ENABLE = High). To return to the display data transfer mode via the RGB interface, change the ENABLE bit first and then set a new address (AD[15:0]) in the AC and the index register to R22h.

VSYNC interface mode

In VSYNC interface mode, internal display operations are synchronized with the frame synchronizing signal (VSYNC). In this mode, a moving picture can be displayed via the system interface by writing data to the internal RAM at more than the minimum speed from the falling edge of frame synchronizing signal (VSYNC). In this case, there are constraints in the RAM writing speed and method. For details, see “External Display Interface”.

No external signal input except VSYNC input is accepted in VSYNC interface mode.

The timings and durations of front porch (FP), back porch (BP) periods and display duration period (NL) are automatically calculated from the falling edge of the frame synchronization signal (VSYNC) according to the instructions set in the relevant registers.

Frame Marker Position (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	FMP[9:0]									

FMP[9:0] – Sets the output position of frame cycle signal (frame marker). When FMP[9:0] = 10’h000, a high-active pulse FMARK is output at the start of back porch period for 1H period (IOVcc-IOGND amplitude signal). FMARK can be used as a trigger signal for frame synchronous write operation. See “FMARK” for details.

Make sure 10’h000 <=FMP <= BP+NL+FP

Table 31

FMP[9:0]	FMARK output position
10'h000	0th line
10'h001	1st line
10'h002	2nd line
:	:
10'h2AC	684rd line
10'h2AD	685th line
10'h2AE	686th line
10'h2AF	687th line

External Display Interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

DPL – Sets the signal polarity of DOTCLK pin.

DPL = 0 : input data on the rising edge of DOTCLK
DPL = 1 : input data on the falling edge of DOTCLK

EPL – Sets the signal polarity of ENABLE pin.

EPL = 0 : writes data DB[17:0] when ENABLE = 0 and disables data write operation when ENABLE = 1.
EPL = 1 : writes data DB[17:0] when ENABLE = 1 and disables data write operation when ENABLE = 0.

HSPL – Sets the signal polarity of HSYNC pin.
HSPL = 0 : Low active
HSPL = 1 : High active

VSPL – Sets the signal polarity of VSYNC pin.
VSPL = 0 : Low active
VSPL = 1 : High active

Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	SAP[2:0]				BT[2:0]			0	AP[2:0]			DK	DSTB	SLP	STB

STB – When STB = "1", the LGDP4551 enters the standby mode. In standby mode, the display operation completely halts, and the internal operation, including internal RC oscillation and reception of external clock pulses, completely halts. Only instructions to release the LGDP4551 from the standby mode (STB = "0") and to start oscillators are accepted during the standby mode. To set the standby mode, follow the sequence of standby mode setting.

SLP – When SLP = 1, the LGDP4551 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change of GRAM data or instruction is accepted in sleep mode. The GRAM data and the instruction bits remain unchanged.

DSTB – When DSTB = 1, the LGDP4551 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and the instruction bit setting are destroyed and must be reset after exiting deep standby mode.

DK – Activates DDVDH. When DK = 0, DDVDH activates at the same timing as VGH. When DK = 1, DDVDH activates separately from VGH.

Table 32

DK	Step-up Cycle in Step-up Circuit 1
1'h0	Startup DDVDH simultaneously with VGH. Startup step-up circuit 1 (VLOUT1 output) according to AP[2:0]
1'h1	Halt step-up circuit 1 (VLOUT1). (Default)

AP[2:0] – Adjusts the constant current in the operation amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0]=3'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.
Adjust the amount of fixed current from the fixed-current source in the internal operational amplifier circuit. VGH operates when AP is not 000. Complete setting AP before setting PON = 1. (While setting PON = 1, setting of AP bit cannot be changed.) For the details of sequences, refer to Flow of "Power Supply Setting".

Table 33

AP[2:0]	LCD power supply circuits	Grayscale voltage generating circuit
3'h0	Halt operation	Halt operation
3'h1	Setting disabled	Setting disabled
3'h2	Normal operation	0.5
3'h3	Normal operation	0.75
3'h4	Normal operation	1
3'h5	Normal operation	1.25
3'h6	Normal operation	1.5
3'h7	Setting disabled	Setting disabled

Note: In this table, the constant current in operational amplifiers is shown by the ratio to the constant current when AP[1:0] is set to 2'h3.

BT[2:0] – Sets the factor used in the step-up circuits. Use an optimal step-up factor for the voltage in use. To reduce power consumption, set a smaller factor.

Table 34 Step up factor and output voltage level

BT[2:0]	DDVDH	VGH	VGL	Capacitor connection Pins
3'h0	Vci1 x 2 [x 2]	DDVDH x 4 [x 8]	–(Vci1 + DDVDH x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
3'h1			–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
3'h2			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
3'h3		Vci1 + DDVDH x 3 [x 7]	–(Vci1 + DDVDH x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
3'h4			–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
3'h5			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
3'h6		DDVDH x 3 [x 6]	–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
3'h7			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±

Note: 1. The step-up factor from Vci1 are shown in the brackets [ ].
2. Connect capacitors where required when using DDVDH, VGH, VGL voltages.
3. Set the following voltages within the respective ranges:
DDVDH = 6.0V(max.), VGH = 15.0V (max.) and VGL = -12.5V (max.)

SAP[2:0] – Adjust the constant current for the operational amplifer circuit in the source driver. A larger constant current stabilizes the operational ampilifer circuit, but current consumption increases. Adjust the constant current taking the display quality-current consumprion trade-off into account. During a period showing no display, set SAP = 0 to halt the operational amplifier circuit to reduce current consumption.

Table 35

SAP[2:0]	Constant current (ratio to 3)
3'h0	Halt operational amplifier
3'h1	Constant current (ratio to 3) : 0.65
3'h2	Constant current (ratio to 3) : 0.8
3'h3	Constant current (ratio to 3) : 1.00
3'h4	Constant current (ratio to 3) : 1.35
3'h5	Constant current (ratio to 3) : 1.60
3'h6	Setting disabled
3'h7	Setting disabled

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC1[2:0]			0	DC0[2:0]			0	VC[2:0]		

Table 36 Step-up frequency (Step-up Circuit 1)

DC0[2:0]	Step-up circuit 1 : step-up frequency (f_{DCDC1})
3'h0	fosc/16
3'h1	fosc/32
3'h2	fosc/64
3'h3	fosc/128
3'h4	fosc/256
3'h5	fosc/8
3'h6	Halt step-up circuit 1
3'h7	fosc/4

Note : Make sure to set DC0 and DC1 to maintain $f_{DCDC1} \geq f_{DCDC2}$.

Table 37 Step-up frequency (Step-up Circuit 2)

DC1[2:0]	Step-up circuit 2 : step-up frequency (f_{DCDC2})
3'h0	fosc/128
3'h1	fosc/256
3'h2	fosc/512
3'h3	fosc/1024
3'h4	fosc/2048
3'h5	fosc/64
3'h6	Halt step-up circuit 2
3'h7	fosc/32

Note : Make sure to set DC0 and DC1 to maintain $f_{DCDC1} \geq f_{DCDC2}$.

Table 38 VciOUT output level

VC[2:0]	VciOUT (Reference Voltage) (Vci1 Voltage)
3'h0	1.00 x VciLVL
3'h1	0.92 x VciLVL
3'h2	0.90 x VciLVL
3'h3	0.87 x VciLVL
3'h4	0.85 x VciLVL
3'h5	0.83 x VciLVL
3'h6	0.73 x VciLVL
3'h7	Setting disabled

Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH[3:0]			

VRH[3:0] – Sets the factor to generate VREG1OUT from VciLVL.

Table 39 VREG1OUT

VRH[3:0]	VREG1OUT Voltage
4'h0	VciOUT x 1.27
4'h1	VciOUT x 1.32
4'h2	VciOUT x 1.37
4'h3	VciOUT x 1.42
4'h4	VciOUT x 1.47
4'h5	VciOUT x 1.52
4'h6	VciOUT x 1.57
4'h7	Setting disabled
4'h8	Setting disabled
4'h9	VciOUT x 1.62
4'hA	VciOUT x 1.67
4'hB	VciOUT x 1.72
4'hC	VciOUT x 1.77
4'hD	VciOUT x 1.82
4'hE	VciOUT x 1.87
4'hF	VciOUT x 1.92

Note: Set the VC and VRH bits to maintain the VREG1OUT voltage at (DDVDH – 0.5) V or less.

PON – Controls the operation to generate VLOUT3. In setting the PON bit, follows the power-supply startup sequence.

PON = 0 : Halts the step-up operation to generate VLOUT3.
PON = 1 : Starts the step-up operation to generate VLOUT3.

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV[4:0]					0	VCM[6:0]						

VCM[6:0] – Sets the VcomH level (the higher voltage of Vcom alternating drive). VCM[6:0] specifies the voltage by VREG1OUT x n, where n is a discrete number from 0.400 to 0.875. To halt internal volume and adjust VcomH with an external resistor from VcomR, set VCM[6:0] = "1111111".

Table 40

VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH
7'h00	VREG1OUT x 0.400	7'h20	VREG1OUT x 0.560	7'h40	VREG1OUT x 0.720	7'h60	VREG1OUT x 0.880
7'h01	VREG1OUT x 0.405	7'h21	VREG1OUT x 0.565	7'h41	VREG1OUT x 0.725	7'h61	VREG1OUT x 0.885
7'h02	VREG1OUT x 0.410	7'h22	VREG1OUT x 0.570	7'h42	VREG1OUT x 0.730	7'h62	VREG1OUT x 0.890
7'h03	VREG1OUT x 0.415	7'h23	VREG1OUT x 0.575	7'h43	VREG1OUT x 0.735	7'h63	VREG1OUT x 0.895
7'h04	VREG1OUT x 0.420	7'h24	VREG1OUT x 0.580	7'h44	VREG1OUT x 0.740	7'h64	VREG1OUT x 0.900
7'h05	VREG1OUT x 0.425	7'h25	VREG1OUT x 0.585	7'h45	VREG1OUT x 0.745	7'h65	VREG1OUT x 0.905
7'h06	VREG1OUT x 0.430	7'h26	VREG1OUT x 0.590	7'h46	VREG1OUT x 0.750	7'h66	VREG1OUT x 0.910
7'h07	VREG1OUT x 0.435	7'h27	VREG1OUT x 0.595	7'h47	VREG1OUT x 0.755	7'h67	VREG1OUT x 0.915
7'h08	VREG1OUT x 0.440	7'h28	VREG1OUT x 0.600	7'h48	VREG1OUT x 0.760	7'h68	VREG1OUT x 0.920
7'h09	VREG1OUT x 0.445	7'h29	VREG1OUT x 0.605	7'h49	VREG1OUT x 0.765	7'h69	VREG1OUT x 0.925
7'h0A	VREG1OUT x 0.450	7'h2A	VREG1OUT x 0.610	7'h4A	VREG1OUT x 0.770	7'h6A	VREG1OUT x 0.930
7'h0B	VREG1OUT x 0.455	7'h2B	VREG1OUT x 0.615	7'h4B	VREG1OUT x 0.775	7'h6B	VREG1OUT x 0.935
7'h0C	VREG1OUT x 0.460	7'h2C	VREG1OUT x 0.620	7'h4C	VREG1OUT x 0.780	7'h6C	VREG1OUT x 0.940
7'h0D	VREG1OUT x 0.465	7'h2D	VREG1OUT x 0.625	7'h4D	VREG1OUT x 0.785	7'h6D	VREG1OUT x 0.945
7'h0E	VREG1OUT x 0.470	7'h2E	VREG1OUT x 0.630	7'h4E	VREG1OUT x 0.790	7'h6E	VREG1OUT x 0.950
7'h0F	VREG1OUT x 0.475	7'h2F	VREG1OUT x 0.635	7'h4F	VREG1OUT x 0.795	7'h6F	VREG1OUT x 0.955
7'h10	VREG1OUT x 0.480	7'h30	VREG1OUT x 0.640	7'h50	VREG1OUT x 0.800	7'h70	VREG1OUT x 0.960
7'h11	VREG1OUT x 0.485	7'h31	VREG1OUT x 0.645	7'h51	VREG1OUT x 0.805	7'h71	VREG1OUT x 0.965
7'h12	VREG1OUT x 0.490	7'h32	VREG1OUT x 0.650	7'h52	VREG1OUT x 0.810	7'h72	VREG1OUT x 0.970
7'h13	VREG1OUT x 0.495	7'h33	VREG1OUT x 0.655	7'h53	VREG1OUT x 0.815	7'h73	VREG1OUT x 0.975
7'h14	VREG1OUT x 0.500	7'h34	VREG1OUT x 0.660	7'h54	VREG1OUT x 0.820	7'h74	VREG1OUT x 0.980
7'h15	VREG1OUT x 0.505	7'h35	VREG1OUT x 0.665	7'h55	VREG1OUT x 0.825	7'h75	Setting disabled
7'h16	VREG1OUT x 0.510	7'h36	VREG1OUT x 0.670	7'h56	VREG1OUT x 0.830	7'h76	Setting disabled
7'h17	VREG1OUT x 0.515	7'h37	VREG1OUT x 0.675	7'h57	VREG1OUT x 0.835	7'h77	Setting disabled
7'h18	VREG1OUT x 0.520	7'h38	VREG1OUT x 0.680	7'h58	VREG1OUT x 0.840	7'h78	Setting disabled
7'h19	VREG1OUT x 0.525	7'h39	VREG1OUT x 0.685	7'h59	VREG1OUT x 0.845	7'h79	Setting disabled
7'h1A	VREG1OUT x 0.530	7'h3A	VREG1OUT x 0.690	7'h5A	VREG1OUT x 0.850	7'h7A	Setting disabled
7'h1B	VREG1OUT x 0.535	7'h3B	VREG1OUT x 0.695	7'h5B	VREG1OUT x 0.855	7'h7B	Setting disabled
7'h1C	VREG1OUT x 0.540	7'h3C	VREG1OUT x 0.700	7'h5C	VREG1OUT x 0.860	7'h7C	Setting disabled
7'h1D	VREG1OUT x 0.545	7'h3D	VREG1OUT x 0.705	7'h5D	VREG1OUT x 0.865	7'h7D	Setting disabled
7'h1E	VREG1OUT x 0.550	7'h3E	VREG1OUT x 0.710	7'h5E	VREG1OUT x 0.870	7'h7E	Setting disabled
7'h1F	VREG1OUT x 0.555	7'h3F	VREG1OUT x 0.715	7'h5F	VREG1OUT x 0.875	7'h7F	Halt internal volume.

Note : Set the VcomH voltage from VCI to (DDVDH – 0.5)V

VDV[4:0] – Sets the alternating amplitudes of VCOM AC voltage. These bits amplify VCOM by from 0.6 to 1.23 times the VREG1OUT voltage. If VCOMG = 0, VDV[4:0] bits are disabled.

Table 41

VDV[4:0]	Vcom amplitude	VDV[4:0]	Vcom amplitude
5'h00	VREG1OUT x 0.60	5'h10	VREG1OUT x 1.05
5'h01	VREG1OUT x 0.63	5'h11	VREG1OUT x 1.08
5'h02	VREG1OUT x 0.66	5'h12	VREG1OUT x 1.11
5'h03	VREG1OUT x 0.69	5'h13	VREG1OUT x 1.14
5'h04	VREG1OUT x 0.72	5'h14	VREG1OUT x 1.17
5'h05	VREG1OUT x 0.75	5'h15	VREG1OUT x 1.20
5'h06	VREG1OUT x 0.78	5'h16	VREG1OUT x 1.23
5'h07	VREG1OUT x 0.81	5'h17	VREG1OUT x 1.26
5'h08	VREG1OUT x 0.84	5'h18	VREG1OUT x 1.29
5'h09	VREG1OUT x 0.87	5'h19	VREG1OUT x 1.32
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.35
5'h0B	VREG1OUT x 0.93	5'h1B	VREG1OUT x 1.38
5'h0C	VREG1OUT x 0.96	5'h1C	VREG1OUT x 1.41
5'h0D	VREG1OUT x 0.99	5'h1D	VREG1OUT x 1.44
5'h0E	VREG1OUT x 1.02	5'h1E	VREG1OUT x 1.47
5'h0F	Setting disabled	5'h1F	VREG1OUT x 1.50

Note : Set the VcomL voltage from (VCL + 0.5)V to 0.5V

VCOMG – When VCOMG = 1, the LGDP4551 can output a negative voltage level for VCOML (1.0 ~ -Vci + 0.5V max). When VCOMG = 0, the LGDP4551 halts the amplifier for negative voltage to save power. When VCOMG = 0, the VDV[4:0] bits are disabled. In this case, adjust the amplitude of VCOM AV voltage with VCM[4:0] bits (VCOMH setting). Set PON = 1 before setting VCOMG = 1.
When VCOMG = 1, voltage of VCOML can be set to any level, and instruction (VDV) becomes valid. VCOMG = 1 is valid when PON = 1. When VCOMG = 0, output of VCOML if fixed to GND level, and setting of instruction (VDV) becomes invalid. When VCOMG = 0, output of VCOML and VCL stop.

Regulator Control (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RSET			0	RI[2:0]			0	RV[2:0]			0	RCONT[2:0]		

RCONT[2:0] – These bits control the input voltage of main bias op_amp.

Table 42

RCONT[2:0]	Input voltage
3'h0	Vci x 0.25
3'h1	Setting diabled
3'h2	Open
3'h3	Vci x 0.30
3'h4	Setting disabled
3'h5	Setting disabled
3'h6	Vci x 0.20
3'h7	Setting disabled

RV[2:0] – These bits control the output voltage of internal logic regulator.

Table 43

RV [2:0]	Vdd voltage
3'h0	Vci x 0.80
3'h1	Vci x 0.75
3'h2	Vci x 0.70
3'h3	Vci x 0.65
3'h4	Vci x 0.60
3'h5	Vci x 0.55
3'h6	Vci x 0.50
3'h7	Vci x 0.45

RI[2:0] – These bits control the bias current of internal logic regulator.

Table 44

RI [2:0]	Constant current
3'h0	0.2
3'h1	0.1
3'h2	2.2
3'h3	3
3'h4	3.2
3'h5	4
3'h6	5.2
3'h7	6

Note : In this table, the constant current is shown by the ratio to the constant current when RI[2:0] is set to 3'h3.

RSET[2:0] – These bits control the main bias.

Gamma Select Control (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SGE	0	0	0	EN_MA	0	0	0	PS

PS – This bit specify the VA mode enable signal.

Table 45

PS	Mode
1'h0	TN mode
1'h1	VA mode

EN_MA – This bit specify the PFN0-5/PFP0-1/PMN/PMP registers Manaul setting enable signal
.

Table 46

		EN_MA	PS
Auto	TN mode	0	0
	VA mode	0	1
Manual	User setting	1	x

SGE – Sets the R/G/B gamma register.

Table 47

SGE	
0	R/G/B gamma register: R30h-R3Fh
1	R gamma register : R30h ~ R3Fh G gamma register : RB0h ~RBFh B gamma register : RC0h ~RCFh

Vcom Control (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	LSZ[2:0]			0	HSZ[2:0]			0	0	0	CMFPD

LSZ[2:0] – This register controls VcomL amplifier to reduce cross-talk in frame inversion.

HSZ[2:0] – This register controls VcomH amplifier to reduce cross-talk in frame inversion.

CMFPD – Enable bit to use LSZ[2:0], HSZ[2:0] registers.
CMFPD = 0 : Enable LSZ[2:0], HSZ[2:0] registers, and set for frame inversion.
CMFPD = 1 : Disable LSZ[2:0], HSZ[2:0] registers, and set for line inversion.

RAM Address Set (Horizontal Address) (R20h)

RAM Address Set (Vertical Address) (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD[7:0]							
W	1	0	0	0	0	0	0	0	AD[16:8]								

AD[16:0] – A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as data is written to the internal GRAM in order to write data consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM='1'), the address AD[16:0] is set in the address counter every frame on the falling edge of VSYNC.
Note 2: In internal clock operation and VSYNC interface operation (RM='0'), the address AD[16:0] is set when executing the instruction.

Table 48

AD[16:0]	**GRAM Data Setting**
17'h00000 – 17'h000EF	Bitmap data on the first line
17'h00100 – 17'h001EF	Bitmap data on the second line
17'h00200 – 17'h002EF	Bitmap data on the third line
:	:
17'h1AD00 – 17'h1ADEF	Bitmap data on the 430th line
17'h1AE00 – 17'h1AEEF	Bitmap data on the 431st line
17'h1AF00 – 17'h1AFEF	Bitmap data on the 432nd line

Write Data to RAM (R22h)

R/W	RS	The bit assignment between RAM write data WD[17:0] and DB[17:0] differs according to the selected interface.
W	1	WD[17:0]

WD[17:0] – The LGDP4551 write data to the internal GRAM by expanding into 18 bits internally. The data expansion fomat into 18 bits differs according to the interface.

The GRAM data represents the grayscale level. The LGDP4551 automatically updates the address according to AM and I/D[1:0] as it writes data in the GRAM. In standby mode, the GRAM is not accessible. The data in 16-bit format is developed into 18 bits according to the register setting (DFM) in 8-/16-bit interface operation.

Note : When writing data in the GRAM via system interface while using the RGB interface, make sure that write operation via two interface do not conflict.

Table 49 GRAM data and corresponding LCD Grayscale level (REV = 1)

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h00	V63	V0
6'h01	V62	V1
6'h02	V61	V2
6'h03	V60	V3
6'h04	V59	V4
6'h05	V58	V5
6'h06	V57	V6
6'h07	V56	V7
6'h08	V55	V8
6'h09	V54	V9
6'h0A	V53	V10
6'h0B	V52	V11
6'h0C	V51	V12
6'h0D	V50	V13
6'h0E	V49	V14
6'h0F	V48	V15
6'h10	V47	V16
6'h11	V46	V17
6'h12	V45	V18
6'h13	V44	V19
6'h14	V43	V20
6'h15	V42	V21
6'h16	V41	V22
6'h17	V40	V23
6'h18	V39	V24
6'h19	V38	V25
6'h1A	V37	V26
6'h1B	V36	V27
6'h1C	V35	V28
6'h1D	V34	V29
6'h1E	V33	V30
6'h1F	V32	V31

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h20	V31	V32
6'h21	V30	V33
6'h22	V29	V34
6'h23	V28	V35
6'h24	V27	V36
6'h25	V26	V37
6'h26	V25	V38
6'h27	V24	V39
6'h28	V23	V40
6'h29	V22	V41
6'h2A	V21	V42
6'h2B	V20	V43
6'h2C	V19	V44
6'h2D	V18	V45
6'h2E	V17	V46
6'h2F	V16	V47
6'h30	V15	V48
6'h31	V14	V49
6'h32	V13	V50
6'h33	V12	V51
6'h34	V11	V52
6'h35	V10	V53
6'h36	V9	V54
6'h37	V8	V55
6'h38	V7	V56
6'h39	V6	V57
6'h3A	V5	V58
6'h3B	V4	V59
6'h3C	V3	V60
6'h3D	V2	V61
6'h3E	V1	V62
6'h3F	V0	V63

Table 50 GRAM data and corresponding LCD Grayscale level (REV = 0)

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h00	V0	V63
6'h01	V1	V62
6'h02	V2	V61
6'h03	V3	V60
6'h04	V4	V59
6'h05	V5	V58
6'h06	V6	V57
6'h07	V7	V56
6'h08	V8	V55
6'h09	V9	V54
6'h0A	V10	V53
6'h0B	V11	V52
6'h0C	V12	V51
6'h0D	V13	V50
6'h0E	V14	V49
6'h0F	V15	V48
6'h10	V16	V47
6'h11	V17	V46
6'h12	V18	V45
6'h13	V19	V44
6'h14	V20	V43
6'h15	V21	V42
6'h16	V22	V41
6'h17	V23	V40
6'h18	V24	V39
6'h19	V25	V38
6'h1A	V26	V37
6'h1B	V27	V36
6'h1C	V28	V35
6'h1D	V29	V34
6'h1E	V30	V33
6'h1F	V31	V32

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h20	V32	V31
6'h21	V33	V30
6'h22	V34	V29
6'h23	V35	V28
6'h24	V36	V27
6'h25	V37	V26
6'h26	V38	V25
6'h27	V39	V24
6'h28	V40	V23
6'h29	V41	V22
6'h2A	V42	V21
6'h2B	V43	V20
6'h2C	V44	V19
6'h2D	V45	V18
6'h2E	V46	V17
6'h2F	V47	V16
6'h30	V48	V15
6'h31	V49	V14
6'h32	V50	V13
6'h33	V51	V12
6'h34	V52	V11
6'h35	V53	V10
6'h36	V54	V9
6'h37	V55	V8
6'h38	V56	V7
6'h39	V57	V6
6'h3A	V58	V5
6'h3B	V59	V4
6'h3C	V60	V3
6'h3D	V61	V2
6'h3E	V62	V1
6'h3F	V63	V0

Read Data from RAM (R22h)

R/W	RS	The bit assignment between RAM write data RD[17:0] and DB[17:0] differs according to the selected interface.
R	1	RD[17:0]

RD[17:0] – 18-bit data read from the GRAM. The bit assignment between RD[17:0] and DB[17:0] (data on the data bus) differs according to the selected interface.

When the LGDP4551 read data from the GRAM to the microcomputer, the first word read immediately after RAM address set is taken in the intenal read-data latch and inbalid data is sent to the data bus DB[17:0]. Vaild data is sent to the data bus as the LGDP4551 reads out the second and subsequence words.

When either 8-bit or 16-bit interface is selected, the LSB of R and B dot data are not read out.

Note : This register is not available in RGB interface operation.

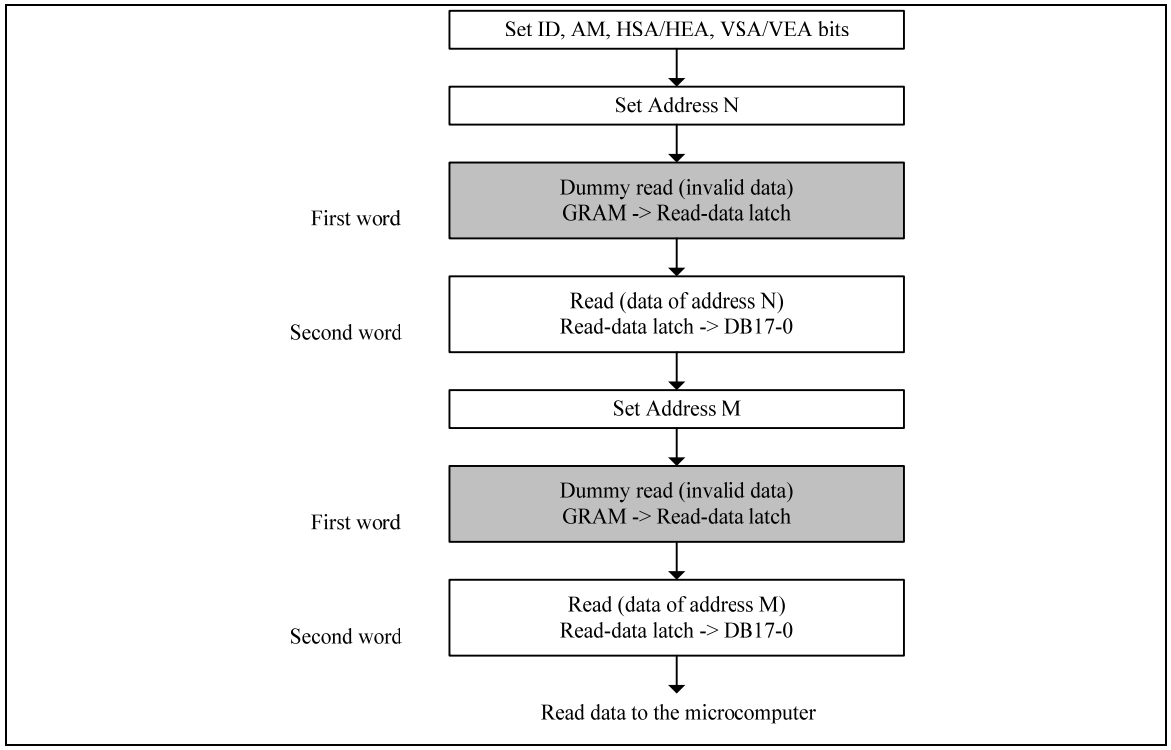


Figure 12

Red Gamma Control 1-16 (R30h to R3Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				
W	1						PFP1[2:0]								PFP0[2:0]		
W	1						PFP3[2:0]								PFP2[2:0]		
W	1						PFN1[2:0]								PFN0[2:0]		
W	1						PFN3[2:0]								PFN2[2:0]		
W	1														PMP[2:0]		
W	1														PMN[2:0]		

PKP5-0[2 :0] – γ fine-adjustment register for positive polarity
PRP1-0[2 :0] – γ gradient-adjustment register for positive polarity
VRP0[3:0], VRP1[4 :0] – γ amplitude-adjustment register for positive polarity

PKN5-0[2 :0] – γ fine-adjustment register for negative polarity
PRN1-0[2 :0] – γ gradient-adjustment register for negative polarity
VRN0[3:0], VRN1[4 :0] – γ amplitude-adjustment register for negative polarity

PFP3-0[2:0] – γ fine adjustment register bits for positive polarity
PFN3-0[2:0] – γ fine adjustment register bits for negative polarity
PMP[2:0] – γ fine adjustment register bits for positive polarity
PMN[2:0] – γ fine adjustment register bits for negative polarity

Note)
When BGR='1', these register setting values are for Blue Gamma Control.

For details, see "γ-Correction Function" section

EPROM Control Register 1 (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	PTM[1:0]		POR	VPP	PPROG	PWE	PA[1:0]		PDIN[7:0]							

EPROM programming control. See "EPROM Control" section.

PDIN[7:0] – Data input. This corresponds to VCM[6:0] bits of R13h.

PA[1:0] – address input. This selects one of four banks of the EPROM.

Table 51

PA[1:0]	Write Data Input	Write OPT Cell
2'h0	PDIN[6:0]	Cell[6:0]
2'h1	PDIN[6:0]	Cell[14:8]
2'h2	PDIN[6:0]	Cell[22:16]
2'h3	PDIN[6:0]	Cell[30:24]

PWE – Write enable.

PPROG – Program mode enable.

VPP – Power switch control for the VPP pin of the embedded EPROM. When VPP = "1", the internal VPP is set to 7.2V; otherwise it is set to 1.8V.

POR – Pin for power-on rest.

PTM[1:0] – Pins for enabling test mode

EPROM Control Register 2 (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0										AUTOWR	RA[1:0]		VCMSEL[1:0]	

EPROM programming control. See "EPROM Control" section.

VCMSEL[1:0] – With VCMSEL pin, sets VcomH level from either the register R13h or the EPROM

Table 52

VCMSEL[1:0]	VcomH Level adjustment
00	VCM[6:0] of the register R13h
01	EPROM data at first if EPROM has data. Otherwise,VCM[6:0] of the register R13h
1x	EPROM data selected by RA[1:0]

RA[1:0] – Read address input. This selects one of four banks of the EPROM.

AUTOWR – Select the methoe of write operation
If AUTOWR='1', write address is PA.
Else AUTOWR='0', write address is auto select address.

EPROM Control Register 3 (R42h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0								PDOUT[7:0]						

PDOUT[7:0] – EPROM Read Data output.

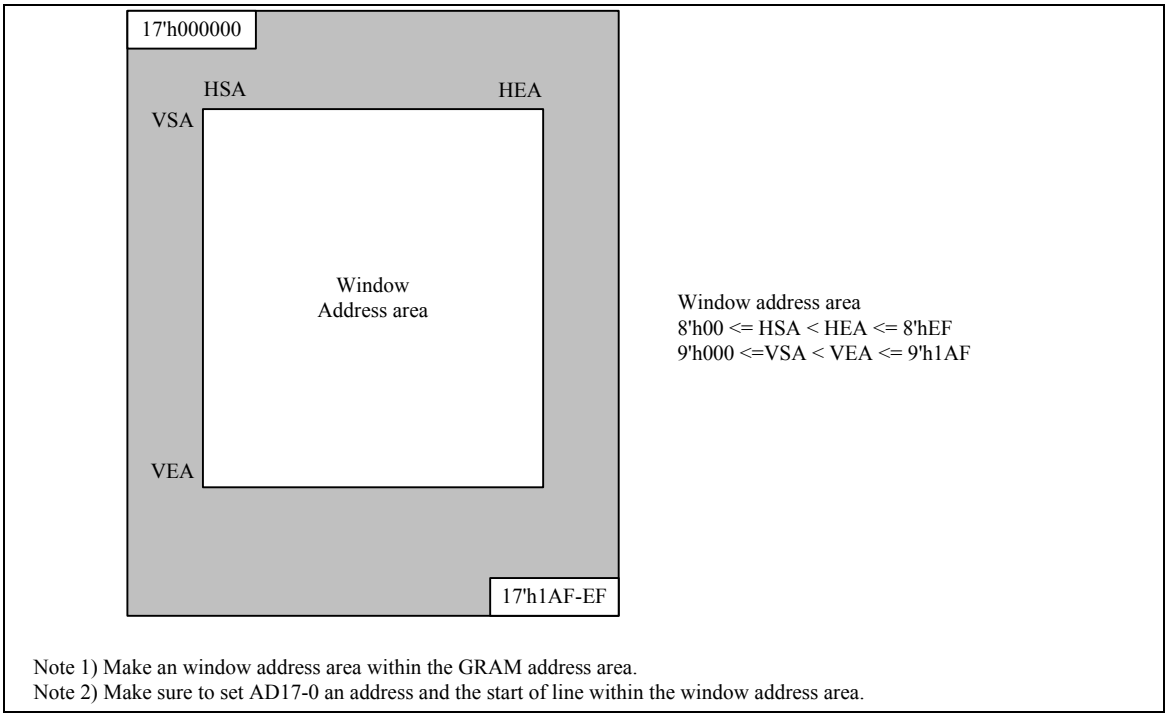
Window Horizontal RAM Address Start/End (R50h/R51h)

Window Vertical RAM Address Start/End (R52h/R53h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	HSA[7:0]							
W	1	0	0	0	0	0	0	0	0	HEA[7:0]							
W	1	0	0	0	0	0	0	0	VSA[8:0]								
W	1	0	0	0	0	0	0	0	VEA[8:0]								

HSA[7:0]/HEA[7:0] – HSA[7:0] and HEA[7:0] represent the addresses at the start and end of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the range on the GRAM to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HSA < HEA ≤ 8'hEF.

VSA[8:0]/VEA[8:0] – VSA[8:0] and VEA[8:0] represent the addresses at the start and end of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the range on the GRAM to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h1AF.



Note 1) Make an window address area within the GRAM address area.
Note 2) Make sure to set AD17-0 an address and the start of line within the window address area.

Figure 13

Driver Output Control (R60h)

Base Image Display Control (R61h)

Vertical Scroll Control (R6Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GS	0	NL[5:0]						0	0	SCN[5:0]					
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
W	1	0	0	0	0	0	0	0	VL[8:0]								

SCN[5:0] – Specifies the gate line where the gate driver starts scan.

NL[5:0] – Sets the number of lines to drive the LCD at an interval of 8lines. The GRAM address mapping is not affected by the number of lines set with NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 53

NL[5:0]	Number of Lines	NL[5:0]	Number of Lines
6'h00	8	6'h1C	232
6'h01	16	6'h1D	240
6'h02	24	6'h1E	248
6'h03	32	6'h1F	256
6'h04	40	6'h20	264
6'h05	48	6'h21	272
6'h06	56	6'h22	280
6'h07	64	6'h23	288
6'h08	72	6'h24	296
6'h09	80	6'h25	304
6'h0A	88	6'h26	312
6'h0B	96	6'h27	320
6'h0C	104	6'h28	328
6'h0D	112	6'h29	336
6'h0E	120	6'h2A	344
6'h0F	128	6'h2B	352
6'h10	136	6'h2C	360
6'h11	144	6'h2D	368
6'h12	152	6'h2F	376
6'h13	160	6'h30	384
6'h14	168	6'h30	392
6'h15	176	6'h31	400
6'h16	184	6'h32	408
6'h17	192	6'h33	416
6'h18	200	6'h34	424
6'h19	208	6'h35	432

6'h1A	216	6'h36~6'h3F	Setting disabled
6'h1B	224		

GS – Set the direction of scan by the gate driver. Set the GS bit in combination with SM and SS bits to optimize scan method to the LCD module.

REV – The grayscale level corresponding to the GRAM data can be reversed by setting REV = 1. This enables the LGDP4551 to display the same image form a same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by resiger setting (PTS).

Table 54

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFF	V63	V0

VLE – Vertical scroll display enable bit. When VLE = 1, the LGDP4551 starts displaying the base image from the line (of the physical display) determined by setting the VL[8:0] bits. VL[8:0] represents the number of lines shifted from the first line of the physical display (the amount of scrolling). Note that the display position of partial image is not affected by the base image scrolling.

The vertical scrolling is not available in external display inteface opration. In this case, make sure to set VLE = 0.

NDL – Sets the source output level in non-display lit driving periods. By setting the NDL bit, the non-display area can be kept lit on.

Table 55

NDL	Non-display area	
	Positive	Negative
0	V63	V0
1	V0	V63

VL[8:0] – Sets the amount of scrolling the base image by the number of lines. The RAM data in the start line address is displayed on the line, which is shifted from the first line of the liquid crystal panel by the number of lines set with VL[8:0]. In setting VL[8:0], make sure VL ≤ 432.

Table 56

SCN[5:0]	Gate line No (Scan start position)			
	SM = 0		SM = 1	
	GS = 0	GS = 1	GS = 0	GS = 1
6'h00	G1	G432	G1	G432
6'h01	G9	G424	G17	G416
6'h02	G17	G416	G33	G400
6'h03	G25	G408	G49	G384
6'h04	G33	G400	G65	G368
6'h05	G41	G392	G81	G352
6'h06	G49	G384	G97	G336
6'h07	G57	G376	G113	G320
6'h08	G65	G368	G129	G304
6'h09	G73	G360	G145	G288
6'h0A	G81	G352	G161	G272
6'h0B	G89	G344	G177	G256
6'h0C	G97	G336	G193	G240
6'h0D	G105	G328	G209	G224
6'h0E	G113	G320	G225	G208
6'h0F	G121	G312	G241	G192
6'h10	G129	G304	G257	G176
6'h11	G137	G296	G273	G160
6'h12	G145	G288	G289	G144
6'h13	G153	G280	G305	G128
6'h14	G161	G272	G321	G112
6'h15	G169	G264	G337	G96
6'h16	G177	G256	G353	G80
6'h17	G185	G248	G369	G64
6'h18	G193	G240	G385	G48
6'h19	G201	G232	G401	G32
6'h1A	G209	G224	G417	G16
6'h1B	G217	G216	G2	G431
6'h1C	G225	G208	G18	G415
6'h1D	G233	G200	G34	G399
6'h1E	G241	G192	G50	G383
6'h1F	G249	G184	G66	G367
6'h20	G257	G176	G82	G351
6'h21	G265	G168	G98	G335
6'h22	G273	G160	G114	G319
6'h23	G281	G152	G130	G303
6'h24	G289	G144	G146	G287
6'h25	G297	G136	G162	G271
6'h26	G305	G128	G178	G255
6'h27	G313	G120	G194	G239
6'h28	G321	G112	G210	G223
6'h29	G329	G104	G226	G207
6'h2A	G337	G96	G242	G191
6'h2B	G345	G88	G258	G175
6'h2C	G353	G80	G274	G159
6'h2D	G361	G72	G290	G143
6'h2E	G369	G64	G306	G127
6'h2F	G377	G56	G322	G111

6'h30	G385	G48	G338	G95
6'h31	G393	G40	G354	G79
6'h32	G401	G32	G370	G63
6'h33	G409	G24	G386	G47
6'h34	G417	G16	G402	G31
6'h35	G425	G8	G18	G15
6'h3D-6'h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Software Reset (R70h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST

SRST – When SRST = 1, software is reset.
When SRST = 0, software reset is canceled.

I/F Endian Control (R71h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCREV[1:0]	

TCREV[1:0] – Controls the endian setting (big/little endian: the order of reveiving data) when transferring one-pixel data via i80 interface inmultiple times. When setting a new value to TCREV[1:0], the order is changed from when the next instruction is executed.

Table 57

TCREV[1:0	**2 Transfers / Pixel**	**3 Transfers / Pixel**
2'h0	Upper to lower(1^{st} to 2^{nd})	Upper to lower(1^{st},2^{nd}, 3^{rd})
2'h1	Setting disabled	Setting disabled
2'h2	Setting disabled	Setting disabled
2'h3	Lower to upper(2^{nd} to 1^{st})	Lower to upper(3^{rd}, 2^{nd}, 1^{st})

Notes : 1. In read operation, the data is transferred from upper bits to lower bits (big endian) regardless of TCREV[1:0] setting.
2. Make sure to set TCREV[1:0] when executing reset or exiting from shutdown mode.

Partial Image 1: Display Position (R80h)

RAM Address (Start/End Line Address) (R81h/R82h)

Partial Image 2: Display Position (R83h)

RAM Address (Start/End Line Address) (R84h/R85h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	PTDP0[8:0]								
W	1	0	0	0	0	0	0	0	PTSA0[8:0]								
W	1	0	0	0	0	0	0	0	PTEA0[8:0]								
W	1	0	0	0	0	0	0	0	PTDP1[8:0]								
W	1	0	0	0	0	0	0	0	PTSA1[8:0]								
W	1	0	0	0	0	0	0	0	PTEA1[8:0]								

PTDP0[8:0] – Sets the display position of partial image 1.
PTDP1[8:0] – Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting make sure that

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display position : (PTDP0, PTEA0)
Coordinates of partial image 2 display position : (PTDP1, PTEA1)

If PTDP0 = 9'h000, the partial image 1 is displayed from the first line of the base image.

PTSA0[8:0] – Sets the start line addresses of the RAM area, respectively for the partial image 1

PTEA0[8:0] – Sets the end display position of partial image 1.

PTSA1[8:0] – Sets the start line addresses of the RAM area, respectively for the partial image 2.

PTEA1[8:0] – Sets the end display position of partial image 2.

Panel Interface Control 1 (R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI[1:0]		RTNI[7:1]							0

RTNI[7:1] – Sets 1H (line) period. This setting is enabled while the LGDP4551's display operation is synchronized with internal clock. RTNI[7:1] should be greater than or equal to 60 (= 3Ch).

DIVI[1:0] – Sets the division ratio of the internal clock frequency. The LGDP4551's internal operation is synchronized with the frequency divided internal clock. When changing the DIVI[1:0] bits, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see "Frame-Frequency Adjustment Function". The setting in DIVI[1:0] is disabled in RGB interface operation.

Frame Frequency Calculation

Frame frequency = fosc/(clock cycles per line x division ratio x (active line + BP + FP))

Table 58 clocks per line (internal clock operation 1 clock = 1 OSC)

RTNI[7:1]	Clock per Line
8'h00 – 8'h3B	Setting disabled
8'h3C	60 clocks
8'h3E	62 clocks
8'h40	64 clocks
8'h42	66 clocks
…….	
8'hFC	252 clocks
8'hFE	254 clocks

Table 59 Division ratio of the internal clock

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

Panel Interface Control 2 (R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOWI[2:0]			0	0	0	0	EQI2[1:0]		EQI1[1:0]	

EQI1[1:0] – Sets equalization period.

Note : when VCOML >= 0V, EQI1,EQI2 setting is disabled.

Table 60

EQI1[1:0]	Equalization period
2'h0	0 (internal clock period [see note])
2'h1	2
2'h2	4
2'h3	6

EQI2[1:0] – Sets equalization period.

Table 61

EQI2[1:0]	Equalization period
2'h0	0 (internal clock period [see note])
2'h1	2
2'h2	4
2'h3	6

NOWI[2:0] – Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation in synchronization with internal clock.

Table 62

NOWI[2:0]	Non-overlap period
3'h0	0 (internal clock period [see note])
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note : The internal clock is the frequency divided clock with the division ratio set with the DIVI[1:0] bits.

Panel Interface Control 3 (R93h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SEQI[2:0]			0	0	0	0	0	MCPI[2:0]		

MCPI[2:0] – Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation in synchronization with internal clock.

Table 63

MCPI[2:0]	Source output position
3'h0	0 (internal clock period [see note])
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note: The internal clock is the frequency divided clock with the division ratio set with the DIVI[[1:0] bits. The source output position is measured from a reference point by the number of internal clock cycle.

SEQI[2:0] – Sets Source equalization period.

Table 64

SEQI[2:0]	Source equalization periold
3'h0	0 (internal clock periold see note)
3'h1	2
3'h2	4
3'h3	6
3'h4	8
3'h5	10
3'h6	12
3'h7	14

Panel Interface Control 4 (R95h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE[1:0]		RTNE[7:1]							0

RTNE[7:1] – Sets the number of internal clocks per 1H (line) period. Set the value that represents the number of DOTCLKs divided by the division ratio, which is input in a 1H period. RTNE[7:0] should be greater than or equal to 60 (= 3Ch).

DIVE[1:0] – Sets DIVE, the internal division ratio of DOTCLK. The internal operation is performed according to the clocks divided by the internal division ratio DIVE.

Table 65 Division ratio of DOTCLK

DIVE[1:0]	Division Ratio	Internal operation clock unit (DOTCLK)			
		18-bit, 1 transfer RGB interface	DOTCLK = 5 MHz	8-bit, 3 transfer RGB interface	DOTCLK = 15 MHz
2'h0	Setting disabled	Setting disabled	-	Setting disabled	-
2'h1	1/1	1 DOTCLKs	0.2 µs	3 DOTCLKs	0.2 µs
2'h2	1/2	2 DOTCLKs	0.4 µs	6 DOTCLKs	0.4 µs
2'h3	1/4	4 DOTCLKs	0.8 µs	12 DOTCLKs	0.8 µs

Table 66 DOTCLK per line (1H period)

RTNE[7:0]	DOTCLK per line (1H)
8'h00 – 8'h3B	Setting disabled
8'h3C	60 clocks
8'h3E	62 clocks
8'h40	64 clocks
8'h42	66 clocks
…….	
8'hFC	252 clocks
8'hFE	254 clocks

Panel Interface Control 5 (R97h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	NOWE[3:0]				0	0	0	0	EQE2[1:0]		EQE1[1:0]	

EQE1[1:0] – Sets equalization period.

Note : when VCOML >= 0V, EQE1,EQE2 setting is daiabled.

Table 67

EQE1[1:0]	Equalization period
2'h0	0 (internal clock period see note)
2'h1	2
2'h2	4
2'h3	6

EQE2[1:0] – Sets equalization period.

Table 68

EQE2[1:0]	Equalization period
2'h0	0 (internal clock period see note)
2'h1	2
2'h2	4
2'h3	6

NOWE[3:0] – Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

Table 69

NOWE[3:0]	Non-overlap period	NOWE[3:0]	Non-overlap period
4'h0	0 (internal clock period see note)	4'h8	32
4'h1	4	4'h9	36
4'h2	8	4'hA	40
4'h3	12	4'hB	44
4'h4	16	4'hC	48
4'h5	20	4'hD	52
4'h6	24	4'hE	56
4'h7	28	4'hF	60

Note : 1 clock = (Number of data transfers / pixel) x DIVE (division ratio) [DOTCLK].

Panel Interface Control 6 (R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2:0]		

MCPE[2:0] – Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation via RGB interface.

Table 70

MCPE[2:0]	Source output position
3'h0	0 (internal clock period see note)
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note : 1 clock = (Number of data transfers / pixel) x DIVE (division ratio) [DOTCLK].

SEQE[2:0] – Sets Source equalization period.

Table 71

SEQE[2:0]	Source equalization periold
3'h0	0 (internal clock periold see note)
3'h1	2
3'h2	4
3'h3	6
3'h4	8
3'h5	10
3'h6	12
3'h7	14

Frame Rate Control (R9Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	OHZ	0	0	0	FRS[4:0]				

FRS[4:0] – Set the frame rate when the internal resistor is used for oscillator circuit.
Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation via RGB interface.

OHZ – Set the test mode
OHZ = 0 – FMARK pin is normal output..
OHZ = 1 – FMARK pin is clock input for test.

Table 72

FRS[4:0]	Ratio of frequency	FRS[4:0]	Ratio of frequency
5'h00	x 0.18	5'h10	x 2.06
5'h01	x 0.33	5'h11	x 2.17
5'h02	x 0.40	5'h12	x 2.22
5'h03	x 0.54	5'h13	x 2.33
5'h04	x 0.60	5'h14	x 2.39
5'h05	x 0.74	5'h15	x 2.50

5'h06	x 0.81	5'h16	x 2.57
5'h07	x 0.94	5'h17	x 2.63
5'h08	x 1.00 (default)	5'h18	x 2.70
5'h09	x 1.13	5'h19	x 2.79
5'h0A	x 1.19	5'h1A	x 2.86
5'h0B	x 1.31	5'h1B	x 2.93
5'h0C	x 1.37	5'h1C	x 2.99
5'h0D	x 1.50	5'h1D	x 3.08
5'h0E	x 1.56	5'h1E	x 3.16
5'h0F	x 1.67	5'h1F	x 3.23

Note : When the default OSC frequency(FRS[4:0]=5'h08) is 3MHz and the register setting is FRS[4:0]=5'h0D , then OSC frequency = 3MHz x 1.50 = 4.5 MHz.

Test Register 1 (RA0h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	TDLY[1:0]		0	0	0	TDFN	0	0	TFOSC	TOSC	0	0	TVCOM[1:0]	

TVCOM[1:0] – Sets the Vcom output level for test.

Table 73

TVCOM [1:0]	**Vcom Level**
2'h0	modulation
2'h1	modulation
2'h2	VCOML
2'h3	VCOMH

TOSC – Sets for the oscillator test.
TFOSC – Sets for the oscillator delay test.
TDFN – Sets for the function test.
TMEM – Sets for the memory test.
TDLY[1:0] – Sets for the delay time test.

Test Register 2 (RA1h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	REGULPD	0	0	0	TSAP	0	0	TSHZ	TPATE	0	TPAT[2:0]		

TSHZ – Sets
TSAP – Sets
REGULPD – Sets
TPATE – Sets
TPAT[2:0] – Sets

Test Register 3 (RA2h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	T8CL	0	0	0	TVRHZ	0	0	0	TVON	0	HaltVreg	MultiVci	

MultiVci – Used for Device Test.
HaltVreg – Used for Device Test.
TVON – Used for Device Test.
TVRHZ – Used for Device Test
T8CL – Used for 8 color mode test

Test Register 4 (RA3h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	RDSM[1:0]		0	0	WRPW[1:0]	

WRPW[1:0] – Used for memory write pulse width test.
RDSM[1:0] – Used for memory read sensing margin test.

Test Register 5 (RA4h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	S_HIZ	0	0	0	SBC

SBC – Source Bias controlUsed for memory write pulse width test.
S_HIZ – stepup2 .

Test Register 6 (RA5h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	RS_RESET	0	0	0	OV

OV – Set data overwrite enable.
OV = 1 : data overwrite disable
OV = 0 : data overwrite enable.

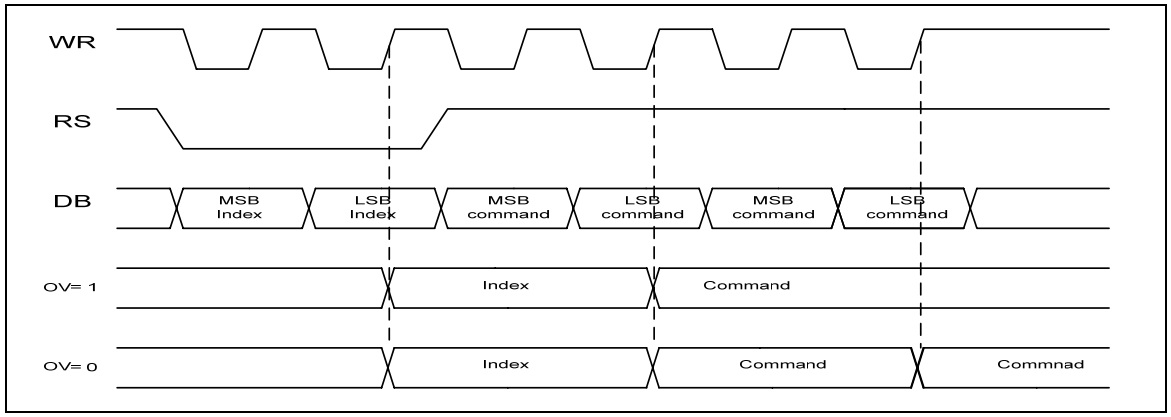


Figure 14

RS_RESET – Set .internal conuter reset enable.
RS_RESET = 1 : internal data counter reset enable
RS_RESET = 0 : internal data counter reset disable

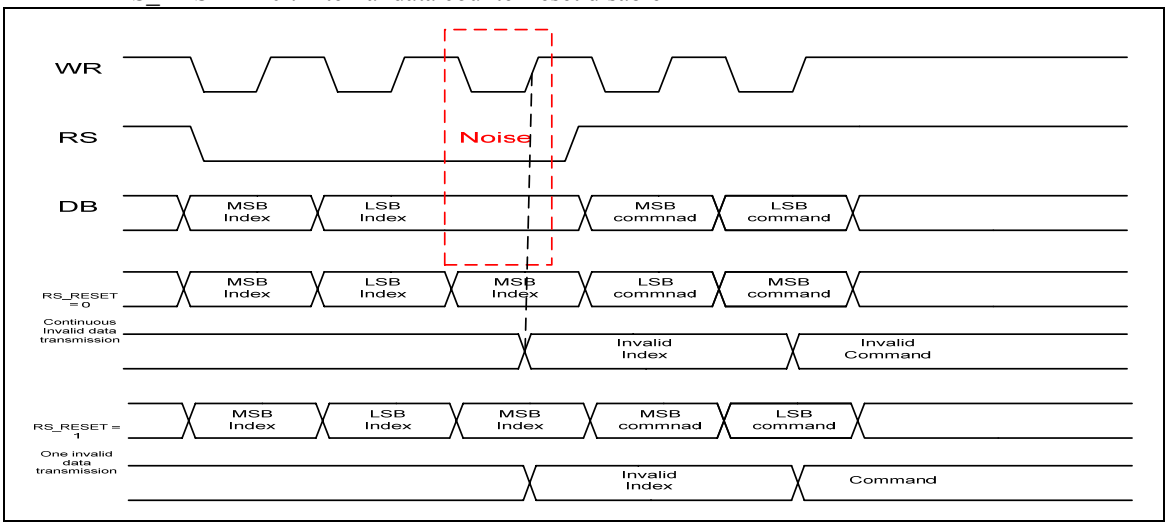


Figure 15

Green Gamma Control 1-16 (RB0h to RBFh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				
W	1						PFP1[2:0]								PFP0[2:0]		
W	1						PFP3[2:0]								PFP2[2:0]		
W	1						PFN1[2:0]								PFN0[2:0]		
W	1						PFN3[2:0]								PFN2[2:0]		
W	1														PMP[2:0]		
W	1														PMN[2:0]		

PKP5-0[2 :0] – γ fine-adjustment register for positive polarity
PRP1-0[2 :0] – γ gradient-adjustment register for positive polarity
VRP0[3:0], R_VRP1[4 :0] – γ amplitude-adjustment register for positive polarity

PKN5-0[2 :0] – γ fine-adjustment register for negative polarity
PRN1-0[2 :0] – γ gradient-adjustment register for negative polarity
VRN0[3:0], VRN1[4 :0] – γ amplitude-adjustment register for negative polarity

PFP3-0[2:0] – γ fine adjustment register bits for positive polarity
PFN3-0[2:0] – γ fine adjustment register bits for negative polarity
PMP[2:0] – γ fine adjustment register bits for positive polarity
PMN[2:0] – γ fine adjustment register bits for negative polarity

Blue Gamma Control 1-16 (RC0h to RCFh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				
W	1						PFP1[2:0]								PFP0[2:0]		
W	1						PFP3[2:0]								PFP2[2:0]		
W	1						PFN1[2:0]								PFN0[2:0]		
W	1						PFN3[2:0]								PFN2[2:0]		
W	1														PMP[2:0]		
W	1														PMN[2:0]		

PKP5-0[2 :0] – γ fine-adjustment register for positive polarity
PRP1-0[2 :0] – γ gradient-adjustment register for positive polarity
VRP0[3:0], R_VRP1[4 :0] – γ amplitude-adjustment register for positive polarity

PKN5-0[2 :0] – γ fine-adjustment register for negative polarity
PRN1-0[2 :0] – γ gradient-adjustment register for negative polarity

VRN0[3:0], VRN1[4 :0] – γ amplitude-adjustment register for negative polarity

PFP3-0[2:0] – γ fine adjustment register bits for positive polarity
PFN3-0[2:0] – γ fine adjustment register bits for negative polarity
PMP[2:0] – γ fine adjustment register bits for positive polarity
PMN[2:0] – γ fine adjustment register bits for negative polarity

Note)
When BGR='1', these register setting values are for Red Gamma Control.

Instruction List

Index	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	Start oscillation																1
01h	Driver output control 1						SM (0)		SS (0)								
02h	LCD Driving Wave Control							BC0 (0)	EOR (0)			NW[5:0] (000000)					
03h	Entry mode	TRI (0)	DFM (0)		BGR (0)					ORG (0)		ID[1:0] (11)		AM (0)		EPF[1:0] (00)	
04h	Resizing Control							RCV[1:0] (00)				RCH[1:0] (00)				RSZ[1:0] (00)	
07h	Display Control 1			PTDE[1:0] (00)					BASEE (0)			GON (0)	DTE (0)	COL (0)		D[1:0] (00)	
08h	Display Control 2					FP[3:0] (1000)								BP[3:0] (1000)			
09h	Display Control 3						PTS[2:0] (000)					PTG[1:0] (00)		ISC[3:0] (0000)			
0Ah	Display Control 4													FMARKOE (0)	FMI[2:0] (000)		
0Ch	External display Interface Control 1			ENC[1:0] (000)					RM (0)			DM[1:0] (00)				RIM[1:0] (00)	
0Dh	Frame Marker Position							FMP[8:0] (000000000)									
0Fh	External display Interface Control 2												VSPL (0)	HSPL (0)		EPL (0)	DPL (0)
10h	Power Control 1		SAP[2:0] (000)				BT[2:0] (0000)				AP[2:0] (000)			DK (1)	DSTB (0)	SLP (0)	STB (0)
11h	Power Control 2						DC1[2:0] (110)				DC0[2:0] (110)				VC[2:0] (000)		
12h	Power Control 3												PON (0)	VRH[3:0] (0000)			
13h	Power Control 4			VCOMG (0)	VDV[4:0] (00000)						VCM[6:0] (0000000)						
15h	Regulator Control		RSET[2:0] (010)				RI[2:0] (000)				RV[2:0] (011)				RCONT (000)		
16h	Gamma Select Control								SGE (0)				EN_MA (0)				PS (0)
17h	Vcom Control						LSZ[2:0] (000)				HSZ[2:0] (000)						CMFPD (1)
20h	RAM Address Set (Horizontal Address)									AD[7:0] (00000000)							
21h	RAM Address Set (Vertical Address)								AD[16:8] (000000000)								
22h	RAM Data	WD[17:0] or RD[17:0]															
30h	Red Gamma Control 1						PKP1[2:0] (000)								PKP0[2:0] (000)		
31h	Red Gamma Control 2						PKP3[2:0] (000)								PKP2[2:0] (000)		
32h	Red Gamma Control 3						PKP5[2:0] (000)								PKP4[2:0] (000)		
33h	Red Gamma Control 4						PRP1[2:0] (000)								PRP0[2:0] (000)		
34h	Red Gamma Control 5						PKN1[2:0] (000)								PKN0[2:0] (000)		
35h	Red Gamma Control 6						PKN3[2:0] (000)								PKN2[2:0] (000)		
36h	Red Gamma Control 7						PKN5[2:0] (000)								PKN4[2:0] (000)		
37h	Red Gamma Control 8						PRN1[2:0] (000)								PRN0[2:0] (000)		
38h	Red Gamma Control 9				VRP1[4:0] (00000)								VRP0[4:0] (00000)				
39h	Red Gamma Control 10				VRN1[4:0] (00000)								VRN0[4:0] (00000)				
3Ah	Red Gamma Control 11						PFP1[2:0] (001)								PFP0[2:0] (001)		
3Bh	Red Gamma Control 12						PFP3[2:0] (001)								PFP2[2:0] (001)		
3Ch	Red Gamma Control 13						PFN1[2:0] (001)								PFN0[2:0] (001)		
3Dh	Red Gamma Control 14						PFN3[2:0] (001)								PFN2[2:0] (001)		
3Eh	Red Gamma Control 15														PMP[2:0] (001)		

3Fh	Red Gamma Control 16														PMN[2:0] (001)		
40h	EPROM Control 1	PTM[1:0] (00)		POR (0)	VPP (0)	PPROG (0)	PWE (0)	PA[1:0] (00)		PDIN[7:0] (00000000)							
41h	EPROM Control 2												AUTOWR (0)	RA[1:0] (00)		VCMSEL[1:0] (00)	
42h	EPROM Control 3									PDOUT[7:0] (11111111)							
50h	Window Horizontal RAM Start Address									HSA[7:0] (00000000)							
51h	Window Horizontal RAM End Address									HEA[7:0] (11101111)							
52h	Window Vertical RAM Start Address								VSA[8:0] (000000000)								
53h	Window Vertical RAM End Address								VEA[8:0] (110101111)								
60h	Driver Output Control 2	GS (0)		NL[5:0] (000000)								SCN[5:0] (000000)					
61h	Base Image Display Control														NDL (0)	VLE (0)	REV (0)
6Ah	Vertical Scroll Control								VL[8:0] (000000000)								
70h	Software Reset																SRST (0)
71h	I/F Endian Control															TCREV[1:0] (00)	
80h	Partial Image 1 Display Position								PTDP0[8:0] (000000000)								
81h	Partial Image 1 RAM Start Line Address								PTSA0[8:0] (000000000)								
82h	Partial Image 1 RAM End Line Address								PTEA0[8:0] (000000000)								
83h	Partial Image 2 Display Position								PTDP1[8:0] (000000000)								
84h	Partial Image 2 RAM Start Line Address								PTSA1[8:0] (000000000)								
85h	Partial Image 2 RAM End Line Address								PTEA1[8:0] (000000000)								
90h	Panel Interface Control 1							DIVI[1:0] (00)		RTNI[7:1] (0101101)							
92h	Panel Interface Control 2						NOWI[2:0] (000)							EQI2[1:0] (00)		EQI1[1:0] (00)	
93h	Panel Interface Control 3						SEQI[2:0] (000)								MCPI[2:0] (000)		
95h	Panel Interface Control 4							DIVE[1:0] (00)		RTNE[7:0] (01011010)							
97h	Panel Interface Control 5					NOWE[3:0] (0000)								EQE2[1:0] (00)		EQE1[1:0] (00)	
98h	Panel Interface Control 6						SEQE[2:0] (000)								MCPE[2:0] (000)		
9Ah	Frame Rate and Color Control								OHZ (0)				FRS[4:0] (01000)				
A0h	Test register 1			TDLY (00)					TDFN (0)			TFOSC (0)	TOSC (0)			TVCOM[1:0] (00)	
A1h	Test register 2				REGULPD (0)				TSAP (0)			TSHZ (0)	TPATE (0)		TPAT[2:0] (000)		
A2h	Test register 3				T8CL (0)				TVRHZ (0)				TVON (0)		HaltVreg (0)	MultiVci (1)	
A3h	Test register 4											RDSM (00)				WRPW (00)	
A4h	Test register 5												S_HIZ (0)				SBC (0)
A5h	Test register 6												RS_RESET (0)				OV (0)
B0h	Green Gamma Control 1						PKP1[2:0] (000)								PKP0[2:0] (000)		
B1h	Green Gamma Control 2						PKP3[2:0] (000)								PKP2[2:0] (000)		
B2h	Green Gamma Control 3						PKP5[2:0] (000)								PKP4[2:0] (000)		
B3h	Green Gamma Control 4						PRP1[2:0] (000)								PRP0[2:0] (000)		
B4h	Green Gamma Control 5						PKN1[2:0] (000)								PKN0[2:0] (000)		

B5h	Green Gamma Control 6						PKN3[2:0] (000)											PKN2[2:0] (000)	
B6h	Green Gamma Control 7						PKN5[2:0] (000)											PKN4[2:0] (000)	
B7h	Green Gamma Control 8						PRN1[2:0] (000)											PRN0[2:0] (000)	
B8h	Green Gamma Control 9					VRP1[4:0] (00000)											VRP0[4:0] (00000)		
B9h	Green Gamma Control 10					VRN1[4:0] (00000)											VRN0[4:0] (00000)		
BAh	Green Gamma Control 11						PFP1[2:0] (001)											PFP0[2:0] (001)	
BBh	Green Gamma Control 12						PFP3[2:0] (001)											PFP2[2:0] (001)	
BCh	Green Gamma Control 13						PFN1[2:0] (001)											PFN0[2:0] (001)	
BDh	Green Gamma Control 14						PFN3[2:0] (001)											PFN2[2:0] (001)	
BEh	Green Gamma Control 15																	PMP[2:0] (001)	
BFh	Green Gamma Control 16																	PMN[2:0] (001)	
C0h	Blue Gamma Control 1						PKP1[2:0] (000)											PKP0[2:0] (000)	
C1h	Blue Gamma Control 2						PKP3[2:0] (000)											PKP2[2:0] (000)	
C2h	Blue Gamma Control 3						PKP5[2:0] (000)											PKP4[2:0] (000)	
C3h	Blue Gamma Control 4						PRP1[2:0] (000)											PRP0[2:0] (000)	
C4h	Blue Gamma Control 5						PKN1[2:0] (000)											PKN0[2:0] (000)	
C5h	Blue Gamma Control 6						PKN3[2:0] (000)											PKN2[2:0] (000)	
C6h	Blue Gamma Control 7						PKN5[2:0] (000)											PKN4[2:0] (000)	
C7h	Blue Gamma Control 8						PRN1[2:0] (000)											PRN0[2:0] (000)	
C8h	Blue Gamma Control 9					VRP1[4:0] (00000)											VRP0[4:0] (00000)		
C9h	Blue Gamma Control 10					VRN1[4:0] (00000)											VRN0[4:0] (00000)		
CAh	Blue Gamma Control 11						PFP1[2:0] (001)											PFP0[2:0] (001)	
CBh	Blue Gamma Control 12						PFP3[2:0] (001)											PFP2[2:0] (001)	
CCh	Blue Gamma Control 13						PFN1[2:0] (001)											PFN0[2:0] (001)	
CDh	Blue Gamma Control 14						PFN3[2:0] (001)											PFN2[2:0] (001)	
CEh	Blue Gamma Control 15																	PMP[2:0] (001)	
CFh	Blue Gamma Control 16																	PMN[2:0] (001)	

Reset Function

The LGDP4551 is initialized with a RESET input. During a reset period, the LGDP4551 is in a busy state and neither instruction nor access to the GRAM data from the MPU is accepted. The LGDP4551's internal power supply circuit unit is initialized also with a RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, neither access to the internal GRAM nor initial setting of instruction bits is accepted.

1. Initial state of instruction bits (default)
See the instruction list. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization
The RAM data is not automatically initialized with a RESET input and must be initialized by software in a display-off period (D1-0 = "00").

3. Output pin initial state *See note

1. LCD driver S1~S720	: GND
G1~G432 : VGL (= GND)	
2. Vcom	: GND
3. VcomDC	: GND
4. VRS	: GND
5. VCS	: GND
6. VREG1OUT	: VGS
7. VciOUT	: Hi-z
8. VLOUT1	: Vci
9. VLOUT2	: DDVDH (= Vci)
10. VLOUT3	: GND
11. FMARK	: GND
12. Oscillator	: Oscillate
13. SDO	: GND

4. Initial state of input/output pins*See note

1. C11+	: Hi-z
2. C11-	: Hi-z
3. C12+	: Hi-z
4. C12-	: Hi-z
5. C13+	: Vci1
6. C13-	: GND
7. C21+	: DDVDH (= Vci)
8. C21-	: GND
9. C22+	: DDVDH (= Vci)
10. C22-	: GND
11. C23+	: DDVDH (= Vci)
12. C23-	: GND
13. VDD	: VDD

Note: The above-mentioned initial states of output and input pins are the ones when the LGDP4551's power supply circuit is connected as exemplified in "Wiring example".

5. Note on Reset function

(1) When a RESET input is entered into the LGDP4551 while it is in deep standby mode, the LGDP4551 starts up the inside logic regulator and makes a transition to the initial state. During this period, the interface pins may be under an unstable condition. For this reason, do not enter a RESET input in deep standby mode.

(2) When transferring instruction using either two or three transfer mode via 8-/9-/16-bit interface, make sure to execute a data transfer synchronization after executing a reset operation.

Basic Mode operation of the LGDP4551

The basic operation modes of the LGDP4551 are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

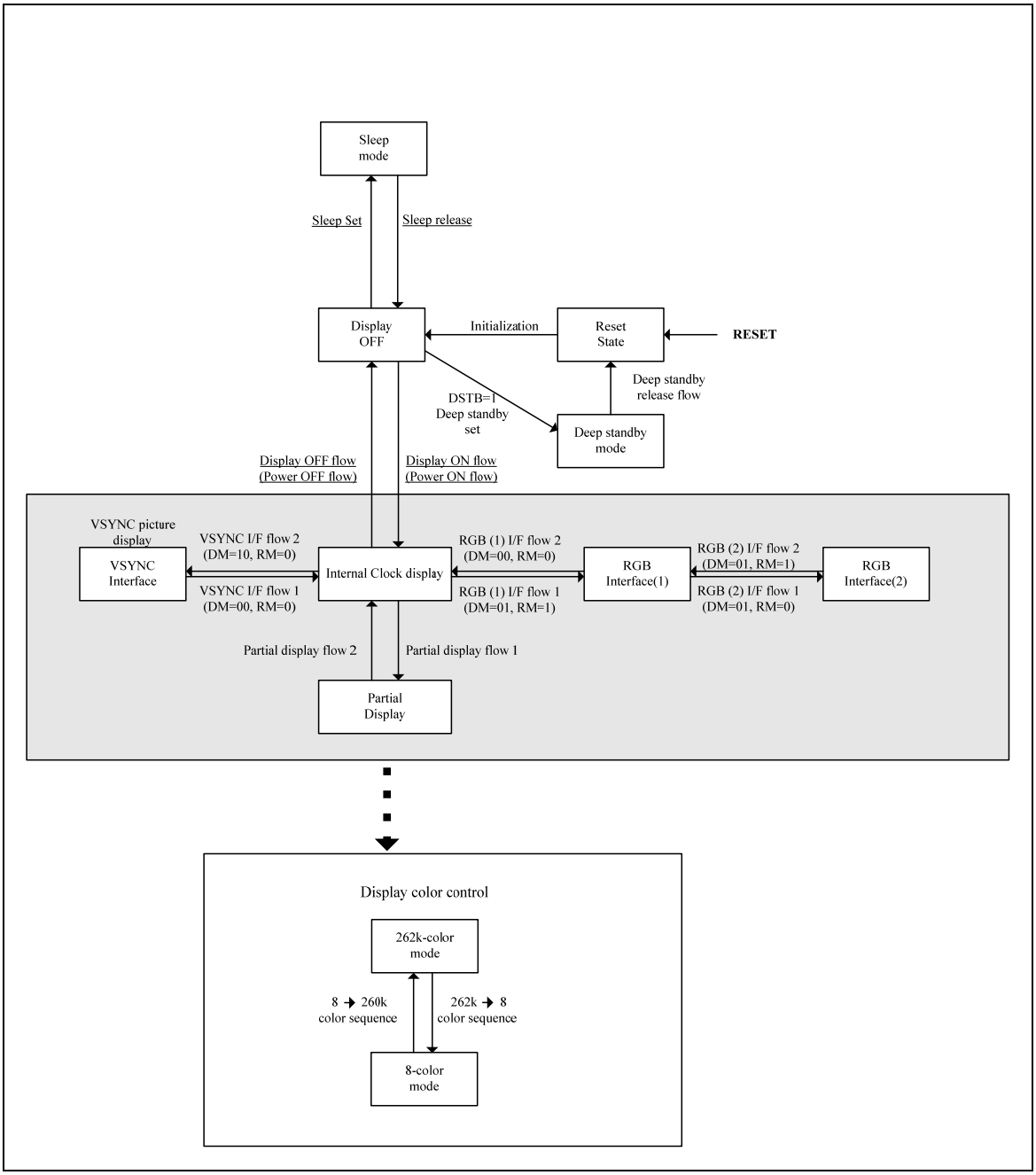


Figure 16

Interface and data format

The LGDP4551 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The LGDP4551 allows selecting an optimum interface according to the kind of display (moving or still picture) in order to transfer data efficiently.

As external display interface, the LGDP4551 supports RGB interface and VSYNC interface, both enabling data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the LGDP4551 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the LGDP4551's GRAM in order to minimize the data transfer by transferring data only when it is necessary to switch the moving picture frames. The window address function specifies the RAM area where data is rewritten for moving picture display and enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display using system interface by writing data to the GRAM at more than a certain speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in speed and methods of writing data to the internal RAM.

The LGDP4551 can operate in either one of the following four modes according to the state of display. The display operation mode is determined by setting the external interface control register. When switching between different modes, make sure to refer to mode switching sequence.

Table 74

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM[1:0]) while RGB interface is in operation.
4. See the "External Display Interface" section for the mode transition sequence.

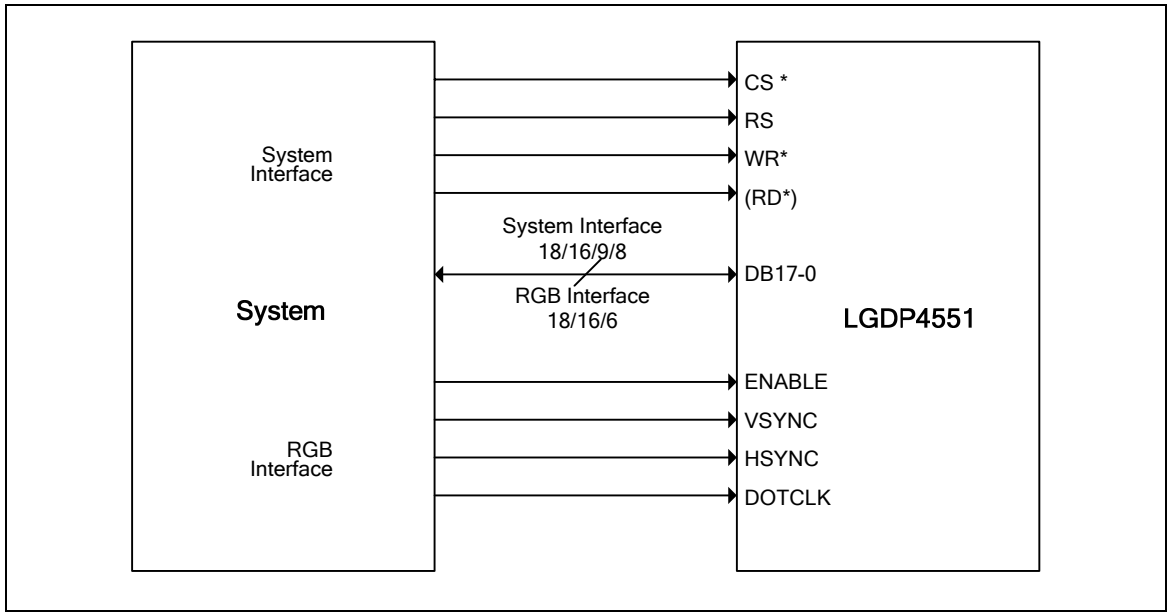


Figure 17 LGDP4551's Interface

Internal clock operation
The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. Any input via external display interface is invalid in this operation. The internal RAM is accessible only via system interface.

RGB interface operation (1)
The display operation is synchronized with the frame synchronous signal (VSYNC), the line synchronous signal (HSYNC), and the dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied throughout the display period using RGB interface.
The LGDP4551 transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function enables the LGDP4551 to display a moving picture and the data in other than the moving picture RAM area simultaneously and transferring only data to be overwritten in the moving picture RAM area when7 rewriting the moving picture RAM area. This structure can minimize the total number of data transfer.
The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the LGDP4551 by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with these settings.

RGB interface operation (2)
This mode enables the LGDP4551 to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first and then set a new address and the index register to R22h.

VSYNC interface operation
The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the LGDP4551 to display a moving picture using system interface by writing data to the internal RAM at more than a minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are constraints in speed and methods of writing RAM data. For details, see the "VSYNC Interface" section. As an external input, only VSYNC signal input is valid in this mode. Any other input via external display interface is invalid.
The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) according to the register settings inside the LGDP4551.

System Interface

The following are the kinds of system interfaces available with the LGDP4551. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 75

IM[2:0]	Interface Mode with MPU	DB pins	Colors
000	80-system 18-bit interface	DB17-0	262,144
001	80-system 9-bit interface	DB17-9	262,144
010	80-system 16-bit interface	DB17-10, DB8-1	262,144 *see Note 1
011	80-system 8-bit interface	DB17-10	262,144 *see Note 2
11*	Clock synchronous serial interface	SDI,SDO	65,536
10*	Setting disabled	-	-

Notes: 1. 65,536 colors in 16-bit signal transfer mode.
2. 65,536 colors in 8-bit 2-transfer mode.

80-system 18-bit Bus Interface

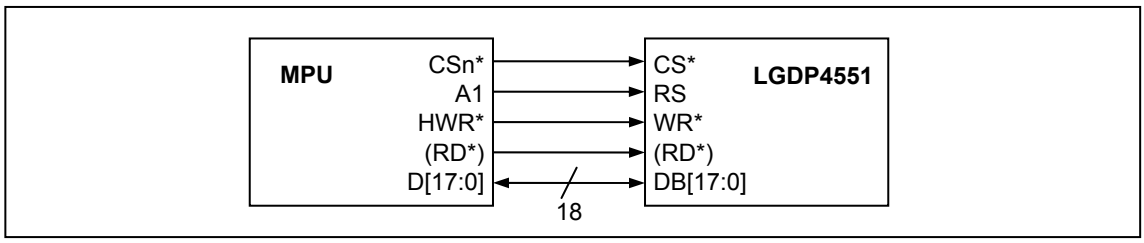


Figure 18 18-bit Interface

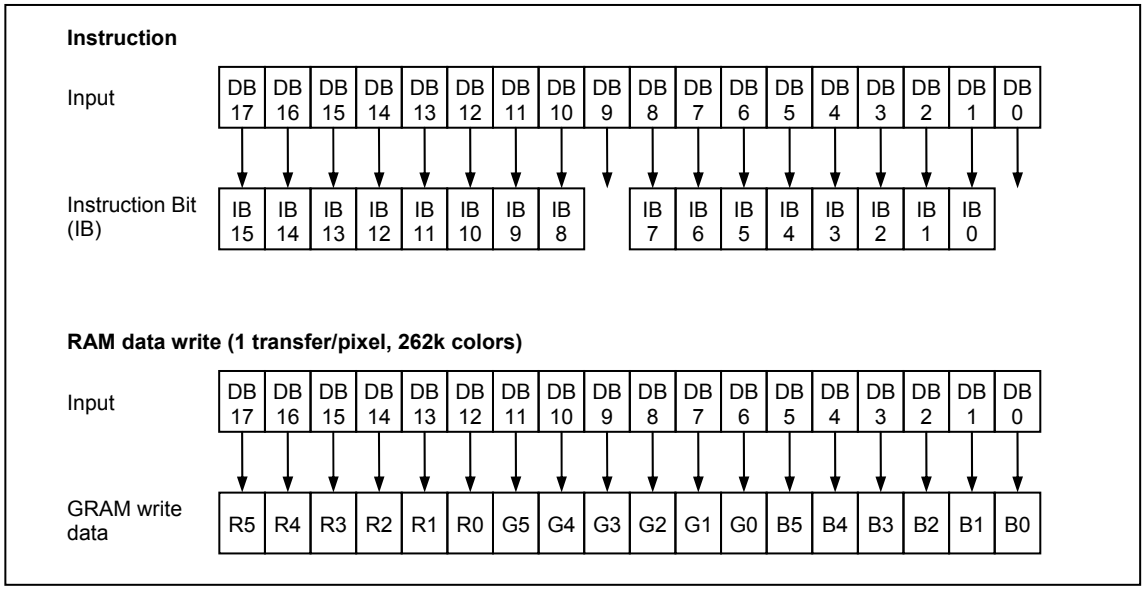


Figure 19 Data format for 18-bit interface

80-system 16-bit Bus Interface

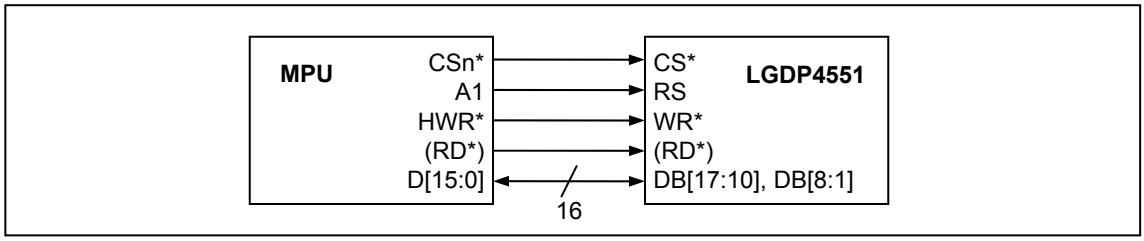


Figure 20 16-bit Interface

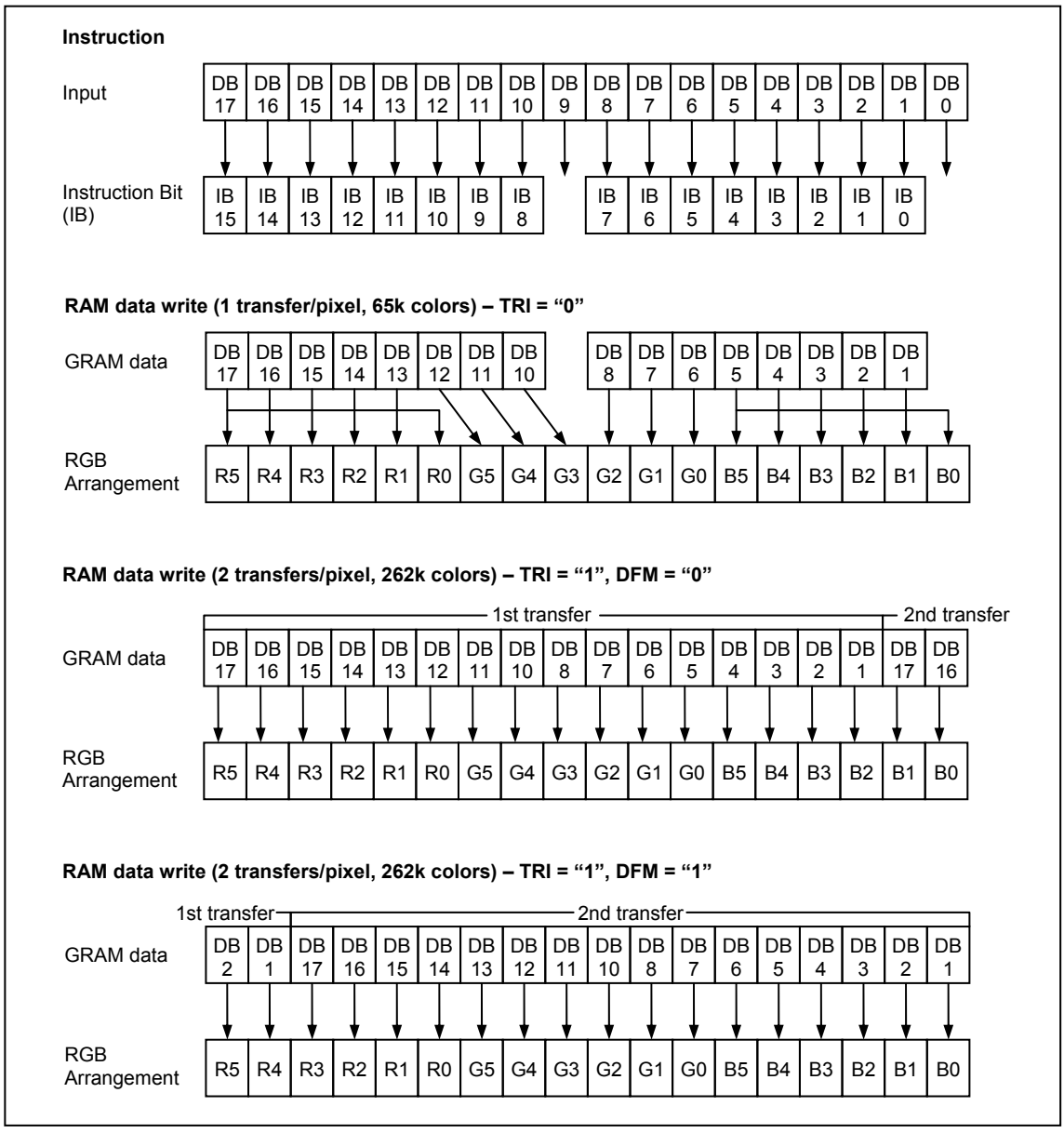


Figure 21 Data format for 16-bit interface

Data Transfer Synchronous in 16-bit Bus Interface operation

The LGDP4551 supports a data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 2/16 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

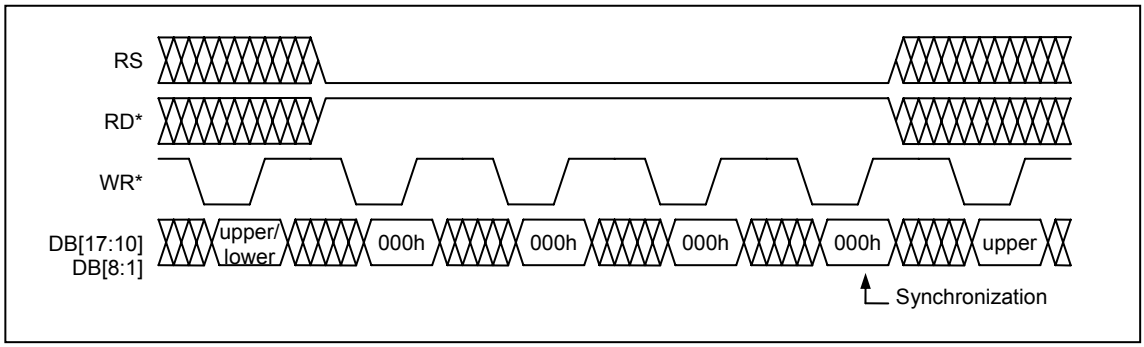


Figure 22 16-bit Data Transfer Synchronization

80-system 9-bit Bus Interface

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into the upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either the IOVcc or IOGND level. When writing to the index register, the upper byte (8 bits) must be written.

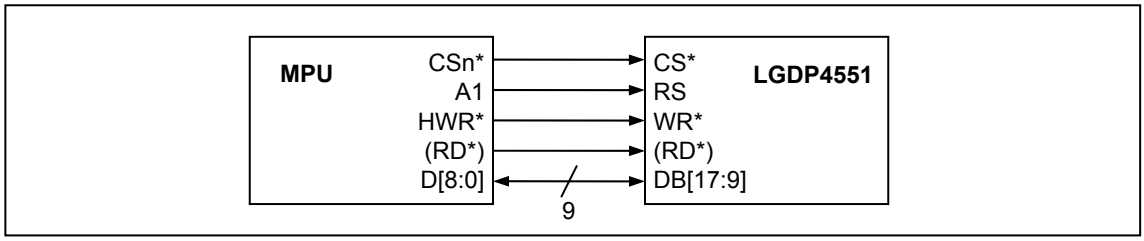


Figure 23 9-bit Intreface

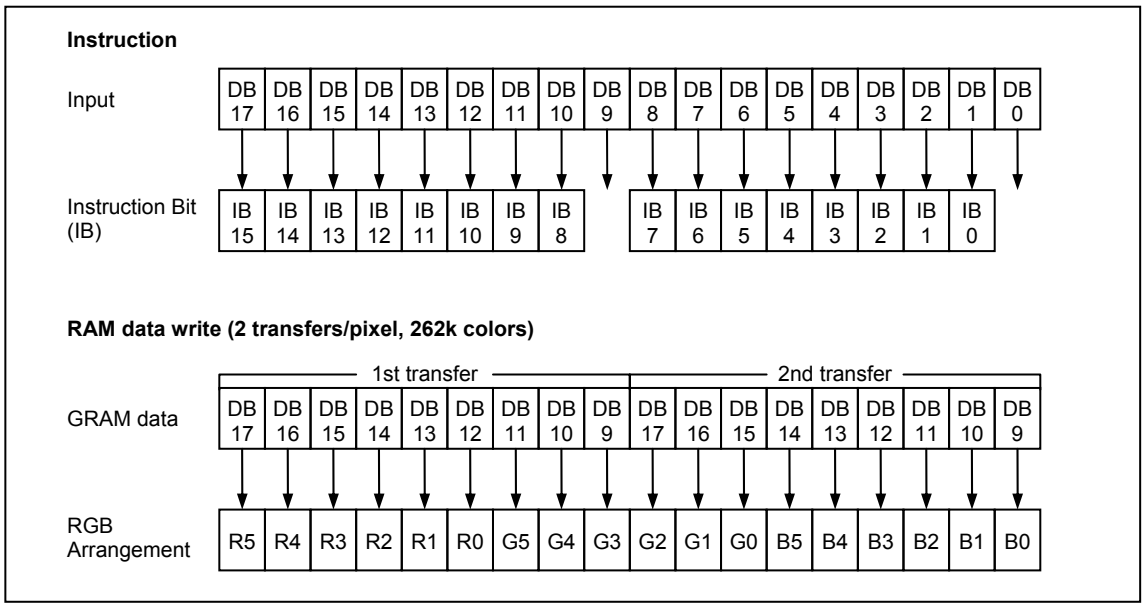


Figure 24 9-bit Intreface Data Format

Data Transfer Synchronous in 9-bit Bus Interface operation

The LGDP4551 supports a data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 9 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

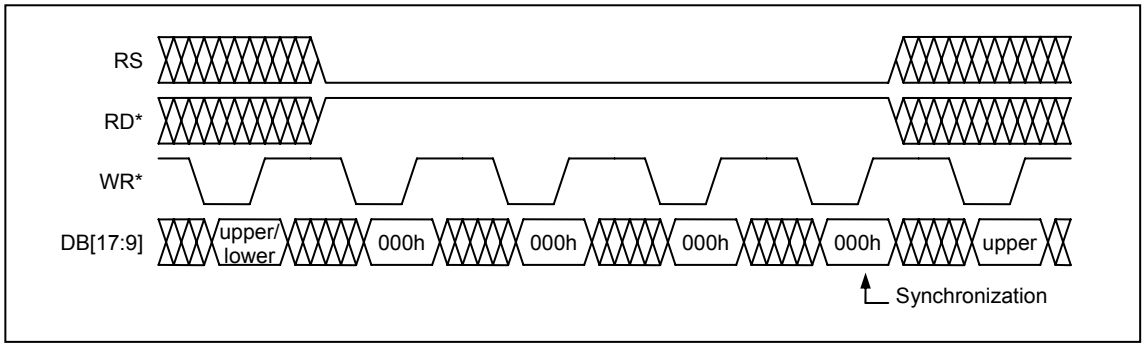


Figure 25 9-bit Data Transfer Synchronization

80-system 8-bit Bus Interface

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either the IOVcc or IOGND level. When writing the index register, the upper byte (8 bits) must be written.

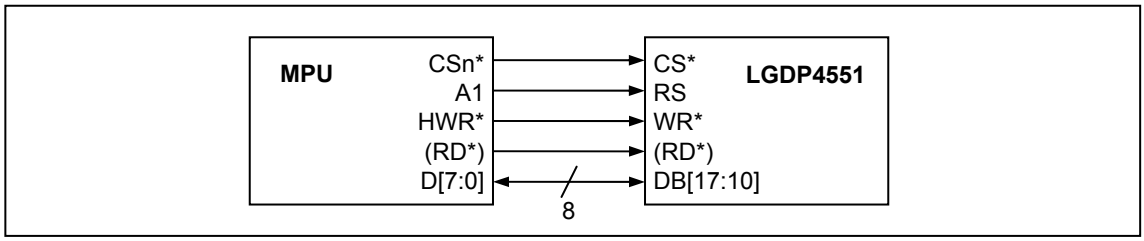


Figure 26 8-bit Interface

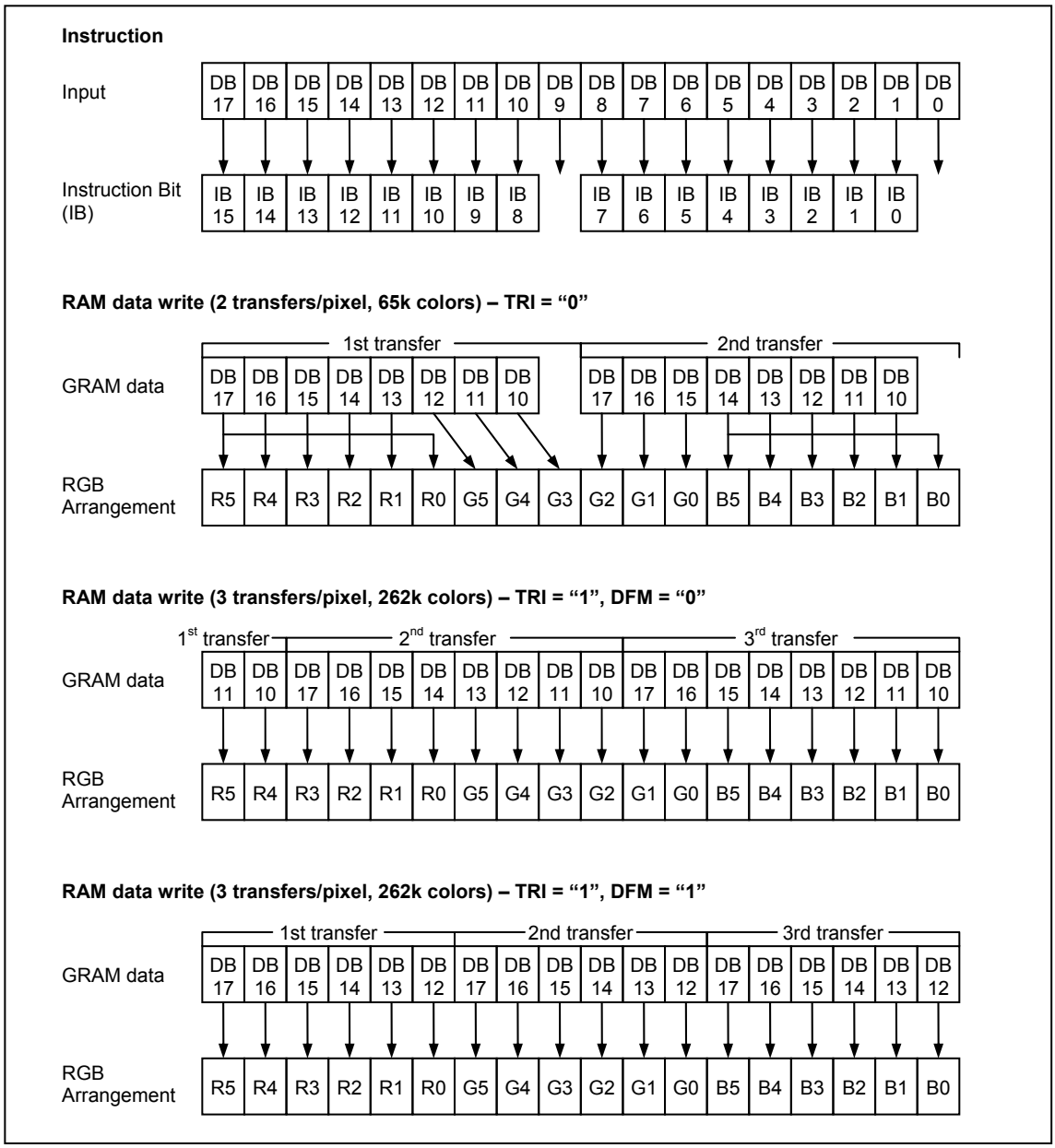


Figure 27 8-bit Intreface Data Format

Data Transfer Synchronous in 8-bit Bus Interface operation

The LGDP4551 supports a data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 8 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

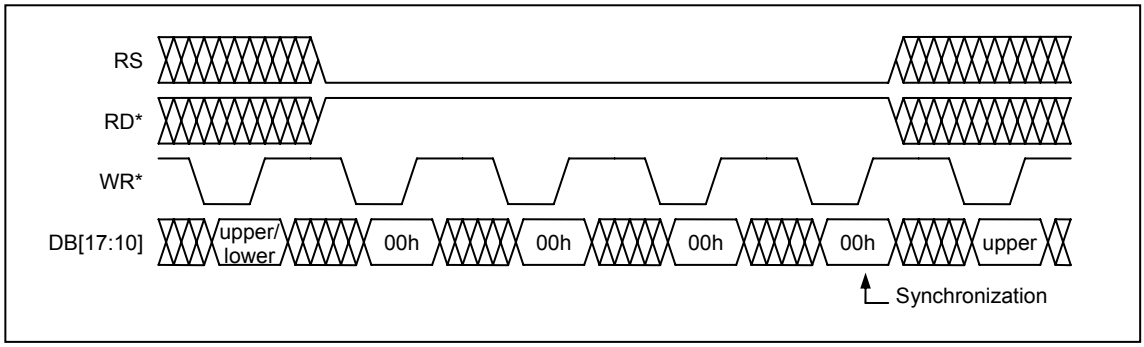


Figure 28 8-bit Data Transfer Synchronization

Serial Interface

The serial interface is selected by setting the IM3/2/1 pins to the IOGND/IOVcc/IOGND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The LGDP4551 recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The LGDP4551 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LGDP4551 are compared and both 6-bit data match, and then the LGDP4551 starts taking in data. The least significant bit of the device identification code is set with the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the LGDP4551 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, an index register write operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). The LGDP4551 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The LGDP4551 writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the LGDP4551 starts transferring or receiving data in units of bytes. The LGDP4551 executes data transfer from the MSB. The LGDP4551's instruction takes 16-bit format and they are executed inside after it is transferred in two bytes (16 bits: DB15-0) from the MSB (The LGDP4551 expands RAM write data into 18-bit format when writing them to the internal GRAM). The first byte received by the LGDP4551 following the start byte is always the upper eight bits of instruction and the second byte is the lower 8 bits of instruction.

In case of reading data from the GRAM, the LGDP4551 does not transfer valid data until first five bytes of data are read from the GRAM following the start byte. The LGDP4551 starts sending valid data as it reads the sixth and subsequent byte data.

Table 76 Start byte format

Transferred bits	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

Note: ID bit is selected by setting the IM0/ID pin.

Table 77

RS	**R/W**	**Function**
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

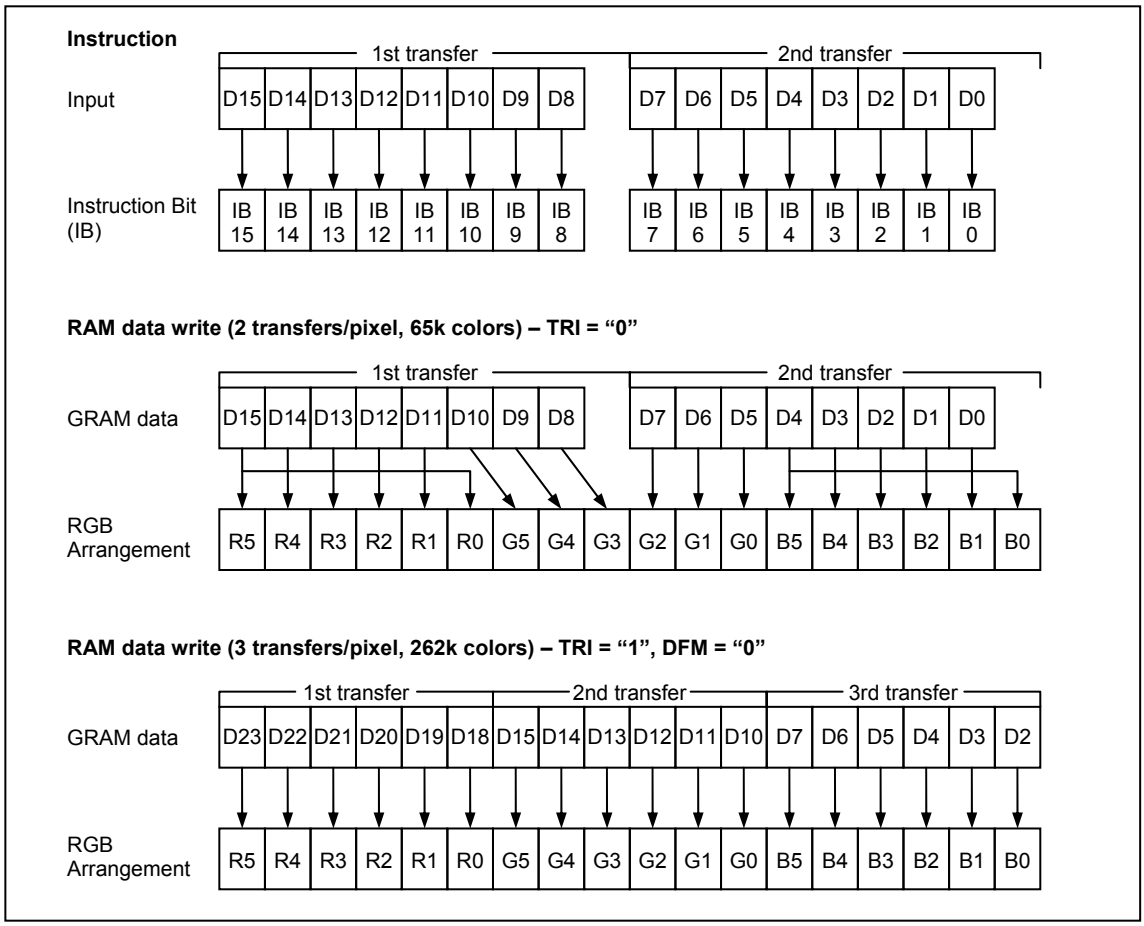


Figure 29 Data format for SPI

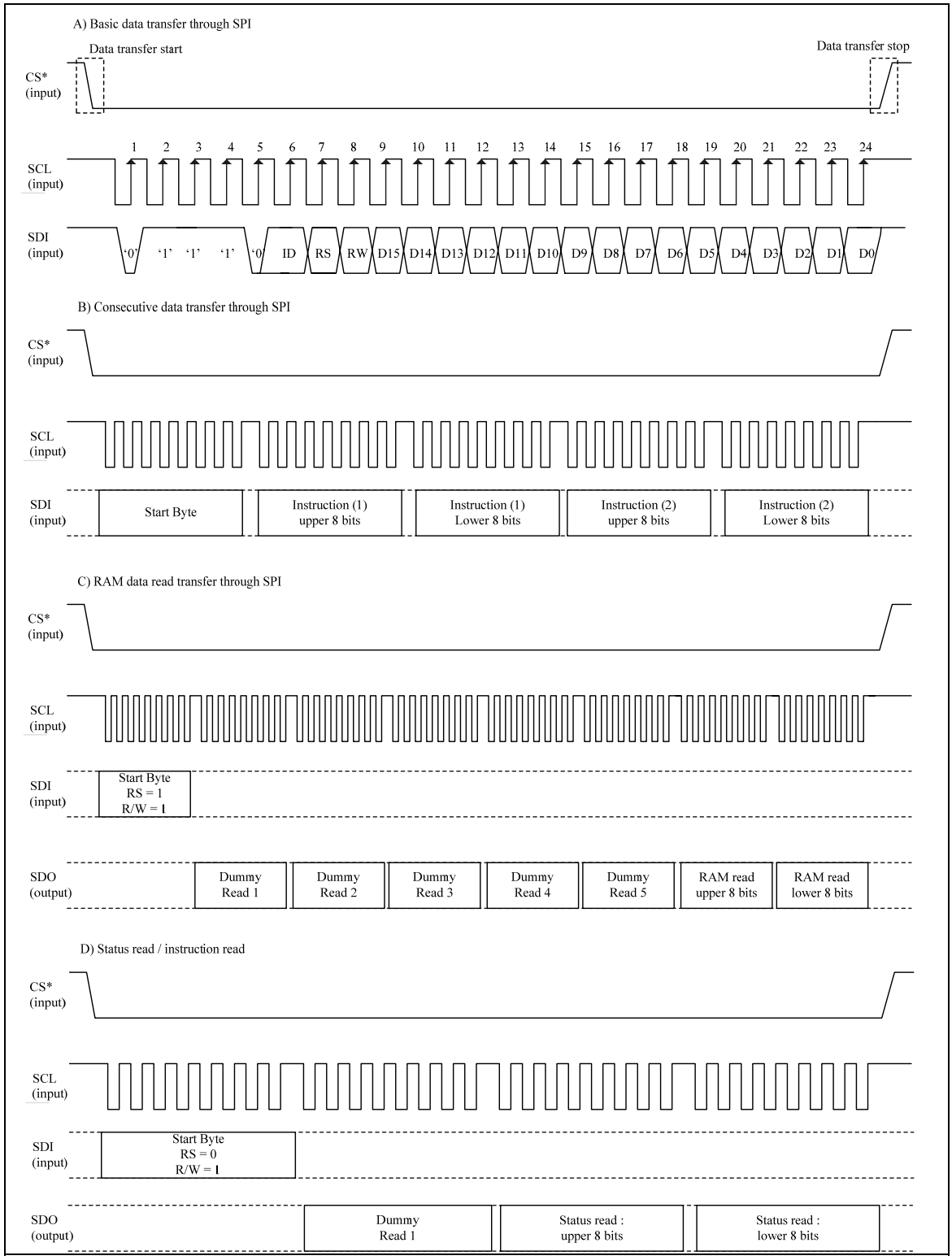


Figure 30 Data Transfer in Serial interface

VSYNC Interface

The LGDP4551 supports VSYNC interface, enabling the LGDP4551 to display a moving picture with minimum modifications to the existing system, using system interface and the frame synchronization signal (VSYNC).

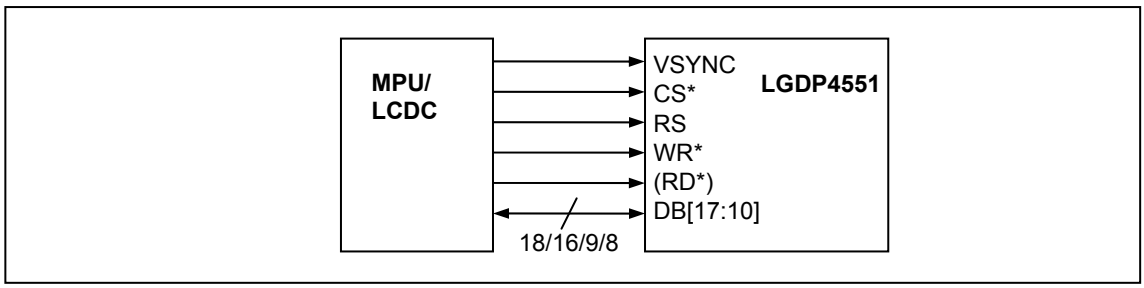


Figure 31 VSYNC Interface

The VSYNC interface is selected by setting DM[1:0] = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at a speed faster to a certain degree than the internal display operation speed, it becomes possible to rewrite data without flickering the moving picture on display and enables the LGDP4551 to display a moving picture using a system interface.

The LGDP4551 performs the display operation with the internal clock signal generated from the internal oscillator and the VSYNC signal in this mode. In VSYNC mode, the data displayed on the screen are written to the internal RAM in order to transfer only the data to be written over the moving picture RAM area and thereby minimize the total data transfer required for moving picture display.

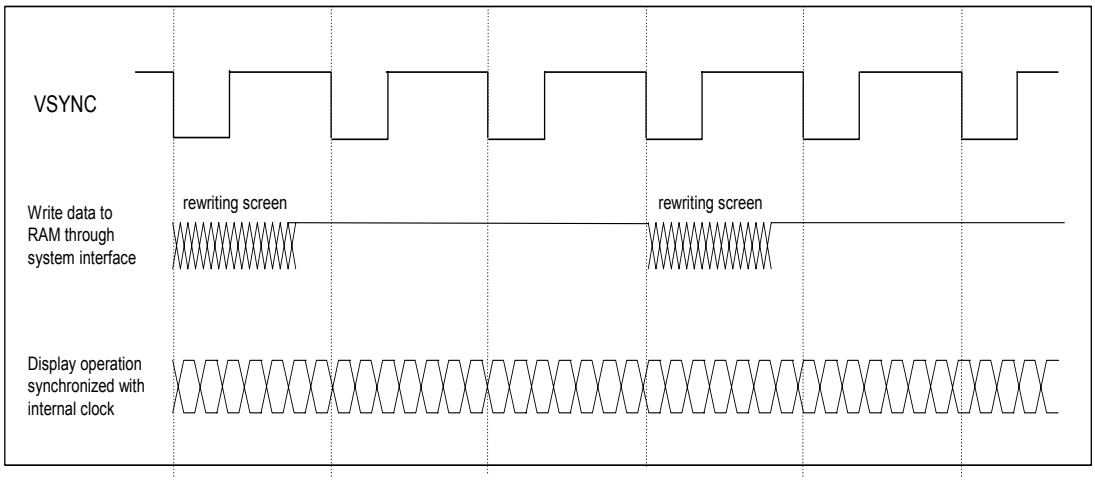


Figure 32 Moving Picture Data Transfers via VSYNC Interfce

The VSYNC interface has the minimum speed of writing data to the internal RAM via the system interface and the minimum internal clock frequency, which are calculated from the following formulae.

Internal clock frequency (fosc) [Hz]
= FrameFrequency × (DisplayLines (NL) + FrontPorch (FP) + BackPorch (BP)) × 60 clocks × variance

$$RAMWriteSpeed > \frac{240 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 60\ clocks \times \frac{1}{fosc}}$$

Note: When the RAM write operation does not start on the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum RAM writing speed and internal clock frequency in VSYNC interface mode is as follows.

[Example]

Display size	240 RGB × 432 lines
Lines	432 lines
Back/front porch	14/2 lines (BP = 1110/FP = 0010)
Frame frequency	70 Hz

Internal clock frequency (fosc)
= 70 Hz × (432 + 2 + 14) lines × 60 Clocks × 1.1 / 0.9 = 2.3 MHz

When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±10% for variances and ensures to complete the display operation within one VSYNC cycle.

In this example, variances attributed to the fabrication process of LSI and room temperature are counted in. Other possible causes of variances, such as differences in external resistors or voltage changes are not in consideration. It is necessary to allow for an enough margin if these factors must be incorporated.

Minimum speed for RAM writing
240 × 432 / {((14 + 432 - 2) lines × 60 clock) / 2.3 MHz} = 8.96 MHz

The above theoretical value is calculated on the premise that the LGDP4551 starts writing data to the internal RAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line where display operation is performed and the RAM line address where data write operation is performed.

The RAM write speed of 5.7MHz or more on the falling edge of VSYNC will guarantee the completion of RAM write operation before the LGDP4551 starts displaying the RAM data on the screen, enabling rewriting the entire screen without flicker.

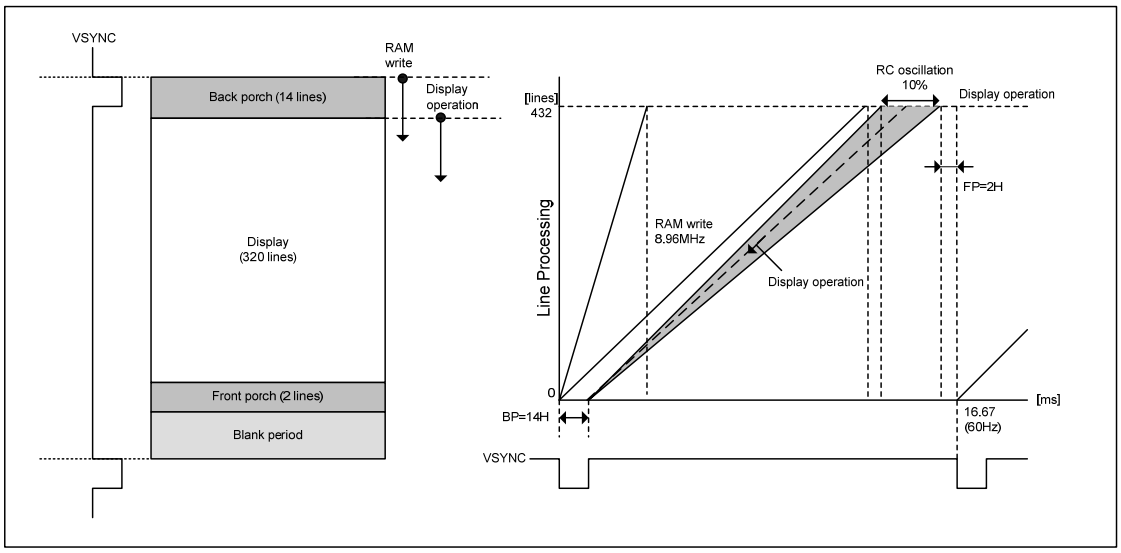


Figure 33 Write/Display Operation Timing via VSYNC Interface

Notes in using the VSYNC interface

1. The above example of calculation gives a theoretical value. In the actual setting, other possible causes of variances not counted in the above example such as differences in internal oscillators should also be taken into consideration. It is strongly recommended to allow for an enough margin in setting a RAM writing speed.

2. The above example of calculation gives a minimum value in case of rewriting the entire screen. If the moving picture display area is smaller than that, the range for setting a minimum RAM writing speed can have extra margins.

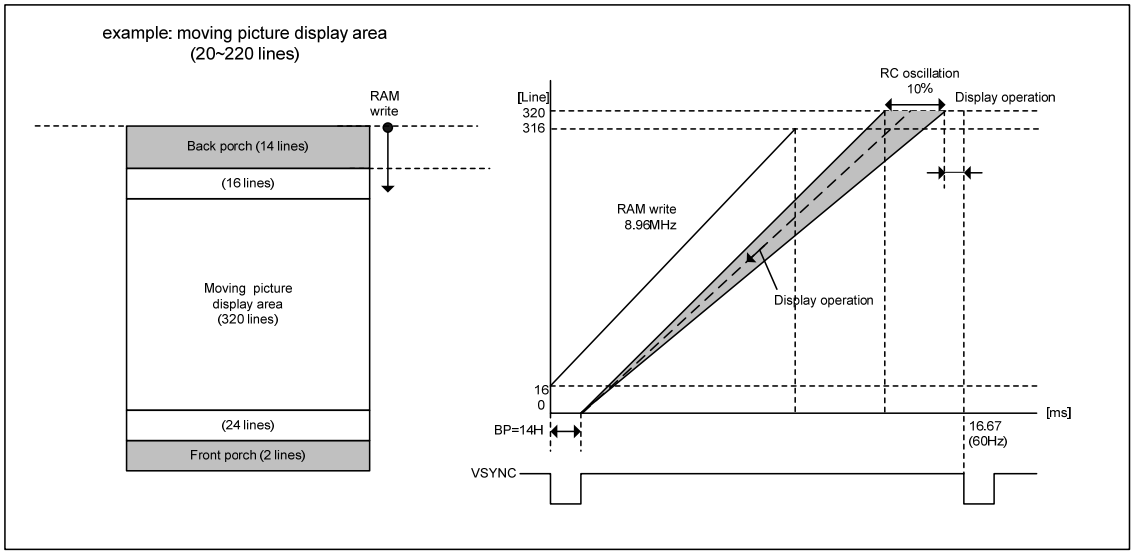


Figure 34 RAM write margin

3. After drawing 1 frame, a front porch period continues until the next input of VSYNC is detected.

4. When switching from the internal clock operation mode (DM1-0 = “00”) to the VSYNC interface mode, or the other way around, it is enabled from the next VSYNC cycle, i.e. after completing the display of the frame, which the LGDP4551 was internally processing when switching the modes.

5. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

6. In VSYNC interface mode, set the AM bit to “0” to transfer display data in the method mentioned above.

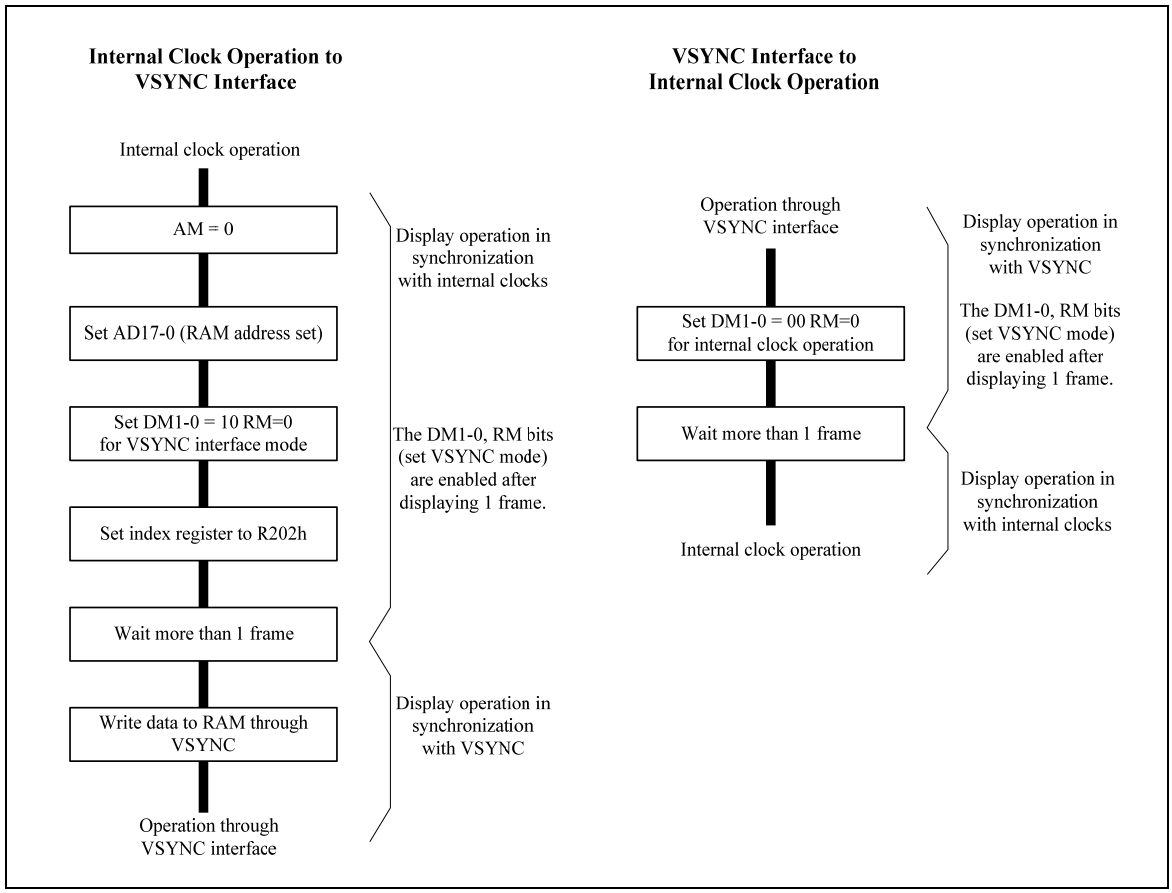


Figure 35 Sequences to Switch between VSYNC and Internal Clock Operation Modes

External Display Interface

The following RGB interfaces are available with the LGDP4551. The interface operation is set with the RIM[1:0] bits. The RGB interface is used for RAM access.

Table 78

RIM[1:0]	RGB Interface	DB Pin
00	18-bit RGB interface	DB[17:0]
01	16-bit RGB interface	DB[17:10], DB[8:1]
10	6-bit RGB interface	DB[17:12]
11	Setting disabled	-

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface in combination with the window address function enables minimizing data transfer by rewriting data in high-speed with low power consumption only within the RAM area where data must be updated. In RGB interface operation, it is necessary to set back and front porch periods before and after the display period, respectively.

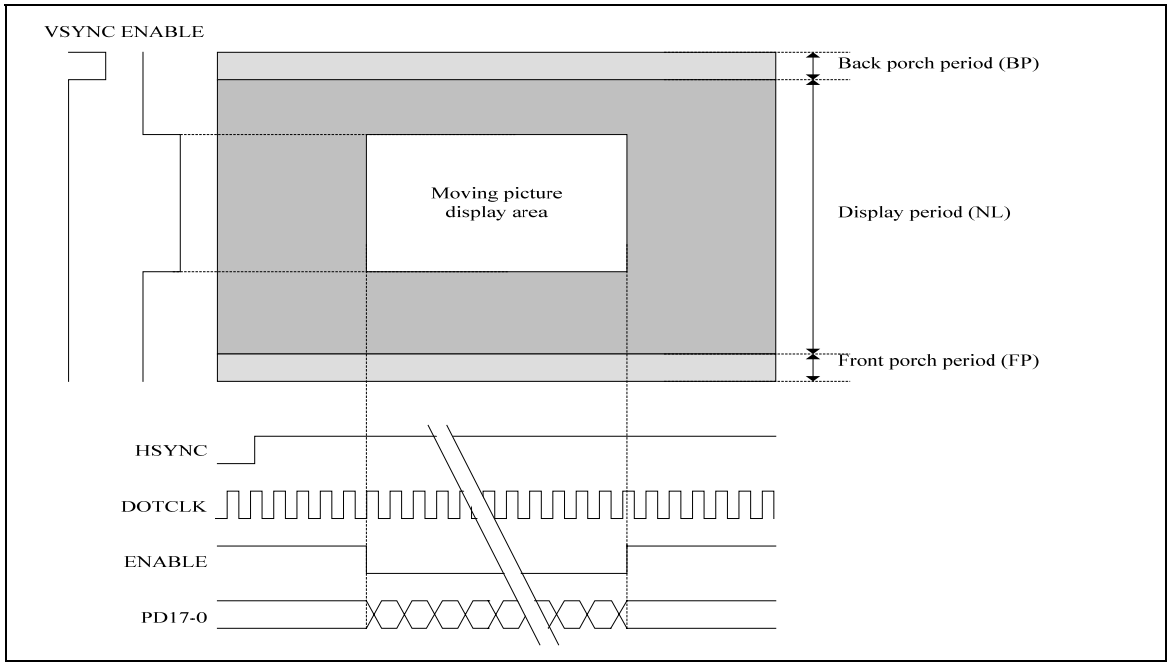


Figure 36 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals are changeable by setting the DPL, EPL, HSPL, and VSPL bits, respectively according to the system configuration.

RGB Interface Timing

The timing relationships of signals in RGB interface operation area as follows.

16-18-bit RGB Interface Timing

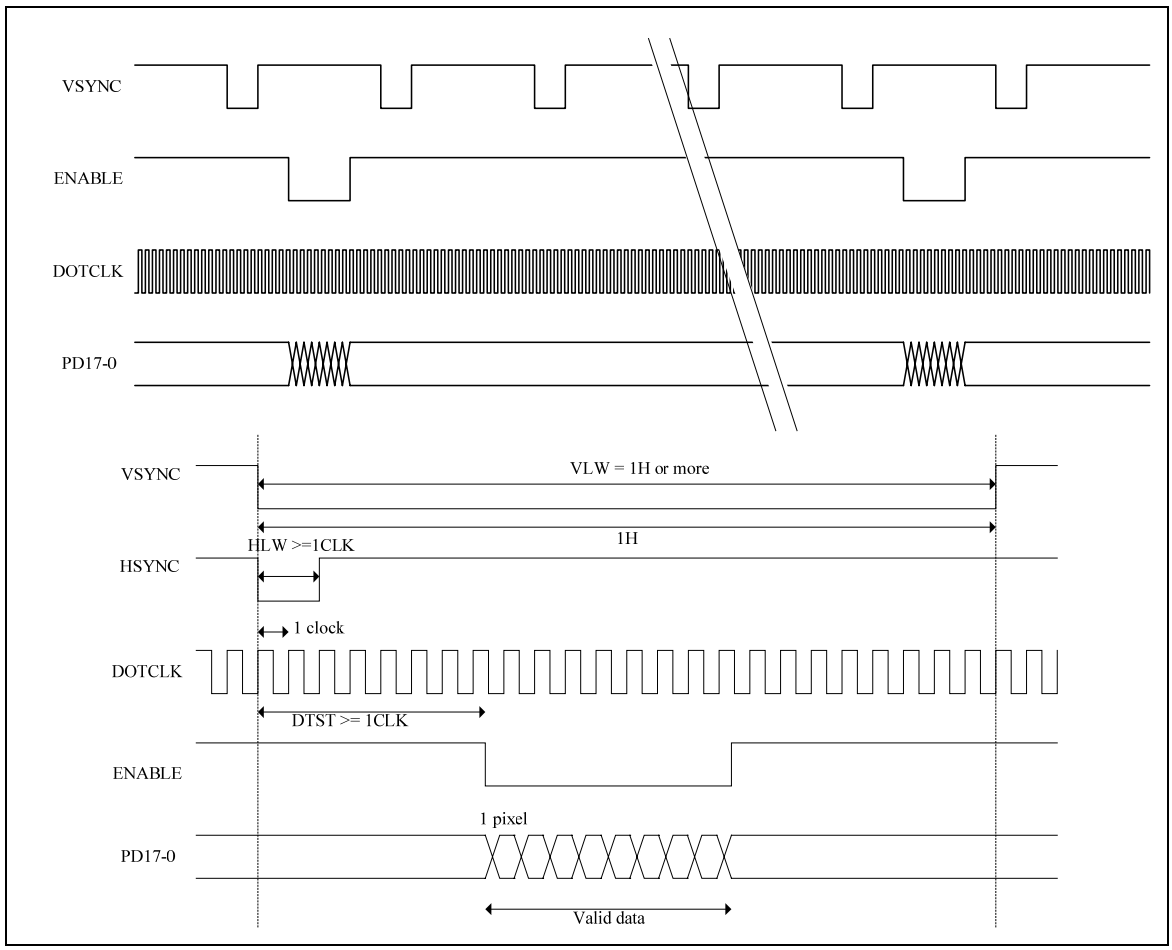


Figure 37

Notes: 1. VLW : VSYNC Low period
HLW : HSYNC Low period
DTST : data transfer setup time

6-bit RGB Interface Timing

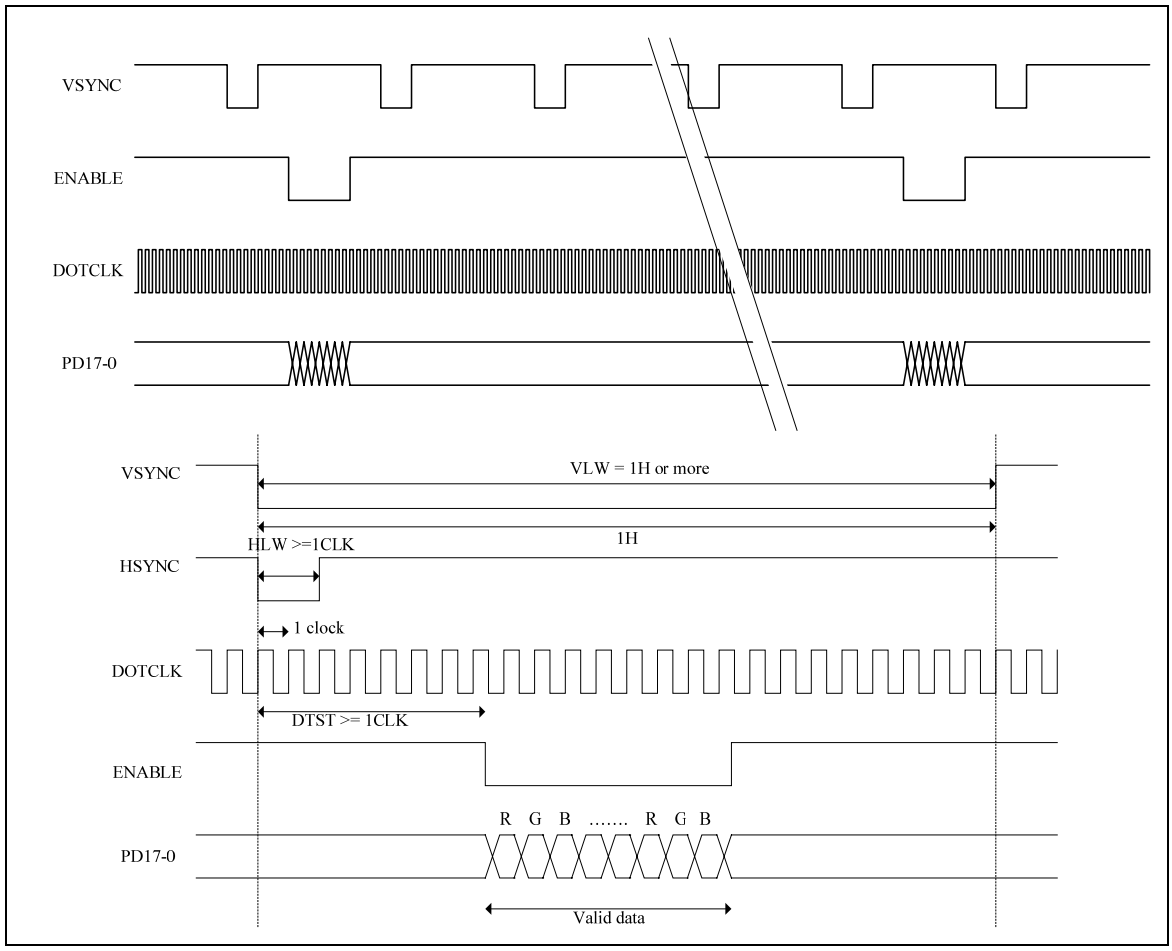


Figure 38

Notes: 1. VLW : VSYNC Low period
HLW : HSYNC Low period
DTST : Data transfer setup time
2. In 6-bit RGB interface operation, set the cycles of VSYNC, HSYNC, ENABLE, DOTCLK so that one pixel is transferred in units of three DOTCLKs via DB17-12 (DB5-0).

Moving Picture Display with the RGB Interface

The LGDP4551 supports RGB interfaces for displaying a moving picture and RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function can minimize data transfer by specifying a moving picture RAM area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. The data transfer is limited to a moving picture RAM area.
4. The reduction in data transfer contributes to the reduction in power consumption by the entire system
5. The combined use with system interface allows updating data in the still picture area, such as icons, while displaying a moving picture via RGB interface

RAM access via system interface in RGB interface operation

The LGDP4551 allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is “Low”. When writing data to the RAM via system interface, set ENABLE “High” to stop writing data via RGB interface. Then set RM = “0” to enable RAM access via system interface. When reverting to the RGB interface operation, wait for a time for a read/write bus cycle. Then, set RM = “1” and the index register to R22h to start accessing RAM via RGB interface. A conflict between RAM accesses via two different interfaces will not guarantee write operation.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

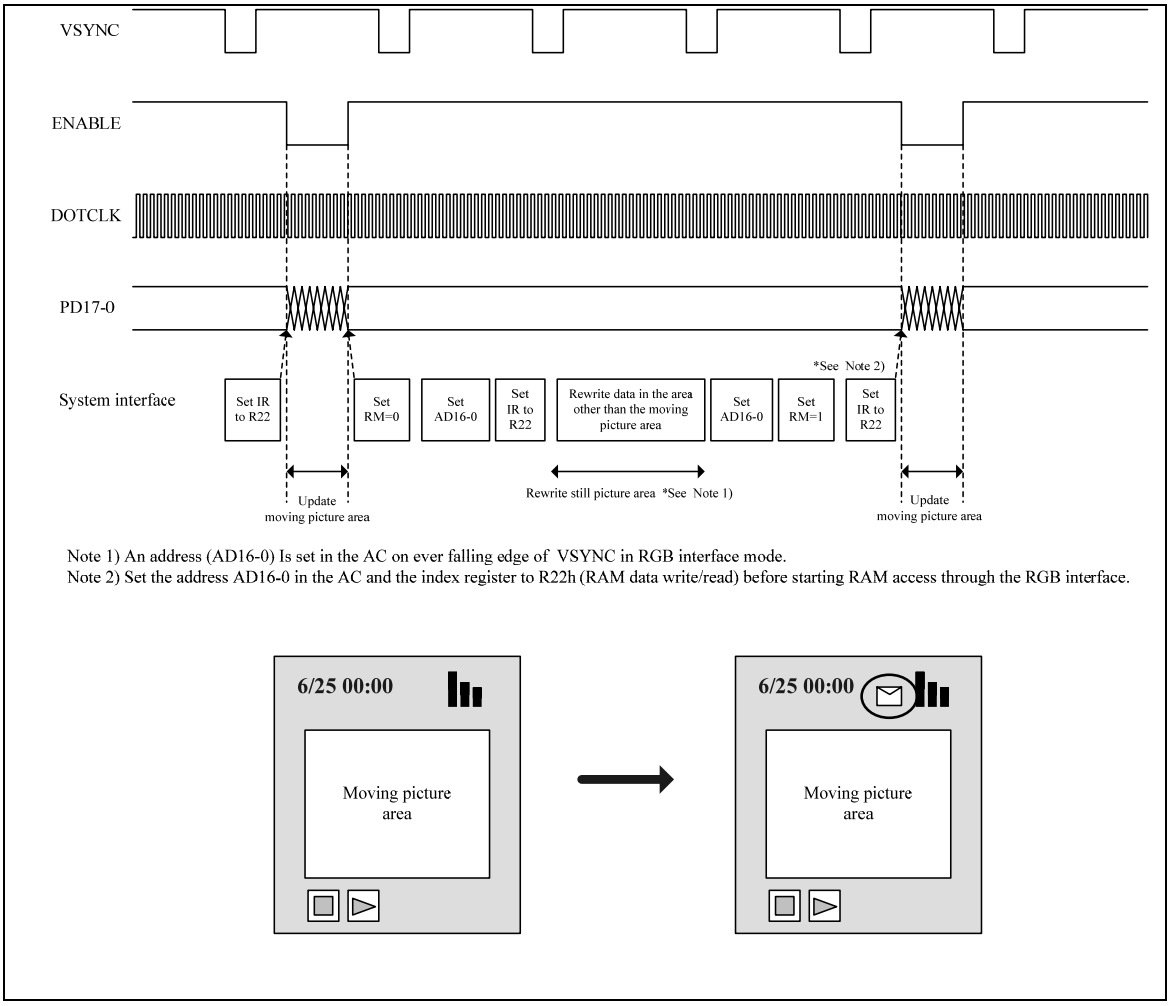


Figure 39 Updating the Still Picture Area while Displaying Moving Picture

6-bit RGB Interface

The 6-bit RGB interface is selected by setting RIM[1:0] = 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus according to data enable signal (ENABLE). Unused pins DB[11:0] must be fixed at either IOVcc or IOGND level.

The instructions are set only via system interface.

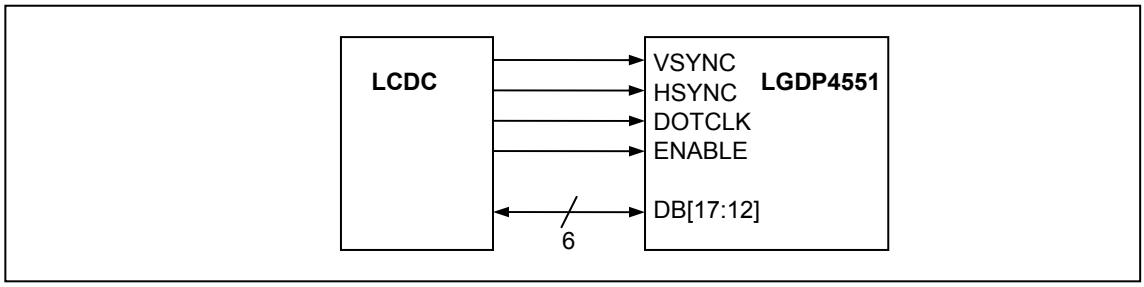


Figure 40 6-bit RGB interface

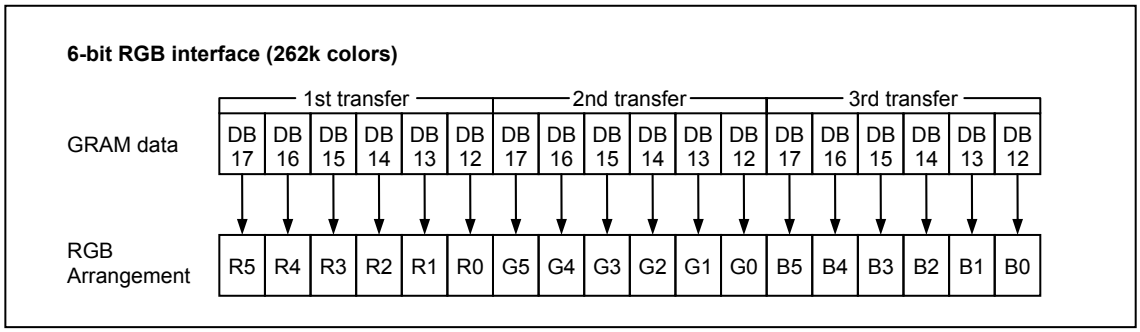


Figure 41 Data format for 6-bit interface

Data Transfer Synchronization in 6-bit Bus Interface operation

The LGDP4551 has data transfer counters to count the first, second, and third 6-bit data transfers in 6-bit RBG interface operation. The transfer counters are always reset to the first data transfer on the falling edge of VSYNC. If there is a mismatch in the number of data transfers, the counters are reset to the first data transfer at the start of each frame (on the falling edge of VSYNC) and data transfer can be restarted in correct order from the next frame. In case of displaying a moving picture, which requires consecutive data transfer, this function can minimize the effect from the data transfer mismatch and help recover the display system to a normal state.

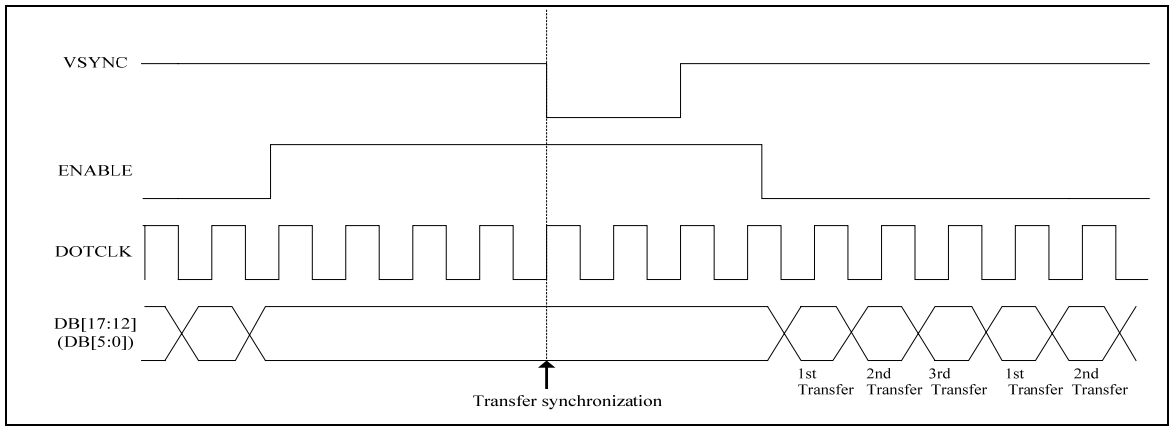


Figure 42 6-bit Transfer Synchronization

16-bit RGB Interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus according to data enable signal (ENABLE).

The instructions are set only via system interface.

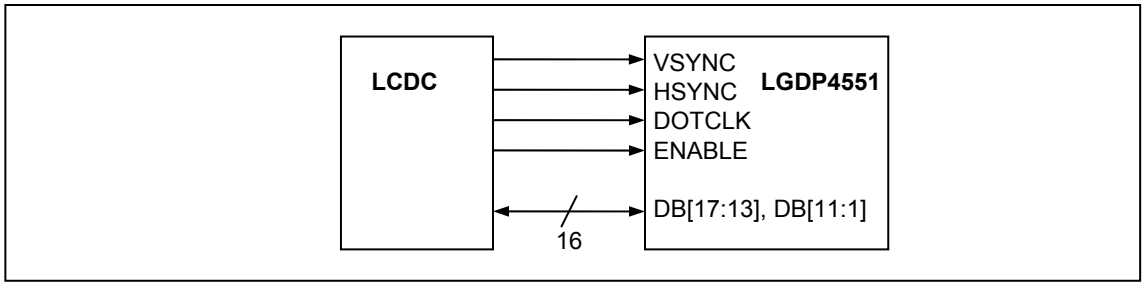


Figure 43 16-bit RGB interface

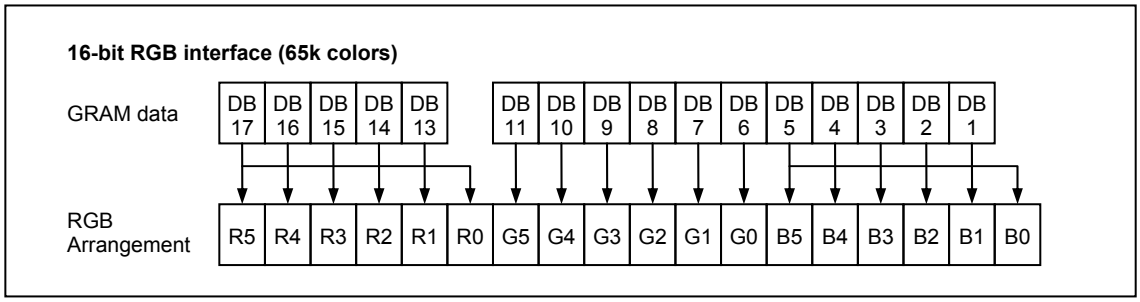


Figure 44 Data format for 16-bit interface

18-bit RGB Interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB17-0) according to data enable signal (ENABLE).

The instructions are set only via system interface.

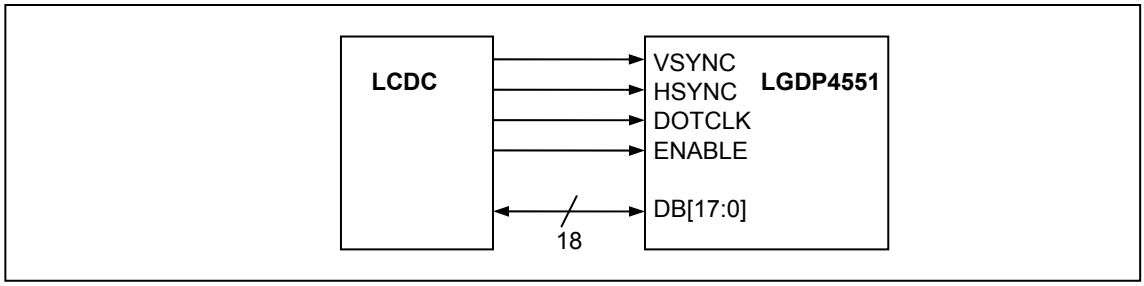


Figure 45 18-bit RGB interface

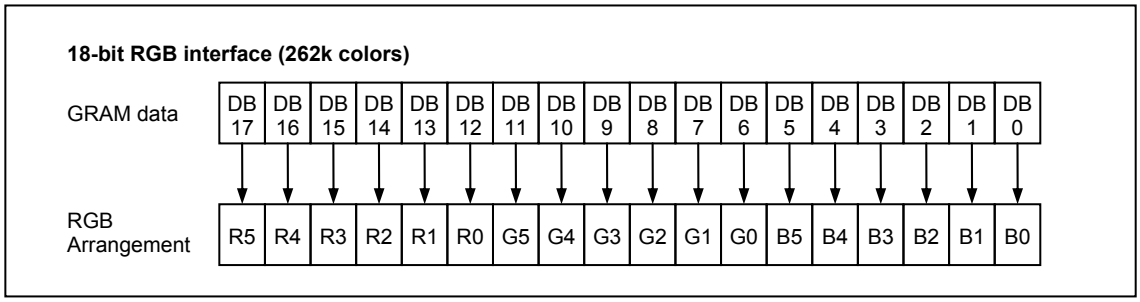


Figure 46 Data format for 18-bit interface

Notes on Using the External Display Interface

1. The following functions are not available in external display interface operation.

Table 79 Functions Not Available in External Display Interface operation

Fucntion	External Display Interface	Internal Display Interface
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied throughout the display operation.

3. The reference clock for generating liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.

4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel.

5. In 6-bit RGB interface operation, each 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. Take this into consideration and make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE, and data transfer via DB17-12 so that data transfer is completed in units of pixels.

6. When switching between the internal operation mode and the external display interface operation, follow the sequences in Figure 43 RGB and Internal Clock Operation Mode switching sequences.

7. In RGB interface operation, a front porch period continues until the next VSYNC input is detected after the end of each frame period.

8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to the internal RAM.

9. In RGB interface operation, RAM address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

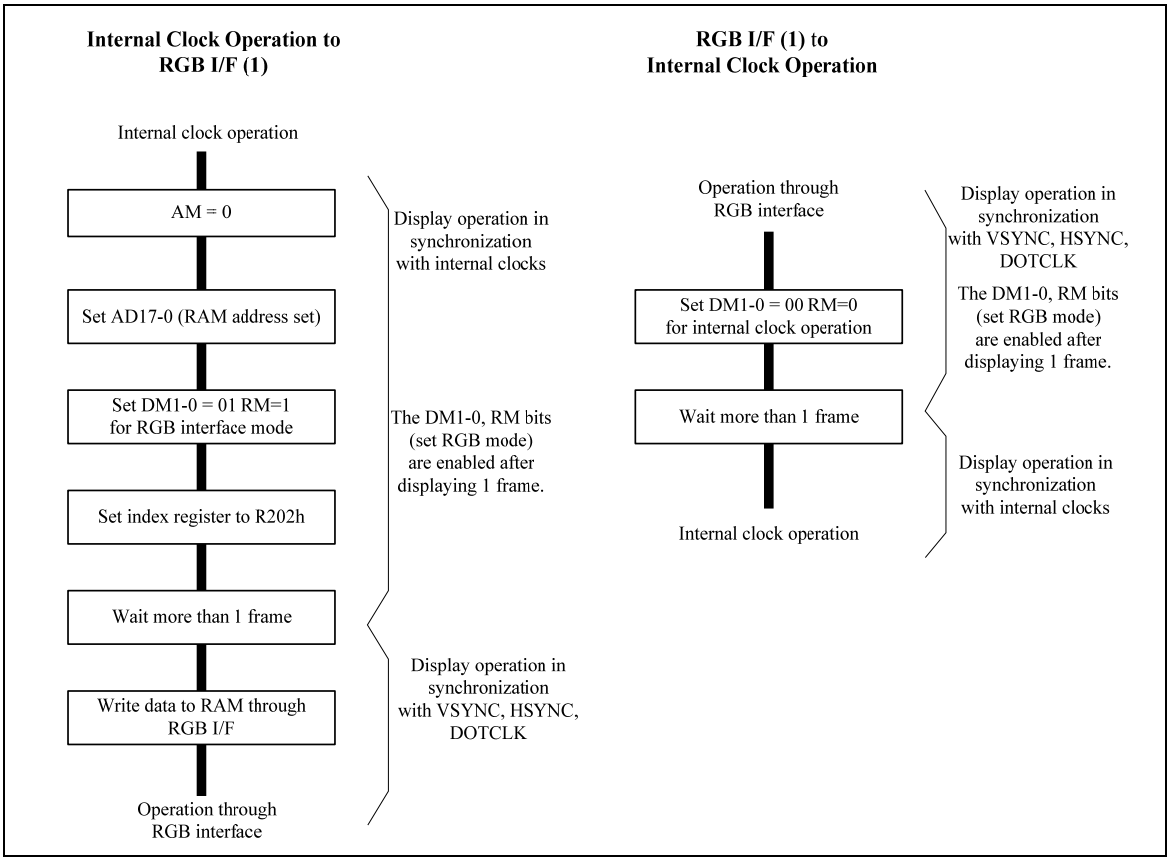


Figure 47 RGB and Internal Clock Operation Mode switching sequences

RAM Address and Display Position on the Panel

The LGDP4551 has memory to store display data of 240RGB x 432 lines. The LGDP4551 incorporates a circuit to control partial display, which enables switching driving methods for full-screen display and partial display.

The LGDP4551 allows separate settings for display control and driving position control and specifying a RAM area for each image displayed on the screen. This structure enables designing a display on the screen not constrained by the mounting position of the display panel.

The following is the sequence of settings for full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image with PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, the register setting in SS bit is required when writing RAM data.

Table 80

	Display ENABLE	Numbers of Lines	RAM area
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h1AF)

Notes : 1: The base image is displayed from the first line of the screen.
2: Make sure NL ≤ 432 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h1AF, respectively.

Table 81

	Display ENABLE	Display position	RAM start position
Partial image 1	PTDE0	(PTDP0, PTEA0)	PTSA0
Partial image 2	PTDE1	(PTDP1, PTEA1)	PTSA1

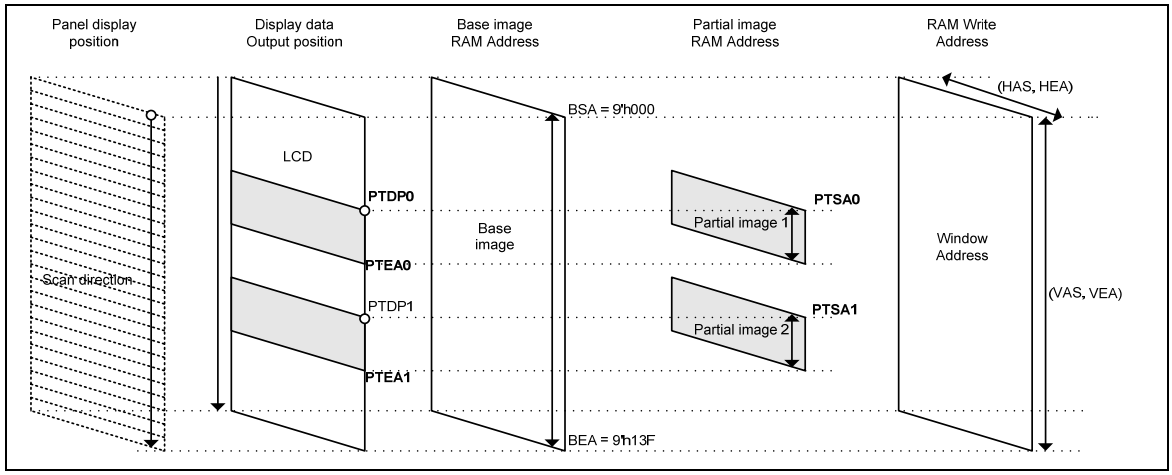


Figure 48 RAM Address, display position and drive position

Restrictions in setting display control instruction

The following are the constraints in setting coordinates of display data, display position, and partial image display.

Screen setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is within the limit: NL ≤ 432 lines

Base image display

1. The base image is displayed from the first line of the screen: BSA = 1st line (of the display panel)

2. The base image RAM area specified with BSA, BEA must include the same or more number of lines necessary to drive the liquid crystal panel (NL setting): BEA - BSA ≥ NL

Partial image display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partials do not overlap each other.

$0 \leq PTDP0 \leq PTEA0 <$
$PTDP1 \leq PTEA1 \leq NL$

The following figure shows the relationship among the RAM address, display position, and driving positions of the panel.

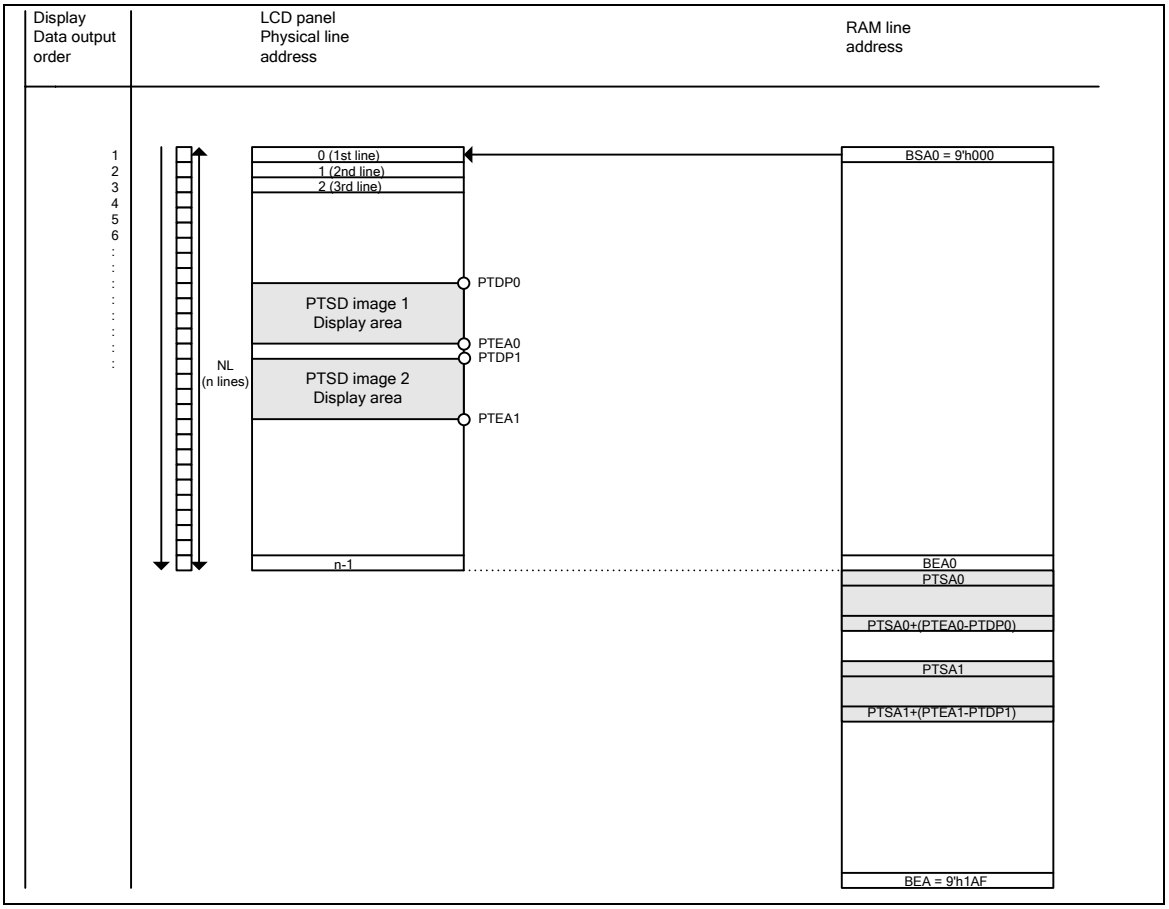


Figure 49 Display RAM Address and display position

Note: In this figure, the RAM address is defined in relation to the display position on the panel. Inside the LGDP4551, the RAM address area where the data is written is defined within a window address area on the GRAM address mapping.

Instruction setting example

The followings are the examples of settings for 240(RGB) x 432(lines) panels.

1. Full screen display (no partial)

The following is an example of setting for full screen display.

Table 82

Base image display insruction	
BASEE	1
NL[5:0]	6'h35
PTDE0	0
PTDE1	0

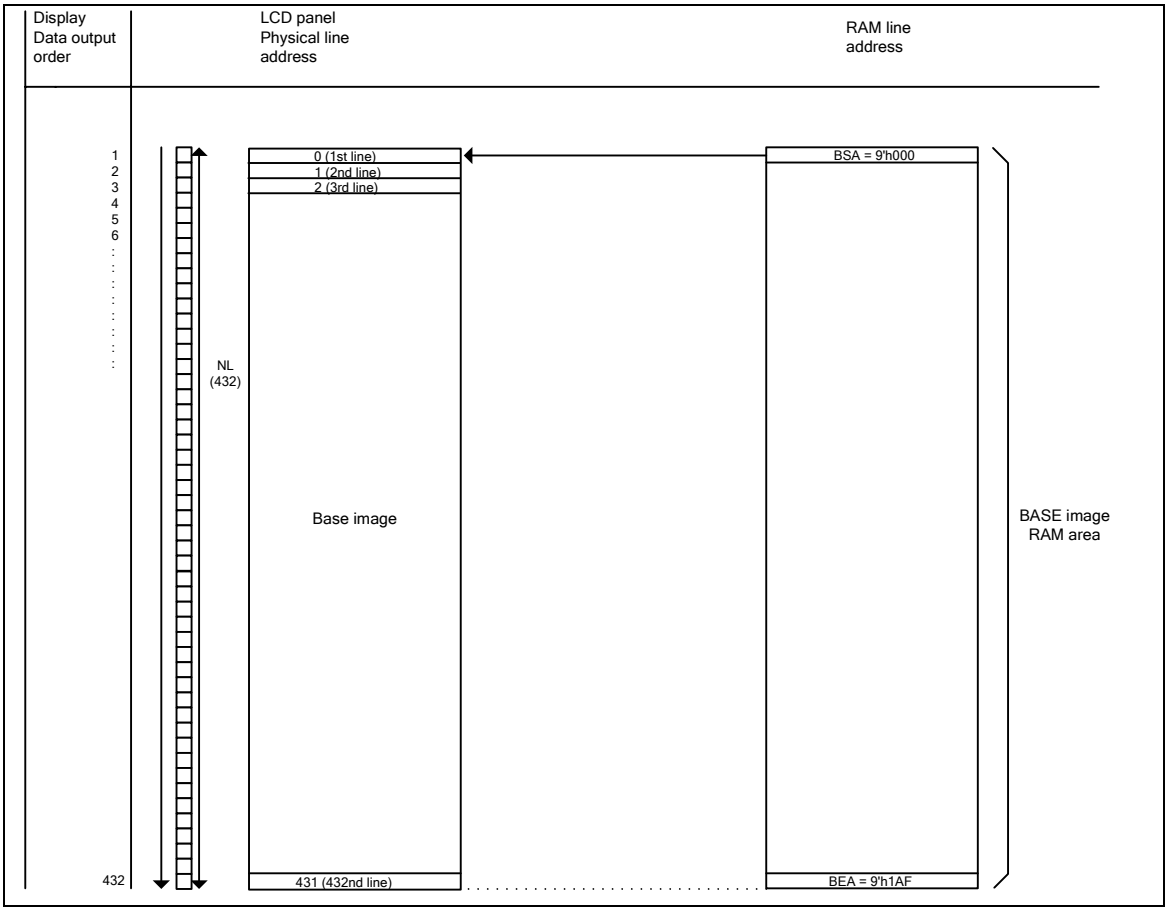


Figure 50 Full screen display (no partial)

2. Partial only

The following is an example of setting for displaying partial image 1 only and turning off the base image display. The partial image 1 is displayed at the position designated by users.

Table 83

Base image display insruction	
BASEE	0
NL[5:0]	6'h35

Partial image 1 display insruction	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h08F
PTDP0[8:0]	9'h080

Partial image 2 display insruction	
PTDE1	0
PTSA1[8:0]	9'h000
PTEA1[8:0]	9'h000
PTDP1[8:0]	9'h000

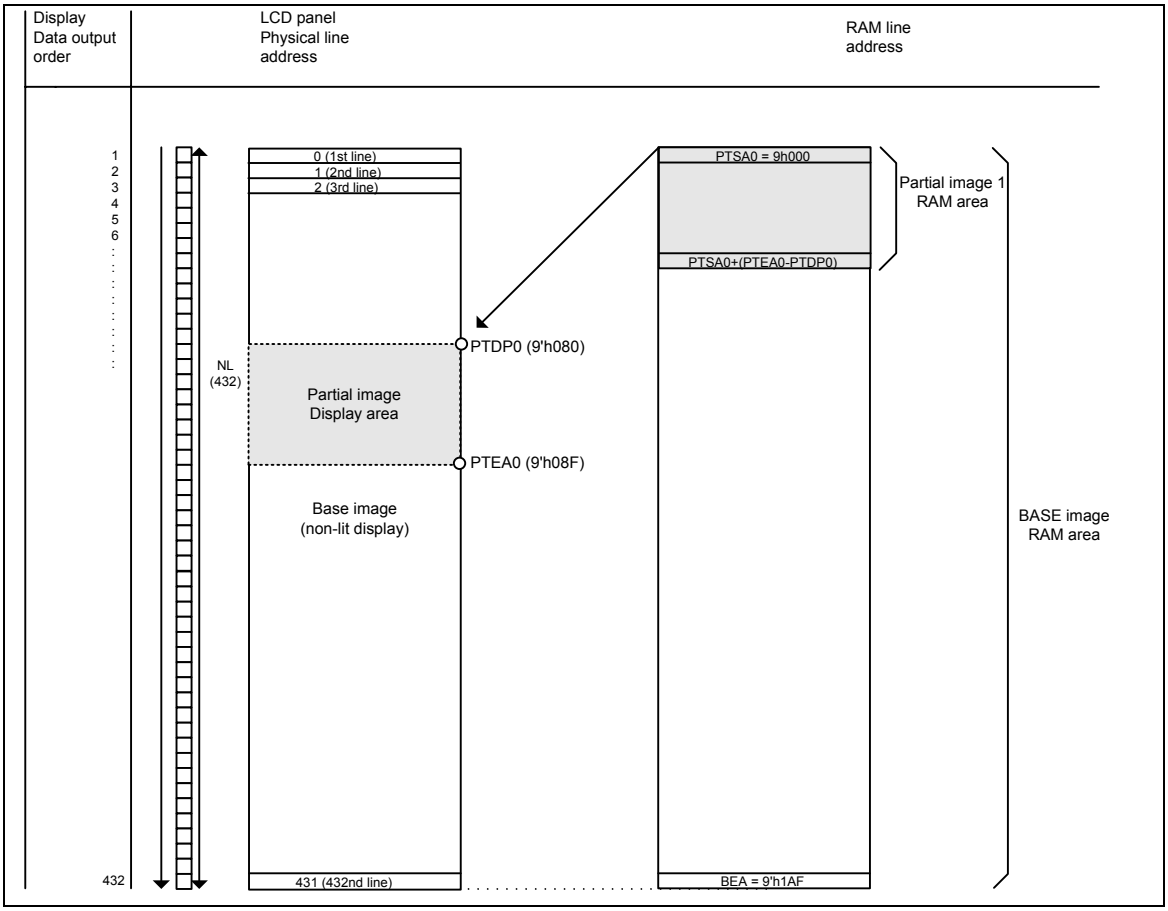


Figure 51 Partial display

Resizing function

The LGDP4551 supports resizing function (x 1/2, x 1/4), which is executed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit representing the contraction factor (x1/2 or x1/4) of the image. This function enables the LGDP4551 to write the resized image data directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system just to transfer data as usual even when resizing of the image is required. This feature makes a resized image easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The LGDP4551 processes the contraction of an image simply by selecting pixels. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.

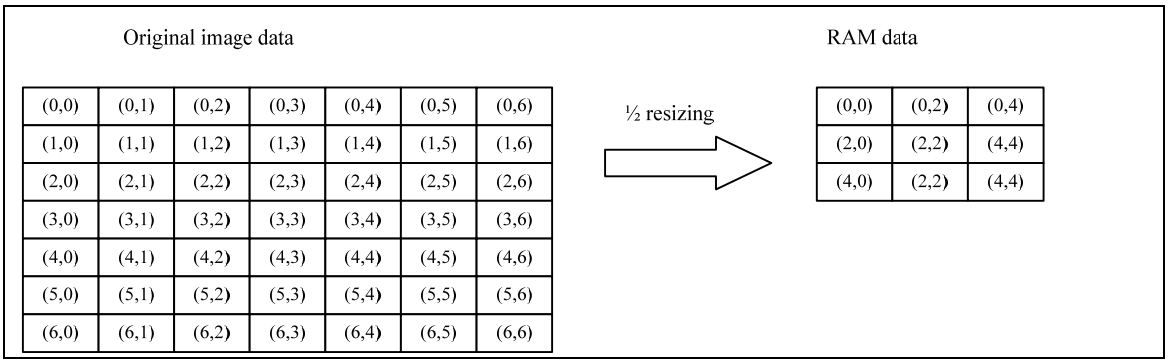


Figure 52 Data transfer in resizing

Table 84

Origianl image size (X x Y)	Resized image Size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
640x480(VGA)	320x240	160x120
352x288(CIF)	176x144	88x72
320x240(QVGA)	160x120	80x60
176x144(QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44

Resizing setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting the RAM area using the window address function, the window address area must be just the size of the resized picture. If resizing creates surplus pixels, which are calculated from the following equations, set them with the RCV, RCH bits before writing data to the internal RAM.

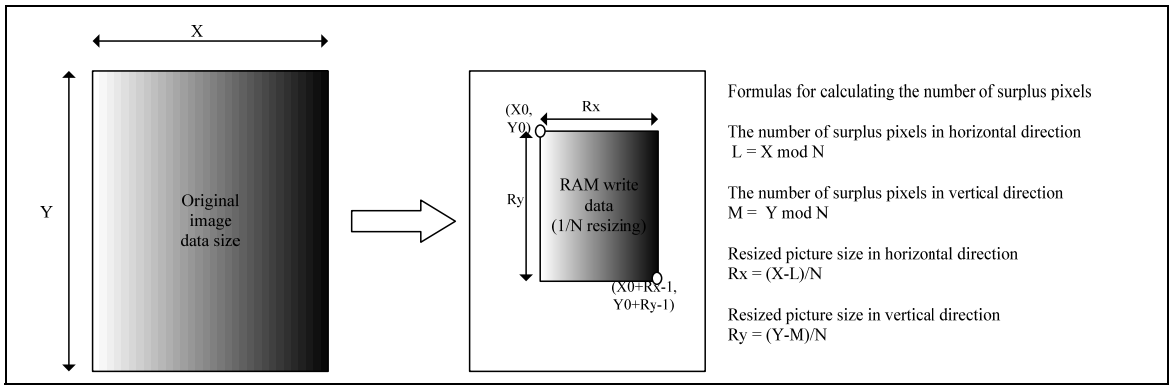


Figure 53 Resizing Setting, surplus pixel calculation

Table 85

Image (before resizing)		
Number of data in horizontal direction	X	
Numbef of data in vertical direction	Y	
Resizing ratio	1/N	

Resizing setting in the LGDP4551		
Resizing setting	RSZ	N-1
Numbef of data in horizontal direction	RCH	L
Numbef of data in vertical direction	RCV	M
RAM writing start address	AD	(X0,Y0)
RAM window address	HAS	X0
	HEA	X0+Rx-1
	VSA	Y0
	VEA	Y0+Ry-1

Notes to Resizing function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are remainder pixels. Otherwise (if RSZ = 2'h0), set RCH = RCV = 2'h0.

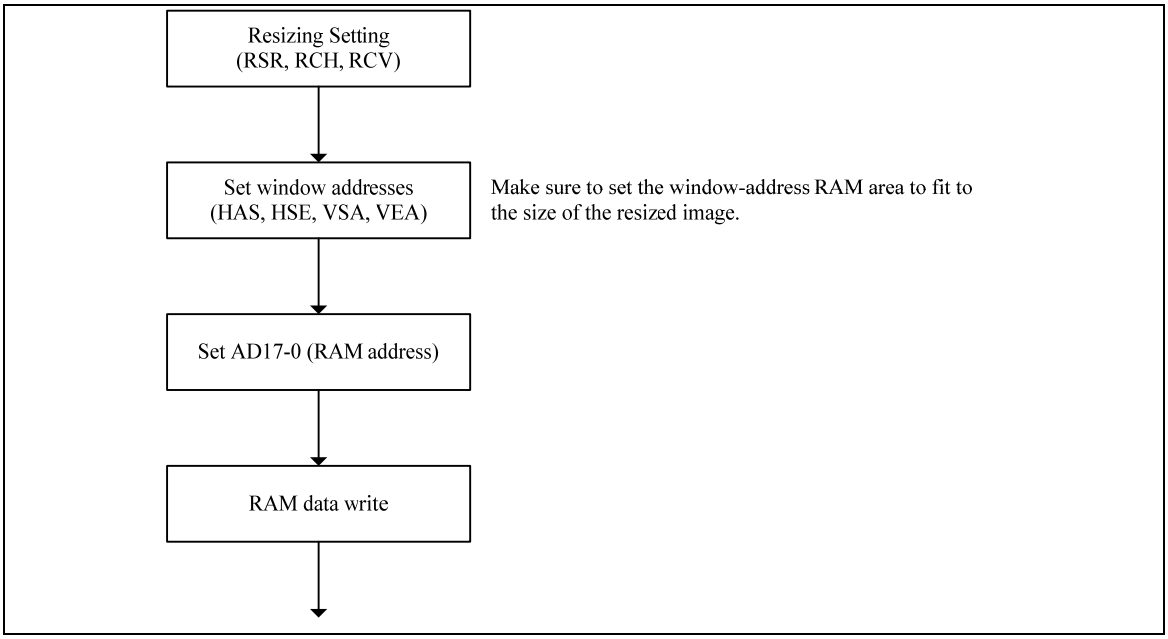


Figure 54 RAM write operation sequence in resizing

FMARK function

The LGDP4551 outputs an FMARK pulse in the timing when driving the line specified with FMP[9:0] bits. The FMARK signal can be used as a trigger signal in writing display data in synchronization with display operation by detecting the address where the RAM data is read out for display operation.

The output interval of FMARK pulse can be set with the FMI[2:0] bits. Set the FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. Sets FMARKOE = 1 when outputting FMARK pulse from the FMARK pin.

Table 86

FMP[9:0]	FMARK output position
10'h000	0
10'h001	1
10'h002	2
:	:
10'h2AD	685
10'h2AE	686
10'h2AF	687
10'h2B0 ~ 3FF	Setting disabled

Table 87

FMI[2:0]	FMARK output interval
3'h0	One frame period
3'h1	2 frame periods
3'h3	4 frame periods
3'h5	6 frame periods
Other setting	Setting disabled

FMP setting example

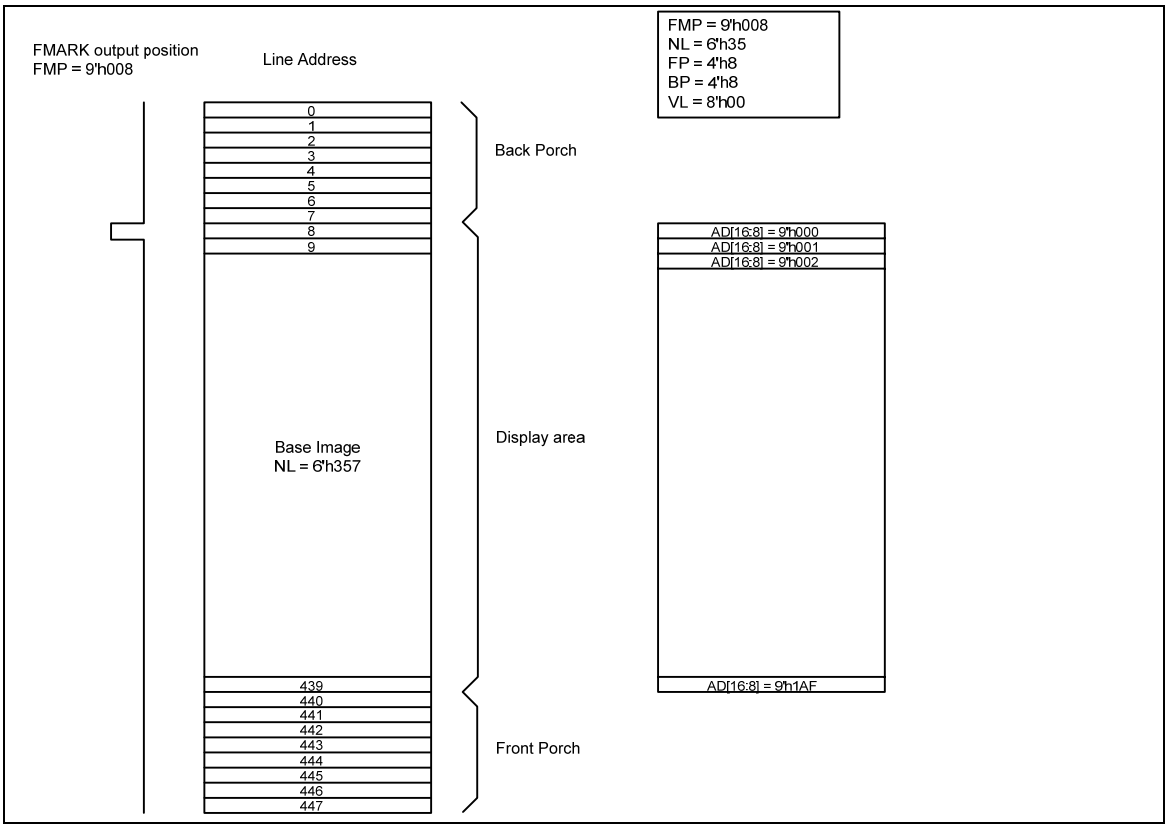


Figure 55

Display operation synchronous data transfer using FMARK

The LGDP4551 uses FMARK signal as a trigger signal to start writing data to the internal GRAM in synchronization with display scan operation.

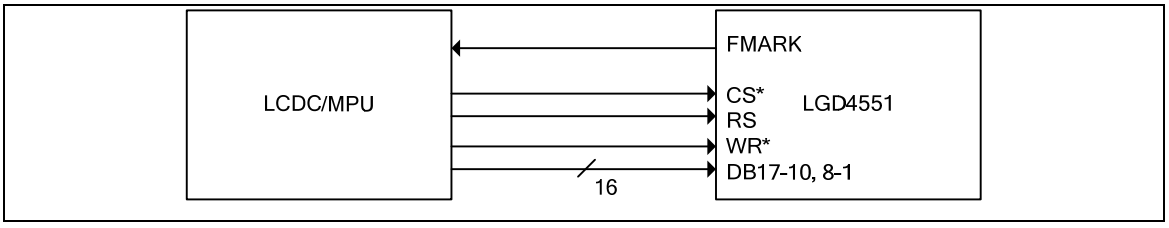


Figure 56 Display synchronous data transfer interface

The LGDP4551 writes display data to the internal GRAM at a speed faster to a certain degree than that of display operation in order to enable a moving picture display via the system interface without flicker. By writing all display data to the internal RAM, only the data tp be overwritten in the moving picture RAM area is transferred and the total data transfer for moving picture display can be minimized.

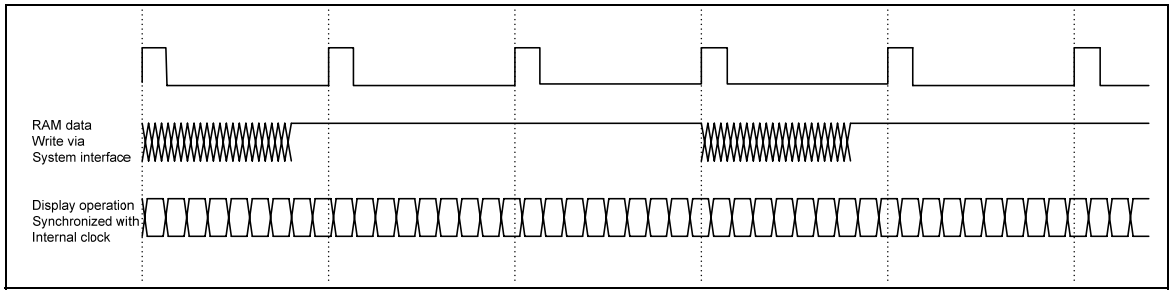


Figure 57 Moving Picture Data Transfers via FMARK function

The data transfer operation via FMARK function has a minimum RAM data rite speed an internal clock frequency, which must be more than the theoretical values chlculated from the following equations

Internal clock frequency (fosc) [Hz]
= FrameFrequency x (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) x 64(clocks) x variance

$$RAMWriteSpeed > \frac{240 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 64\ clocks \times \frac{1}{fosc}}$$

Note : When RAM write operation is not started right after the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of the RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the LGDP4551 to write data including image data consecutively without taking data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area setting range]
(Horizontal direction) 8'h00 ≤ HSA ≤ HEA ≤ 8'hEF
(Vertical direction) 9'h000 ≤ VSA ≤ VEA ≤ 9'h1AF
[RAM Address setting range]
(RAM address) HSA ≤ AD7-0 ≤ HEA
VSA ≤ AD16-8 ≤ VEA

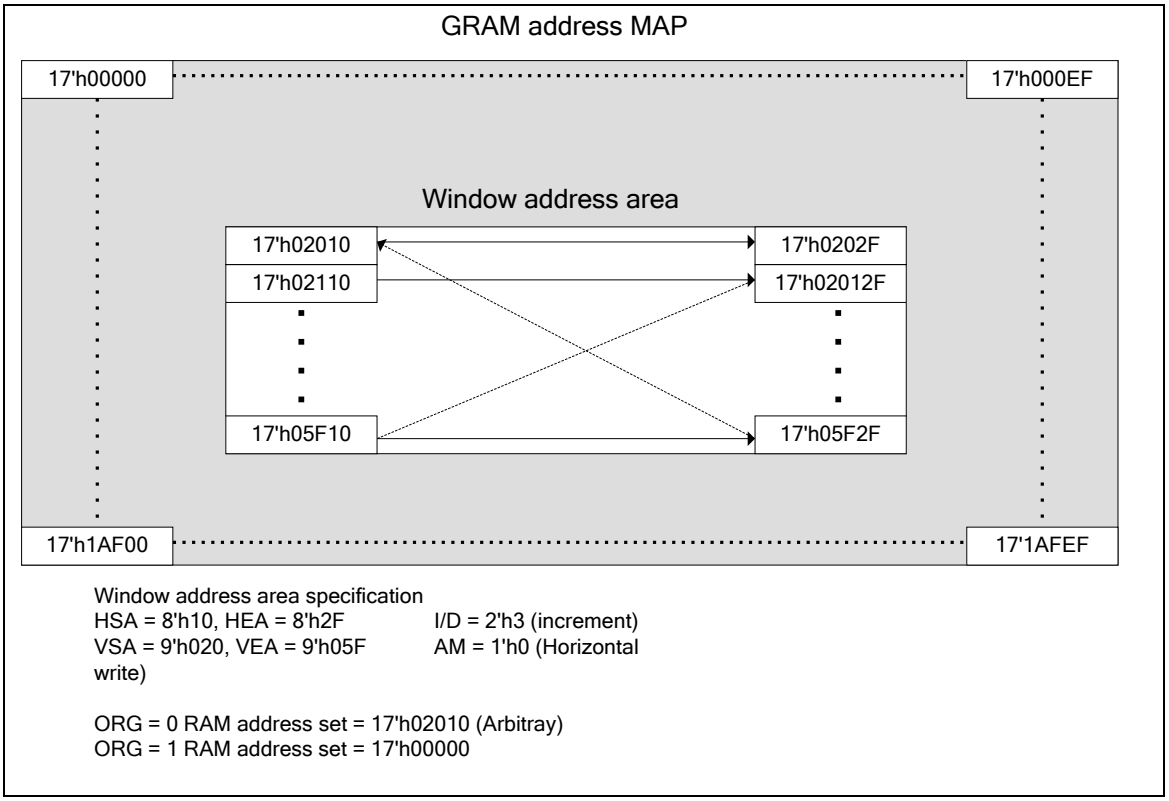


Figure 58 Automatic address update within a Window Address Area

EPROM Control

LGDP4551 has an embedded EPROM which is a 32-bit one-time programmable (OTP) IP from eMemory Technology Inc. (EO01X32KCV6).
EO01X32KCV6 is a CMOS, 1bit (1-bit) program OTP logic device. The main memory block is organized as 8-bits by 4 banks. See the data sheet of EO01X32KCV6.
The pins of the embedded EPROM can be controlled using the EPROM control 1 (R60h) register as shown below.

Table 88

EO01X32KCV6	Bit fields of register R40h
PTM = 0V/1.8V	PTM[1:0] = 00/11
POR = 0V/1.8V	POR = 0/1
VPP = 1.8V/7.2V	VPP = 0/1
PPROG = 0V/1.8V	PPROG = 0/1
PWE = 0V/1.8V	PWE = 0/1
PA[1:0] = 0V/1.8V	PA[1:0] = 0/1
PDIN[7:0] = 0V/1.8V	PDIN[7:0] = 0/1

The RA[1:0] of register R41h selects one of four EPROM bytes.
Accessing EPROM control registers, follow the timing requirements of read and program cycles.

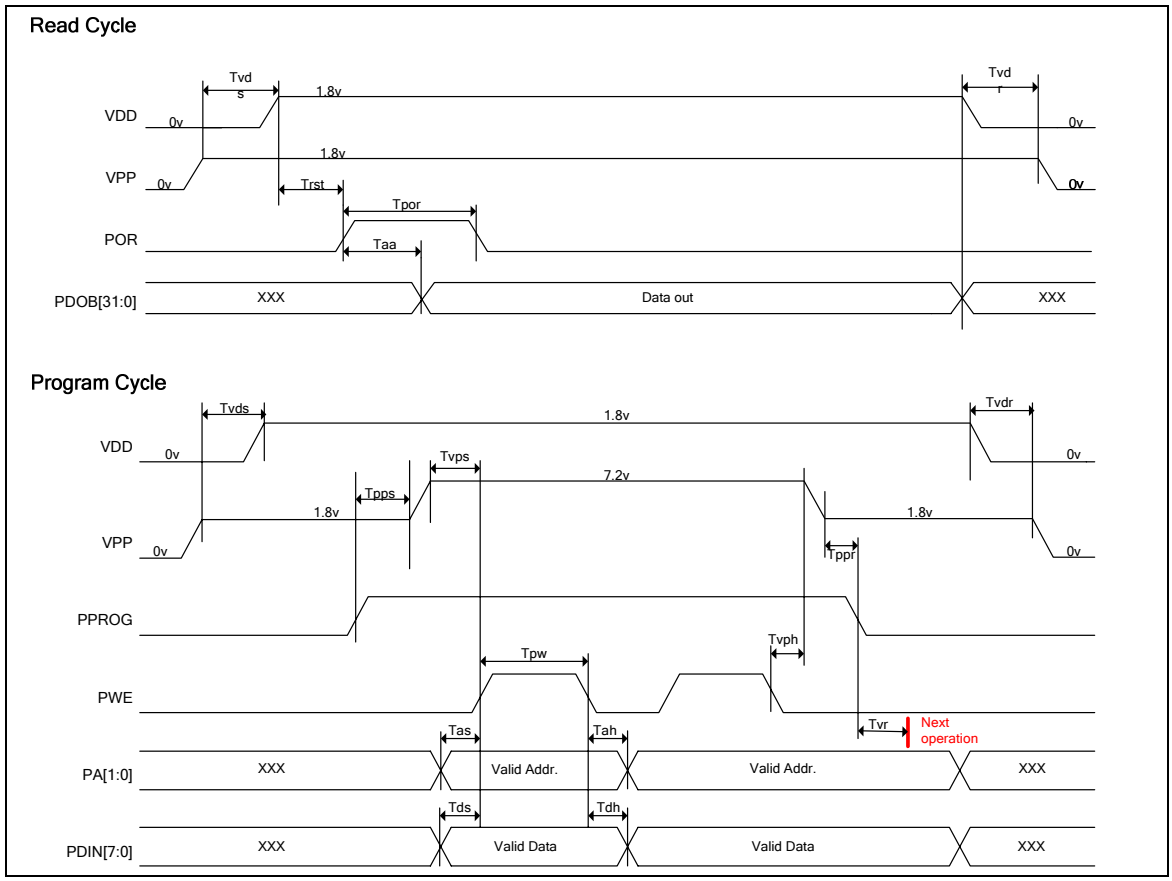


Figure 59 EPROM timings

Table 89

Parameter	Symbol	EO01X32KCV6		Unit
		Min	Max	
Risimg Time / Fallimg Time	T_r / T_f	-	1	ns
Data Access Time	T_{aa}	-	70	ns
Power-on Pulse Width Time	T_{por}	200	-	ns
Address / Data Setup Time	T_{as} / T_{ds}	4	-	ns
Address / Data Hold Time	T_{ah} / T_{dh}	9	-	ns
External VPP Setup Time	T_{vps}	0	-	ns
External VPP Hold Time	T_{vph}	0	-	ns
Program Recovery Time	T_{vr}	10	-	us
Program Pulse Width	T_{pw}	300	350	us
VDD Setup Time	T_{vds}	0	-	ms
VDD Recovery Time	T_{vdr}	0	-	ms
PPROG Setup Time	T_{pps}	10	-	ns
PPROG Recovery Time	T_{ppr}	10	-	ns
Power on Read Time	T_{rst}	20	-	ns

Notes
1. All electrical and timing parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.
2. All program signals that align together in the timing diagrams should be derived from the rising clock edge.
3. All timing measurements are from the 50% of the input to 50% of the output.
4. All input waveforms have rising time (t_r) and falling time (t_f) of 1ns from 10% to 90% of the input waveforms.
5. For capacitive loads greater than 1pF, access time will increase by 1ns per pF of additional loading.
6. Program time means one byte program time in user mode

Scan Mode Setting

The LGDP4551 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the LGDP4551 and the LCD panel.

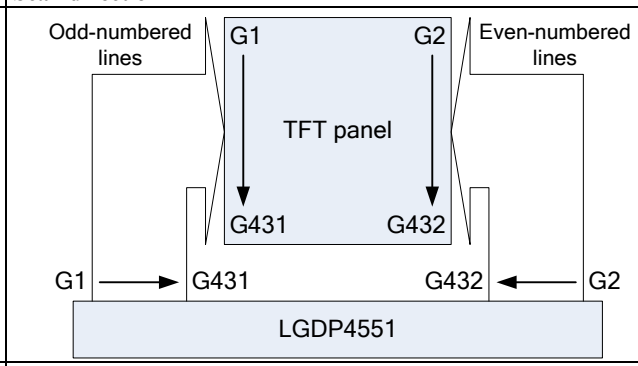
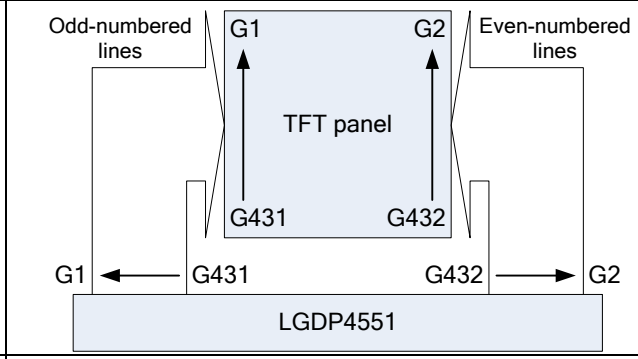
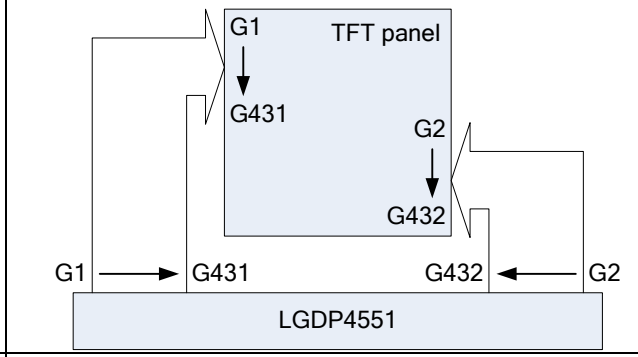
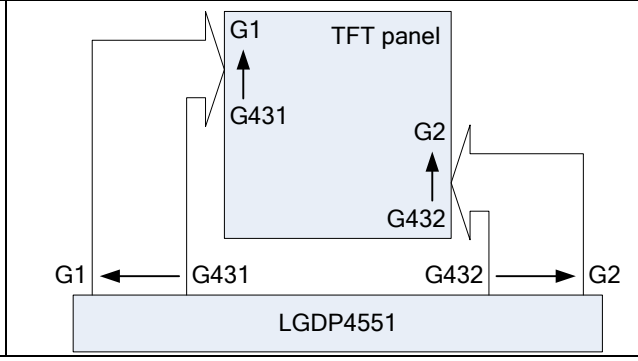
SM	GS	Scan direction	
0	0		G1, G2, G3, G4, …, G430, G431, G432
0	1		G432, G431, G430, …, G4, G3, G2, G1
1	0		G1, G3, G5, …, G429, G431, G2, G4, G6, …, G430, G432
1	1		G432, G430, G428, …, G6, G4, G2, G431, G429, G427, …, G5, G3, G1

Figure 60

Line Inversion AC Drive

The LGDP4551, in addition to the frame-inversion liquid crystal AC drive, supports the n-line inversion AC drive, in which the polarity of liquid crystal is inverted in units of n lines, where n takes a number from 1 to 64. The quality of display will be improved by using n-line inversion AC drive.
In determining n (the value set with the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells .

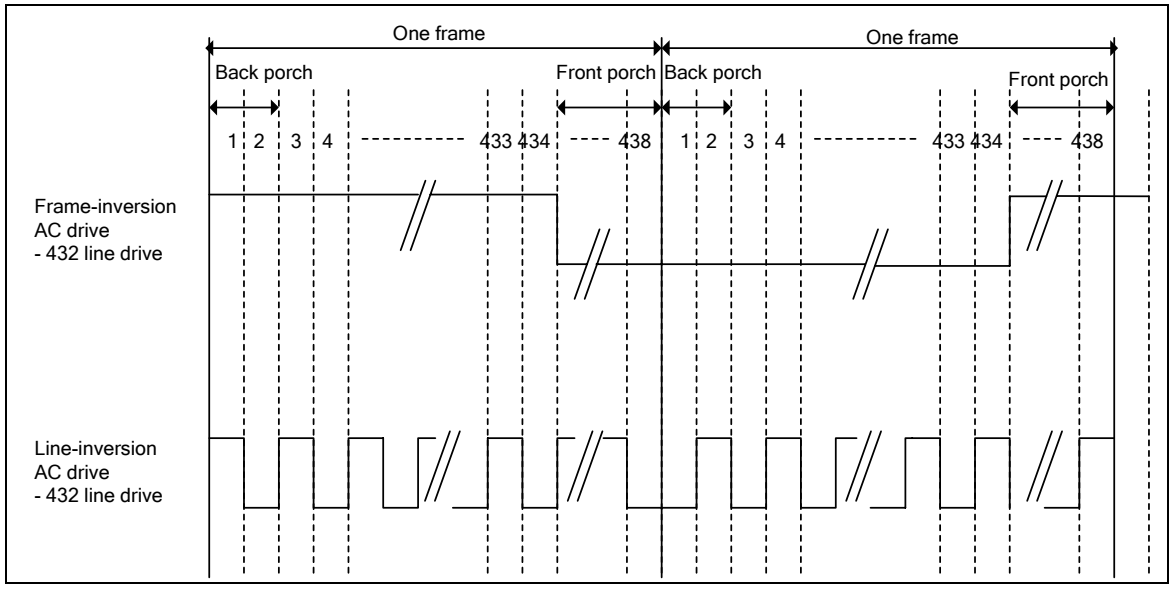


Figure 61 Example of Alternating Signals for n-line Inversion

Frame-Frequency Adjustment Function

The LGDP4551 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting the DIVI/E, RTNI/E bits without changing the oscillation frequency.

To switch frame frequencies according to whether displaying a moving picture or displaying a still picture, set a high oscillation frequency in advance. Then, set a low frame frequency to save power consumption when displaying a still picture. When displaying a moving picture, set the frequency high.

Relationship between the liquid crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frqme frequency is calaulated from the following equation. The frame frequency can be adjusted by setting the 1H period adjustment (RTNI/E) bit and the operation clock division (DIVI/E) bit.

Equlation for calculating frame frequency

$$Frame\ Frequency = \frac{Fosc}{Number\ Of\ Clocks\ Per\ Line \times Division\ Ratio \times (Line + FP + BP)}$$

Fosc	: RC oscillation frequency
Number of Clocks per line	: RTNI/E bit
Division Ratio	: DIVI/E bit
Line	: number of lines to drive the LCD (NL bit)
FP	: Number of lines for front porch
BP	: Number of lines for back porch

Example of Calculation : when maximum frame frequency = 70Hz

Number of lines : 432 lines
1H period : 60 Clock cycles (RTNI/E[7:0] = “00111100”)
Division ratio of operating clock : 1/1
Front porch : 2 lines
Back porch : 14 lines

Fosc = 70 (Hz) x 60 (clocks) x 1/1 x (432 + 2 + 14) (Lines) = 1. 87(MHz)

In this case, the RC oscillation frequency is to set to 1.87MHz. Adjust the value of the external resistor coneected to the RC oscillator so that RC oscillation frequency becomes 1.87MHz.

Partial Display Function

The partial display function allows the LGDP4551 to drive linies selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven with non-display level to reduce power consumption.

The power saving effect can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

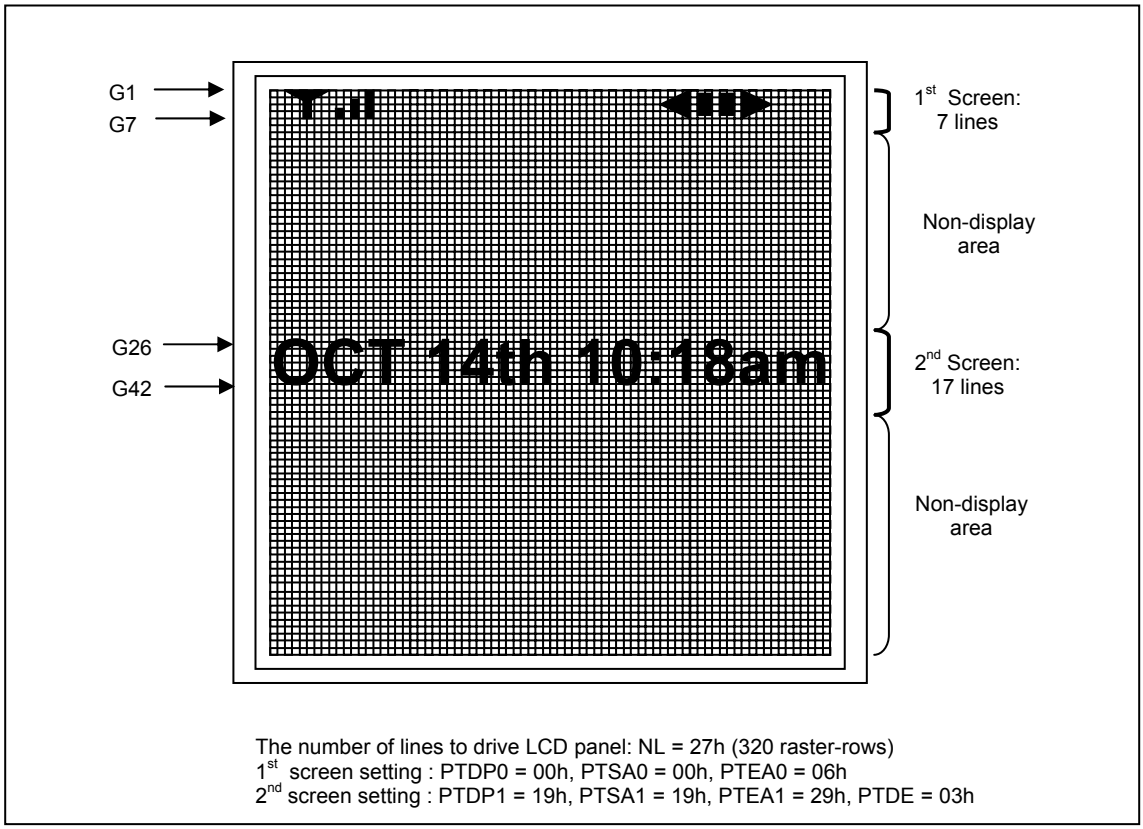


Figure 62

Liquid crystal panel interface timing

The relationships between RGB interface signals and liquid crustal panel control signals in interhal operation and RGB interface operations are as follows.

Internal clock operation

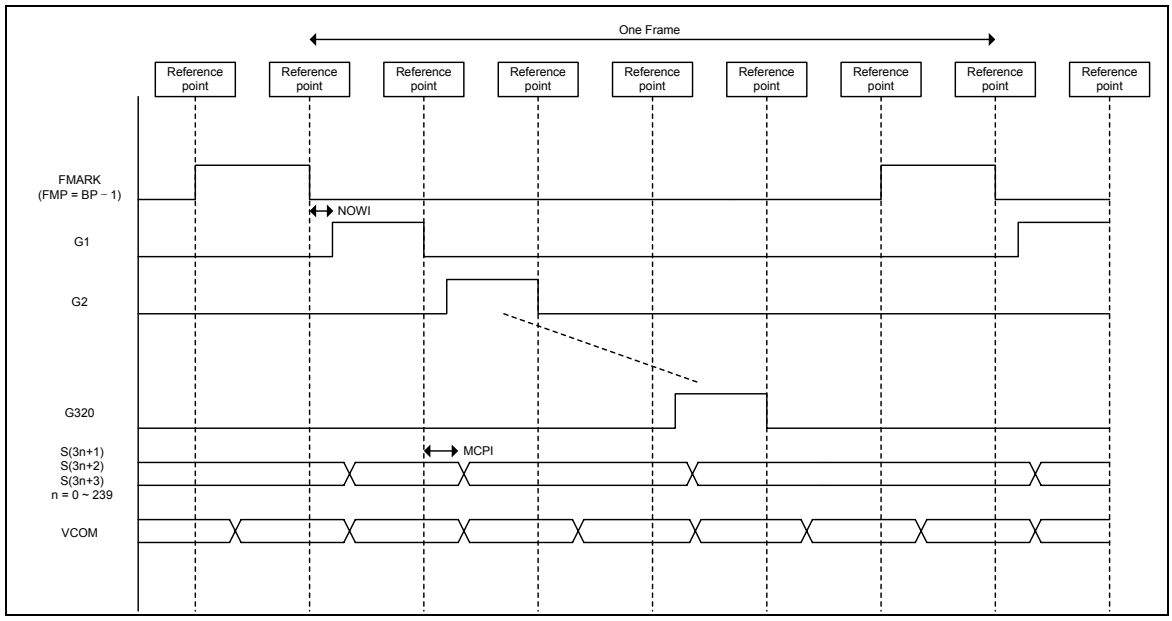


Figure 63

RGB Interface operation

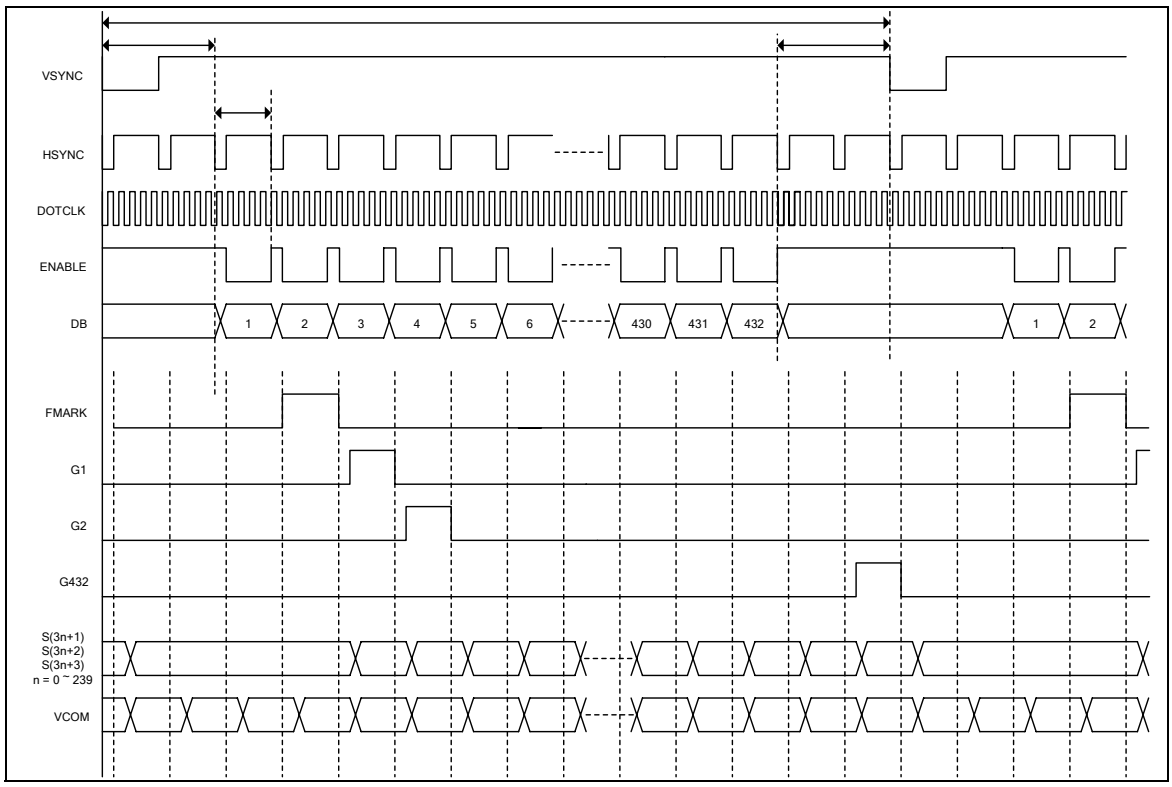


Figure 64

γ-Correction Function

The LGDP4551 has the γ-correction function to display in 262,144 colors simultaneously. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LGDP4551 available with liquid crystal panels of various characteristics.

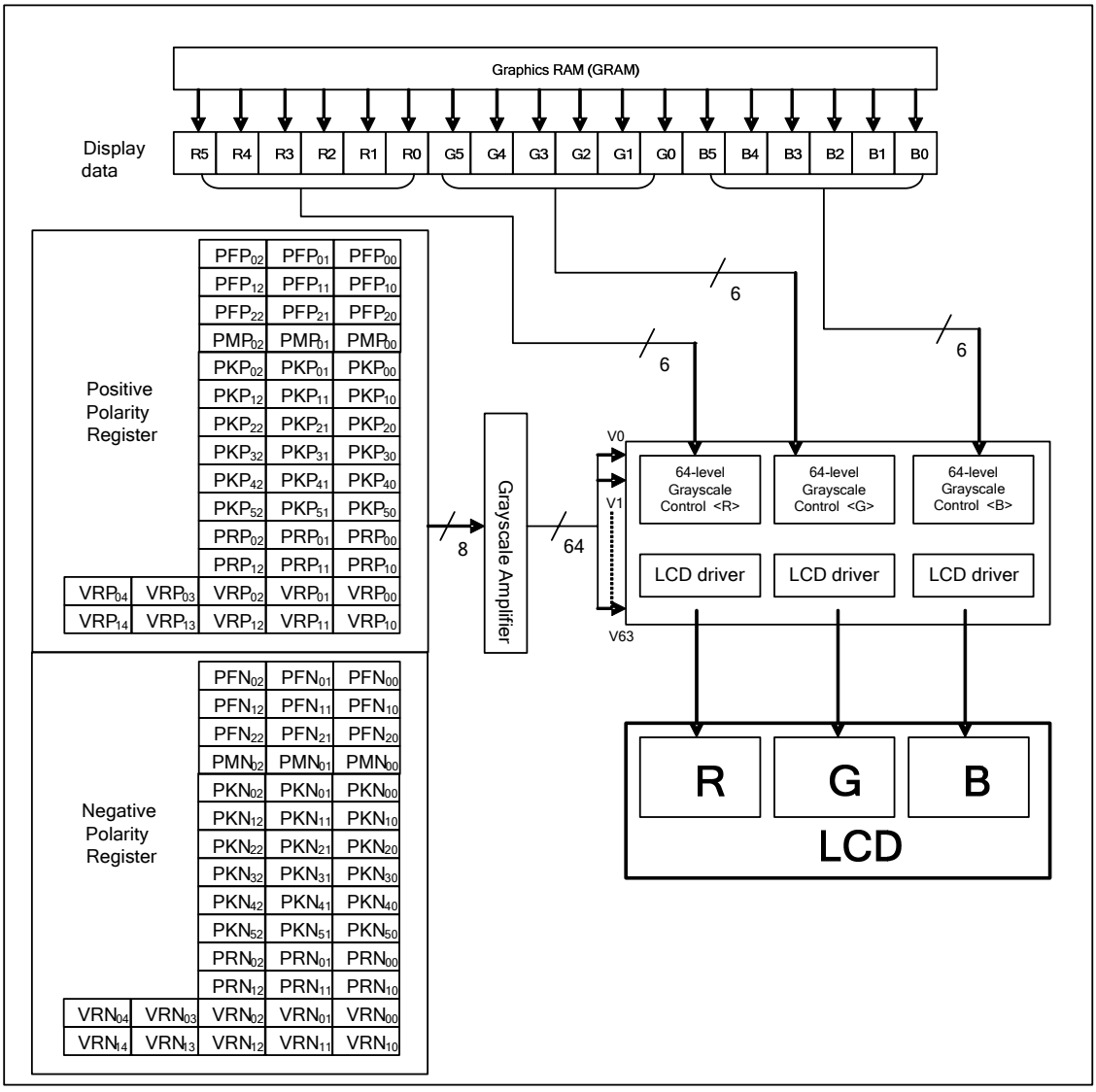


Figure 65 Grayscale control

Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the LGDP4551.

To generate 64 grayscale voltages (V0 to V63), the LGDP4551 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

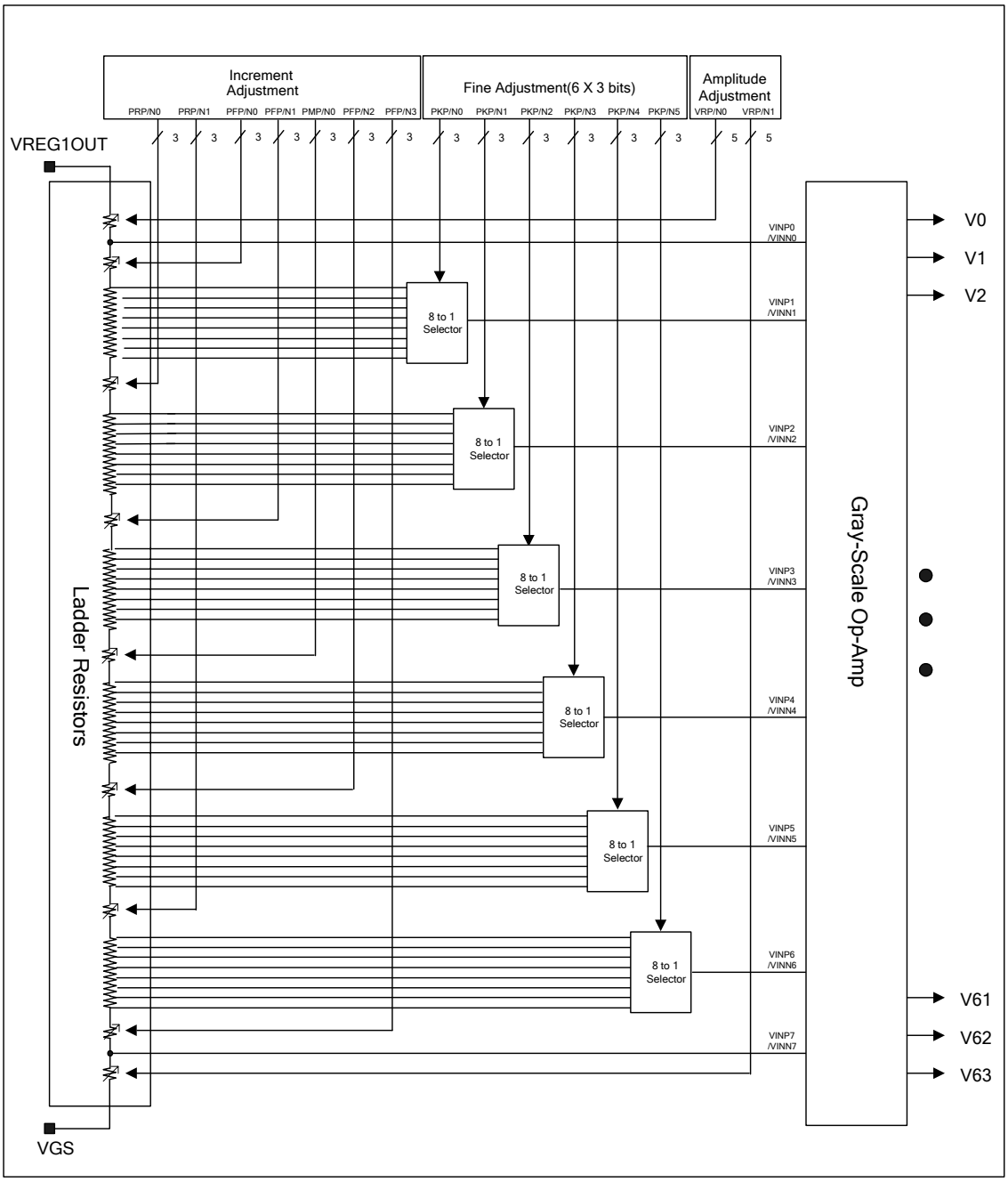


Figure 66 Grayscale amplifier unit

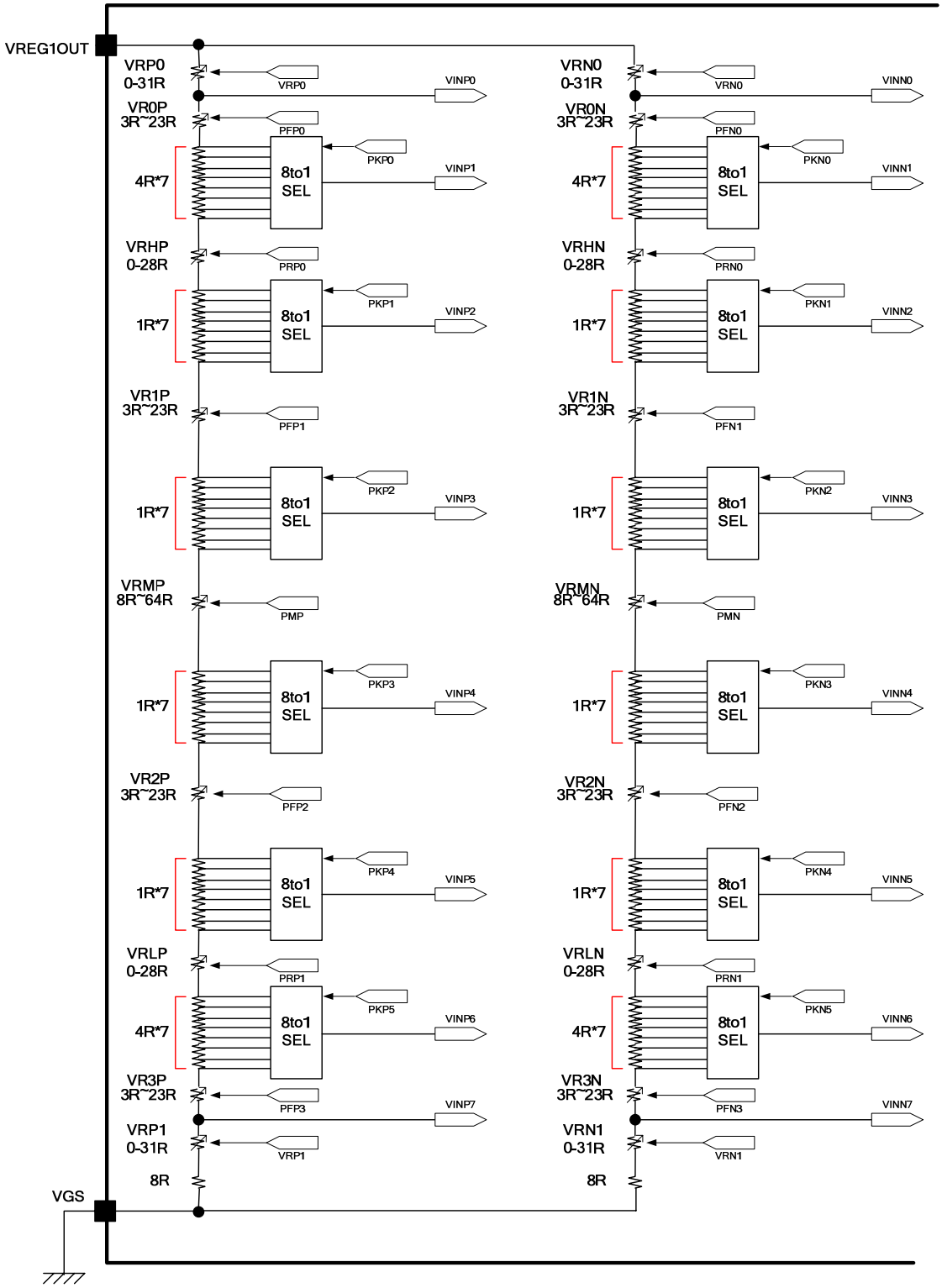


Figure 67 Ladder resistor units and 8-to-1 selectors

γ-Correction Register

The γ-correction registers of the LGDP4551 consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for γ-characteristics of a liquid crystal panel. These γ-correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.

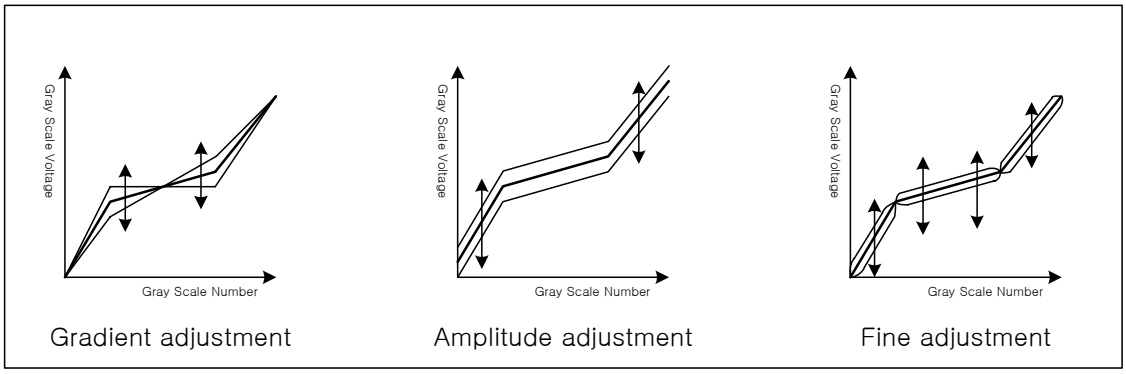


Figure 68

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 90 List of registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
	PFP0[2:0]	PFN0[2:0]	Variable resistor VR0P(N)
	PFP1[2:0]	PFN1[2:0]	Variable resistor VR1P(N)
	PFP2[2:0]	PFN2[2:0]	Variable resistor VR2P(N)
	PFP3[2:0]	PFN3[2:0]	Variable resistor VR3P(N)
	PMP[2:0]	PMN[2:0]	Variable resistor VRMP(N)
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder Resistors and 8-to-1 Selector

Block Configuration

The reference voltage generating unit as illustrated in figure 66 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LGDP4551 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)/VR0~4P(N)/VRMP(N)) and amplitude adjustment (VRP(N)0~1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 91 Gradient adjustment

Contents of register PRP(N)0/1[2:0]	Resistance VRHP(N) VRLP(N)	Contents of register PFP(N)0/1/2/3[2:0]	Resistance VR0/1P(N) VR2/3P(N)	Contents of register PMP(N)[2:0]	Resistance VRMP(N)
000	0R	000	3R	000	8R
001	4R	001	5R	001	16R
010	8R	010	9R	010	24R
011	12R	011	11R	011	32R
100	16R	100	15R	100	40R
101	20R	101	17R	101	48R
110	24R	110	21R	110	56R
111	28R	111	23R	111	64R

.

Table 92 Amplitude adjustment

Contents of register VRP(N)0[4:0]	Resistance VRP(N)0 VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages

Table 93 Fine adjustment registers and selected voltage

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
3'h0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
3'h1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
3'h2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3'h3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
3'h4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
3'h5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
3'h6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
3'h7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formula.

Table 94 Formula for calculating voltage (1)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VREG1OUT - ΔV*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV*(VRP0+VR0P+0R)/SUMRP	PKP0= 3'h0	VINP1
KVP2	VREG1OUT - ΔV*(VRP0+VR0P+4R)/SUMRP	PKP0= 3'h1	
KVP3	VREG1OUT - ΔV*(VRP0+VR0P+8R)/SUMRP	PKP0= 3'h2	
KVP4	VREG1OUT - ΔV*(VRP0+VR0P+12R)/SUMRP	PKP0= 3'h3	
KVP5	VREG1OUT - ΔV*(VRP0+VR0P+16R)/SUMRP	PKP0= 3'h4	
KVP6	VREG1OUT - ΔV*(VRP0+VR0P+20R)/SUMRP	PKP0= 3'h5	
KVP7	VREG1OUT - ΔV*(VRP0+VR0P+24R)/SUMRP	PKP0= 3'h6	
KVP8	VREG1OUT - ΔV*(VRP0+VR0P+28R)/SUMRP	PKP0= 3'h7	
KVP9	VREG1OUT - ΔV*(VRP0+VR0P+28R+VRHP)/SUMRP	PKP1= 3'h0	VINP2
KVP10	VREG1OUT - ΔV*(VRP0+VR0P+29R+VRHP)/SUMRP	PKP1= 3'h1	
KVP11	VREG1OUT - ΔV*(VRP0+VR0P+30R+VRHP)/SUMRP	PKP1= 3'h2	
KVP12	VREG1OUT - ΔV*(VRP0+VR0P+31R+VRHP)/SUMRP	PKP1= 3'h3	
KVP13	VREG1OUT - ΔV*(VRP0+VR0P+32R+VRHP)/SUMRP	PKP1= 3'h4	
KVP14	VREG1OUT - ΔV*(VRP0+VR0P+33R+VRHP)/SUMRP	PKP1= 3'h5	
KVP15	VREG1OUT - ΔV*(VRP0+VR0P+34R+VRHP)/SUMRP	PKP1= 3'h6	
KVP16	VREG1OUT - ΔV*(VRP0+VR0P+35R+VRHP)/SUMRP	PKP1= 3'h7	
KVP17	VREG1OUT - ΔV*(VRP0+VR0/1P+35R+VRHP)/SUMRP	PKP2= 3'h0	VINP3
KVP18	VREG1OUT - ΔV*(VRP0+VR0/1P+36R+VRHP)/SUMRP	PKP2= 3'h1	
KVP19	VREG1OUT - ΔV*(VRP0+VR0/1P+37R+VRHP)/SUMRP	PKP2= 3'h2	
KVP20	VREG1OUT - ΔV*(VRP0+VR0/1P+38R+VRHP)/SUMRP	PKP2= 3'h3	
KVP21	VREG1OUT - ΔV*(VRP0+VR0/1P+39R+VRHP)/SUMRP	PKP2= 3'h4	
KVP22	VREG1OUT - ΔV*(VRP0+VR0/1P+40R+VRHP)/SUMRP	PKP2= 3'h5	
KVP23	VREG1OUT - ΔV*(VRP0+VR0/1P+41R+VRHP)/SUMRP	PKP2= 3'h6	
KVP24	VREG1OUT - ΔV*(VRP0+VR0/1P+42R+VRHP)/SUMRP	PKP2= 3'h7	
KVP25	VREG1OUT - ΔV*(VRP0+VR0/1P+42R+VRHP +VRMP)/SUMRP	PKP3= 3'h0	VINP4
KVP26	VREG1OUT - ΔV*(VRP0+VR0/1P+43R+VRHP +VRMP)/SUMRP	PKP3= 3'h1	
KVP27	VREG1OUT - ΔV*(VRP0+VR0/1P+44R+VRHP +VRMP)/SUMRP	PKP3= 3'h2	
KVP28	VREG1OUT - ΔV*(VRP0+VR0/1P+45R+VRHP +VRMP)/SUMRP	PKP3= 3'h3	
KVP29	VREG1OUT - ΔV*(VRP0+VR0/1P+46R+VRHP +VRMP)/SUMRP	PKP3= 3'h4	
KVP30	VREG1OUT - ΔV*(VRP0+VR0/1P+47R+VRHP +VRMP)/SUMRP	PKP3= 3'h5	
KVP31	VREG1OUT - ΔV*(VRP0+VR0/1P+48R+VRHP +VRMP)/SUMRP	PKP3= 3'h6	
KVP32	VREG1OUT - ΔV*(VRP0+VR0/1P+49R+VRHP +VRMP)/SUMRP	PKP3= 3'h7	
KVP33	VREG1OUT - ΔV*(VRP0+VR0/1/2P+49R+VRHP +VRMP)/SUMRP	PKP4= 3'h0	VINP5
KVP34	VREG1OUT - ΔV*(VRP0+VR0/1/2P+50R+VRHP +VRMP)/SUMRP	PKP4= 3'h1	
KVP35	VREG1OUT - ΔV*(VRP0+VR0/1/2P+51R+VRHP +VRMP)/SUMRP	PKP4= 3'h2	
KVP36	VREG1OUT - ΔV*(VRP0+VR0/1/2P+52R+VRHP +VRMP)/SUMRP	PKP4= 3'h3	
KVP37	VREG1OUT - ΔV*(VRP0+VR0/1/2P+53R+VRHP +VRMP)/SUMRP	PKP4= 3'h4	
KVP38	VREG1OUT - ΔV*(VRP0+VR0/1/2P+54+VRHP +VRMP)/SUMRP	PKP4= 3'h5	
KVP39	VREG1OUT - ΔV*(VRP0+VR0/1/2P+55R+VRHP +VRMP)/SUMRP	PKP4= 3'h6	
KVP40	VREG1OUT - ΔV*(VRP0+VR0/1/2P+56R+VRHP +VRMP)/SUMRP	PKP4= 3'h7	
KVP41	VREG1OUT - ΔV*(VRP0+VR0/1/2P+56R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h0	VINP6
KVP42	VREG1OUT - ΔV*(VRP0+VR0/1/2P+60R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h1	
KVP43	VREG1OUT - ΔV*(VRP0+VR0/1/2P+64R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h2	
KVP44	VREG1OUT - ΔV*(VRP0+VR0/1/2P+68R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h3	
KVP45	VREG1OUT - ΔV*(VRP0+VR0/1/2P+72R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h4	

KVP46	VREG1OUT - ΔV*(VRP0+VR0/1/2P+76R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h5	
KVP47	VREG1OUT - ΔV*(VRP0+VR0/1/2P+80R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h6	
KVP48	VREG1OUT - ΔV*(VRP0+VR0/1/2P+84R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h7	
KVP49	VREG1OUT - ΔV*(VRP0+VR0/1/2/3P+84R+VRHP+VRMP +VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors = 92R+VRHP+VRLP+VRP0+VRP1+VR0P+VR1P+VR2P +VR3P+VRMP

ΔV : Difference in electrical potential between VREG1OUT and VGS

Table 95 Formula for calculating voltage (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	VINP2+(VINP1-VINP2)*(30/48)
V3	VINP2+(VINP1-VINP2)*(23/48)
V4	VINP2+(VINP1-VINP2)*(16/48)
V5	VINP2+(VINP1-VINP2)*(12/48)
V6	VINP2+(VINP1-VINP2)*(8/48)
V7	VINP2+(VINP1-VINP2)*(4/48)
V8	VINP2
V9	VINP3+(VINP2-VINP3)*(22/24)
V10	VINP3+(VINP2-VINP3)*(20/24)
V11	VINP3+(VINP2-VINP3)*(18/24)
V12	VINP3+(VINP2-VINP3)*(16/24)
V13	VINP3+(VINP2-VINP3)*(14/24)
V14	VINP3+(VINP2-VINP3)*(12/24)
V15	VINP3+(VINP2-VINP3)*(10/24)
V16	VINP3+(VINP2-VINP3)*(8/24)
V17	VINP3+(VINP2-VINP3)*(6/24)
V18	VINP3+(VINP2-VINP3)*(4/24)
V19	VINP3+(VINP2-VINP3)*(2/24)
V20	VINP3
V21	VINP4+(VINP3-VINP4)*(22/23)
V22	VINP4+(VINP3-VINP4)*(21/23)
V23	VINP4+(VINP3-VINP4)*(20/23)
V24	VINP4+(VINP3-VINP4)*(19/23)
V25	VINP4+(VINP3-VINP4)*(18/23)
V26	VINP4+(VINP3-VINP4)*(17/23)
V27	VINP4+(VINP3-VINP4)*(16/23)
V28	VINP4+(VINP3-VINP4)*(15/23)
V29	VINP4+(VINP3-VINP4)*(14/23)
V30	VINP4+(VINP3-VINP4)*(13/23)
V31	VINP4+(VINP3-VINP4)*(12/23)

Grayscale voltage	Formula
V32	VINP4+(VINP3-VINP4)*(11/23)
V33	VINP4+(VINP3-VINP4)*(10/23)
V34	VINP4+(VINP3-VINP4)*(9/23)
V35	VINP4+(VINP3-VINP4)*(8/23)
V36	VINP4+(VINP3-VINP4)*(7/23)
V37	VINP4+(VINP3-VINP4)*(6/23)
V38	VINP4+(VINP3-VINP4)*(5/23)
V39	VINP4+(VINP3-VINP4)*(4/23)
V40	VINP4+(VINP3-VINP4)*(3/23)
V41	VINP4+(VINP3-VINP4)*(2/23)
V42	VINP4+(VINP3-VINP4)*(1/23)
V43	VINP4
V44	VINP5+(VINP4-VINP5)*(22/24)
V45	VINP5+(VINP4-VINP5)*(20/24)
V46	VINP5+(VINP4-VINP5)*(18/24)
V47	VINP5+(VINP4-VINP5)*(16/24)
V48	VINP5+(VINP4-VINP5)*(14/24)
V49	VINP5+(VINP4-VINP5)*(12/24)
V50	VINP5+(VINP4-VINP5)*(10/24)
V51	VINP5+(VINP4-VINP5)*(8/24)
V52	VINP5+(VINP4-VINP5)*(6/24)
V53	VINP5+(VINP4-VINP5)*(4/24)
V54	VINP5+(VINP4-VINP5)*(2/24)
V55	VINP5
V56	VINP6+(VINP5-VINP6)*(44/48)
V57	VINP6+(VINP5-VINP6)*(40/48)
V58	VINP6+(VINP5-VINP6)*(36/48)
V59	VINP6+(VINP5-VINP6)*(32/48)
V60	VINP6+(VINP5-VINP6)*(25/48)
V61	VINP6+(VINP5-VINP6)*(18/48)
V62	VINP6
V63	VINP7

Note: Make sure DDVDH-V0 > 0.5V

Relationship between RAM Data and Voltage Output Levels
The relationship between RAM data and source output voltage levels is as follows..

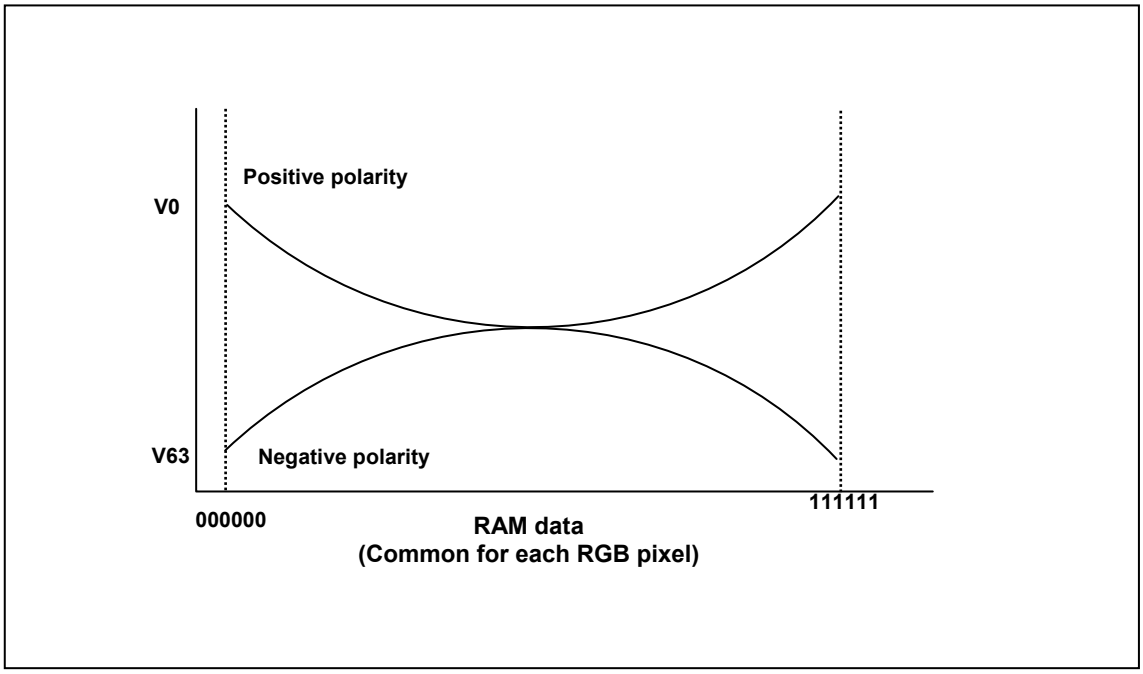


Figure 69 RAM data and the output voltage (REV = "1")

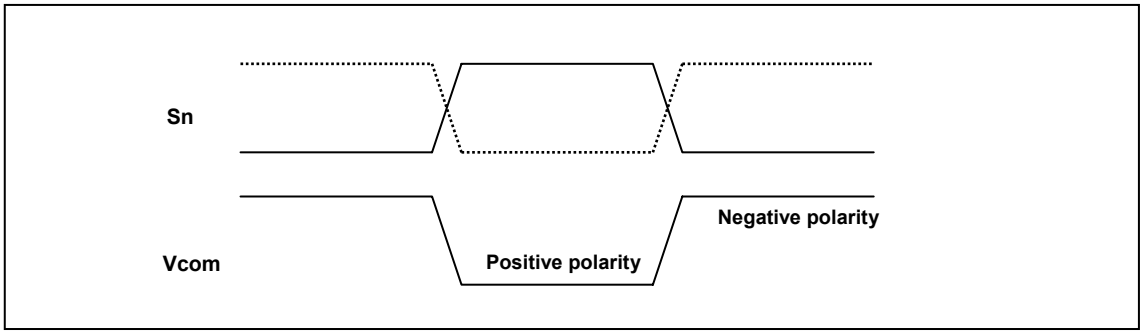


Figure 70 Source output and Vcom

8-Color Display Mode

The LGDP4551 has a function to display in 8colors. In 8-color mode, available grayscale levels are V0 and V63, and the power supplies of other grayscales (V1 to V62) are halted to reduce power consumption.

In 8-color display mode, the MSBs of the respective dot data (R5, G5, B5) are written to the rest of the dot data in order to display in 8 colors without rewriting the RAM data.

The γ- correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.

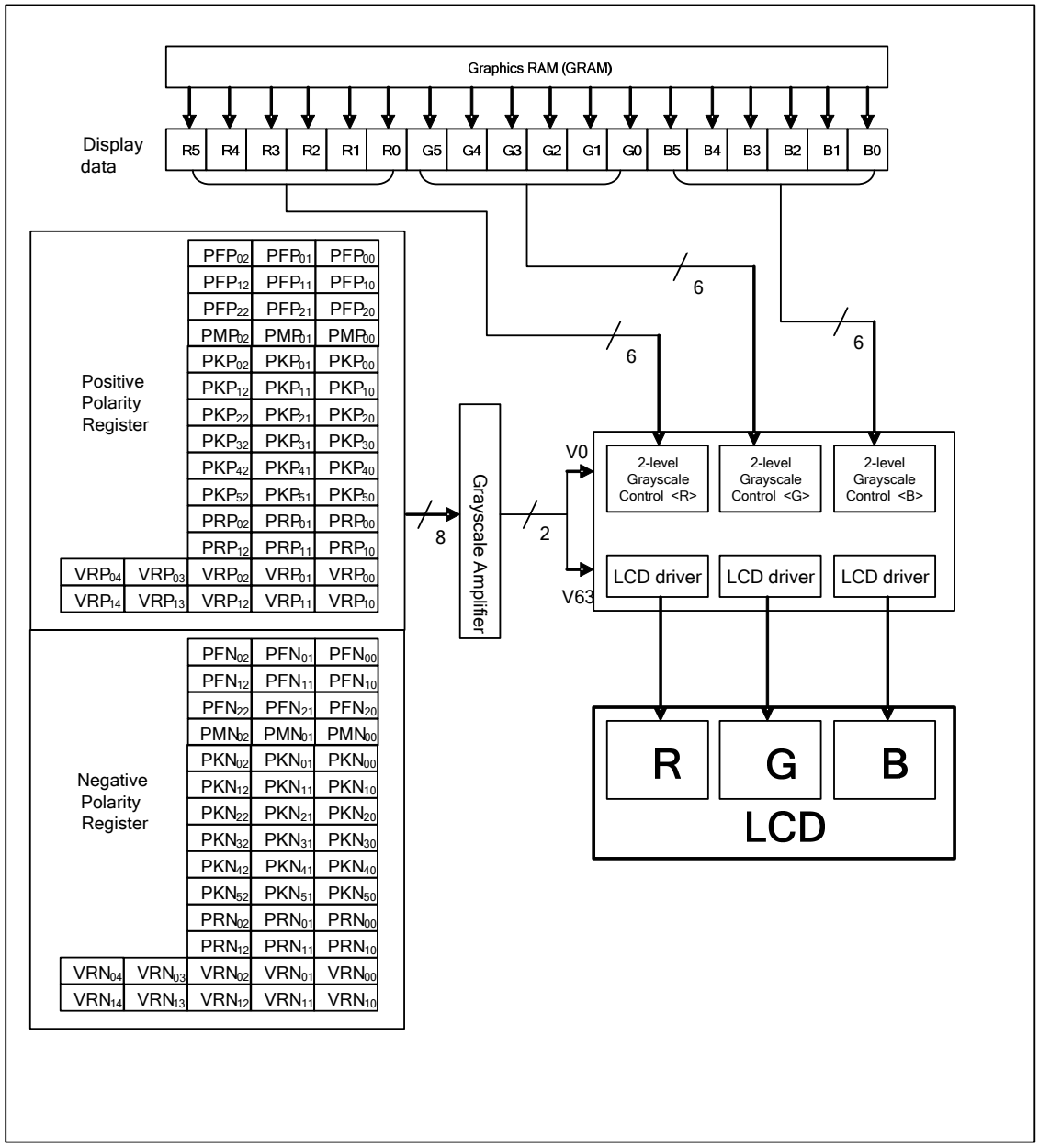


Figure 71 8-color display mode

To switch between the 262,144-color mode and 8-color mode, follow the sequence below.

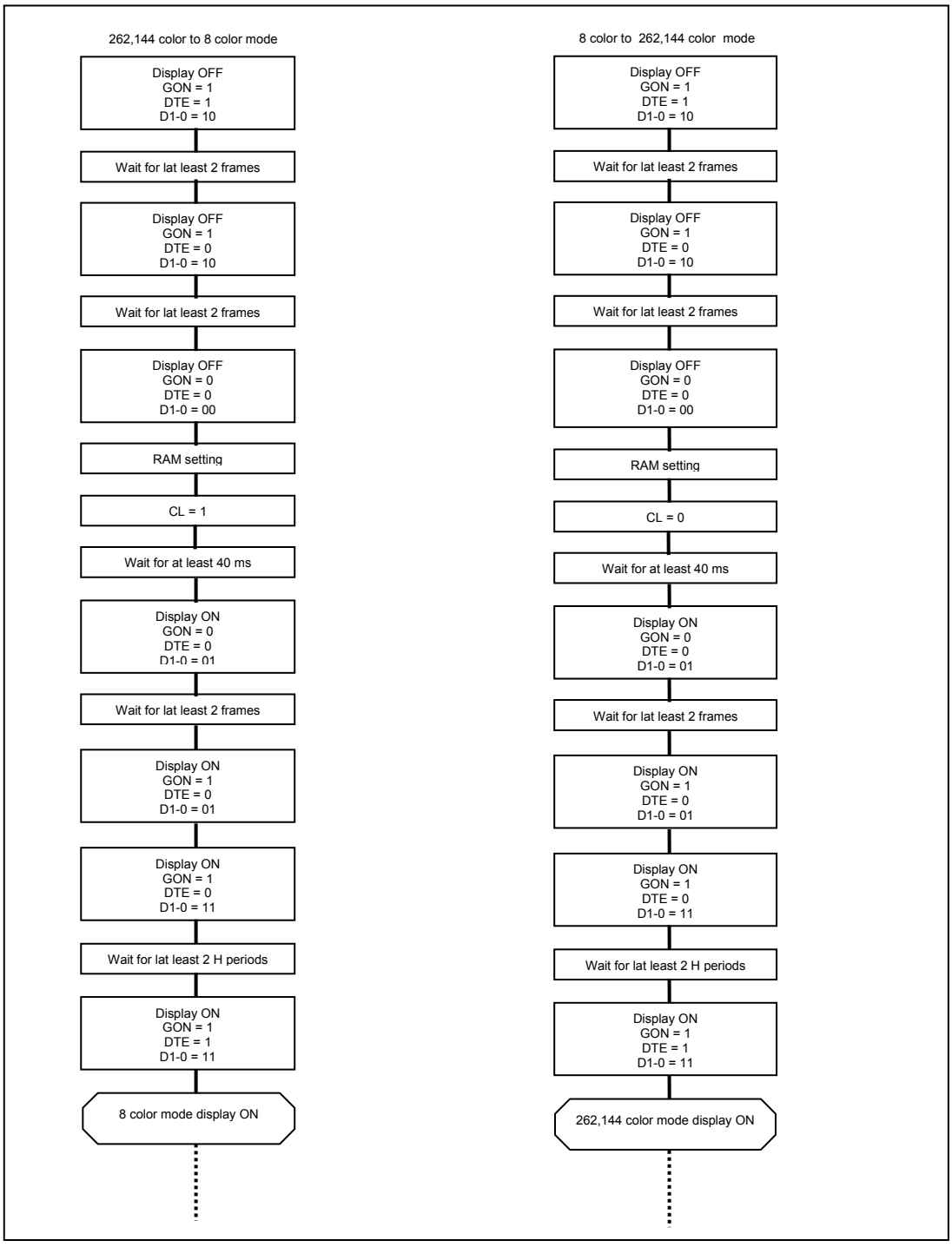


Figure 72

Power-supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the LGDP4551.

Power supply circuit connection example 1 (Vci1 = VciOUT)

In the following example, the VciOUT level is adjusted internally with the VciOUT output circuit.

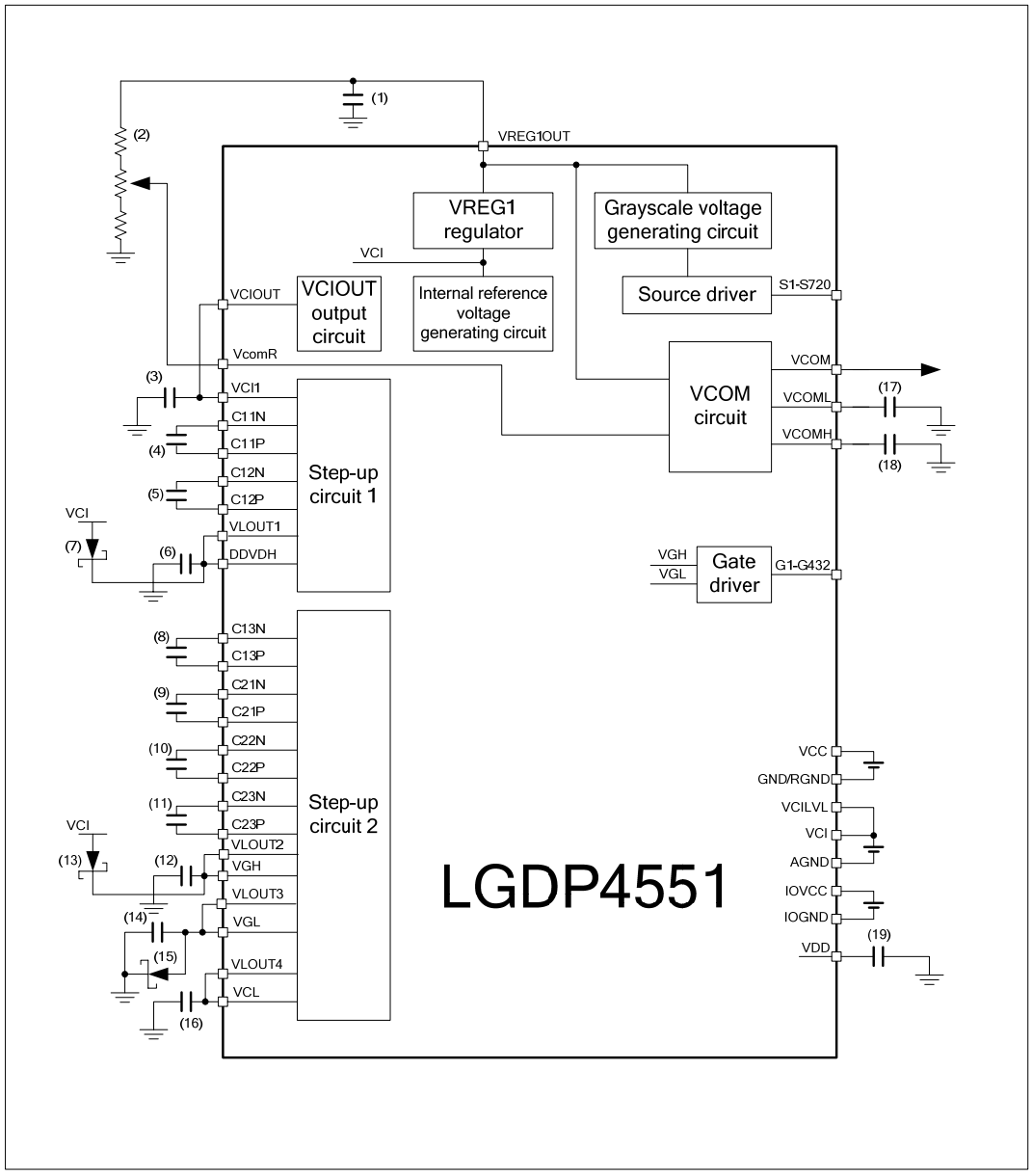


Figure 73

Note: The wiring resistance between the schottky diode and GND/VGL must be 10Ohm or less.

Power supply circuit connection example2 (Vci1 = Vci direct input)

In the following example, the electrical Vci is directly applied to Vci1. In this case, the VciOUT level cannot be adjusted internally but step-up operation becomes more effective

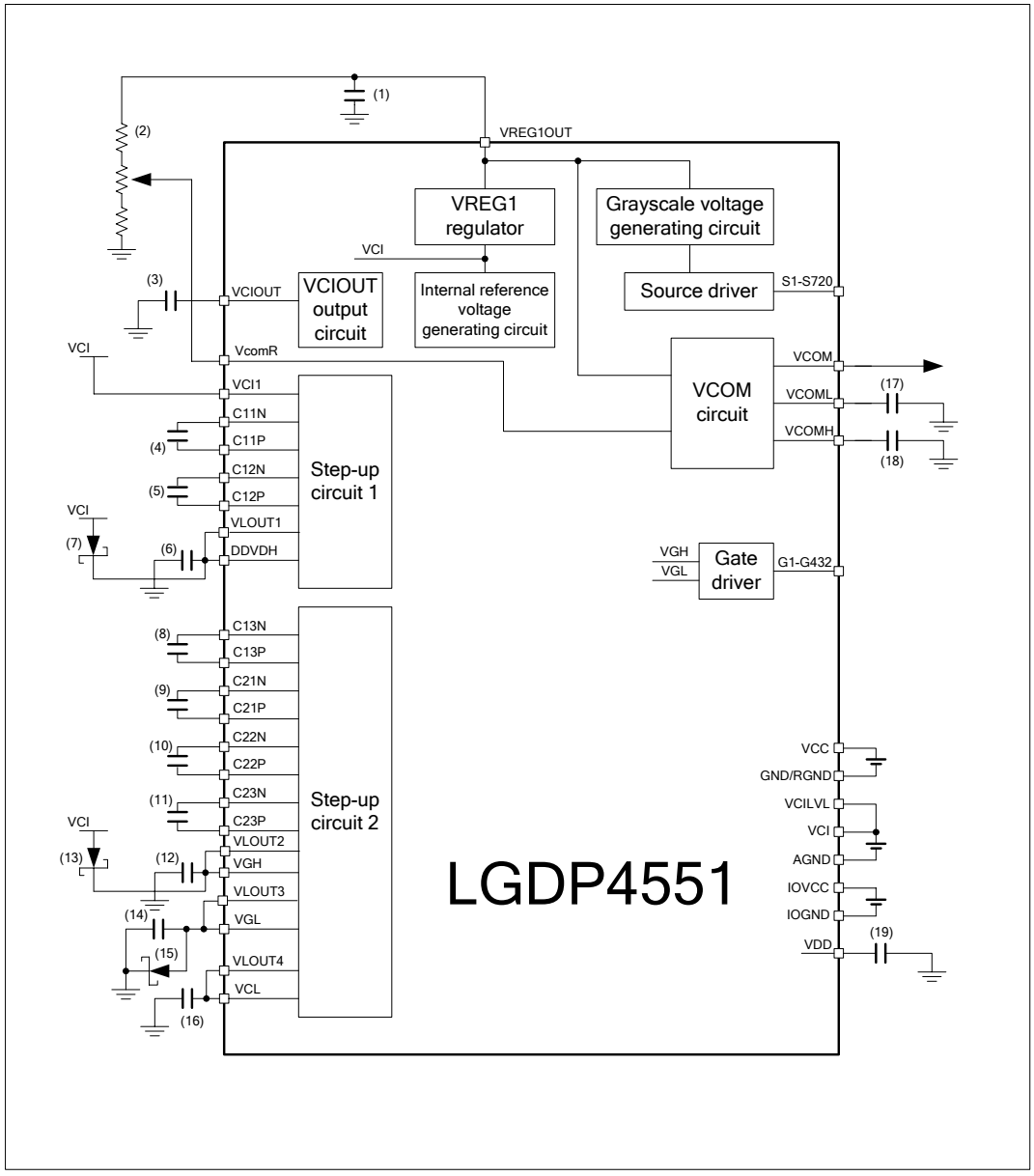


Figure 74

Note: 1. The wiring resistance between the schottky diode and GND/VGL must be 10Ohm or less.
2. When directly applying the Vci level to Vci1, set VC=3'h0.

Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the LGDP4551 are as follows.

Table 96 Capacitor

Capacitance	Voltage proof	Pin Connection
1uF (B characteristics)	6V	(1)VREG1OUT, (3)VciOUT, (4) C11N/P, (5) C12N/P, (8) C13N/P, (16) VLOUT4, (17) VCOML, (18) VCOMH, (19) VDD
	10V	(6) VLOUT1, (9) C21N/P, (10) C22N/P, (11) C23N/P
	25V	(12) VLOUT2, (14) VLOUT3

Notes: 1. Check with the LC module.
2. The numbers in the parentheses corresponds to the numbers of the elements in Figure 72, Figure 73.

Table 97 Schottky Diode

Specification	Pin Connection
VF<0.4 V/20 mA@25℃, VR ≥ 30V	(7) Vci-DDVDH (15) GND-VGL (13) Vci-VGH

Table 98 Variable Resistor

Specification	Pin Connection
>200kΩ	(2) VcomR

Voltage Setting Pattern Diagram

The pattern diagram of voltage setting and waveforms of the liquid crystal application voltages are as follows.

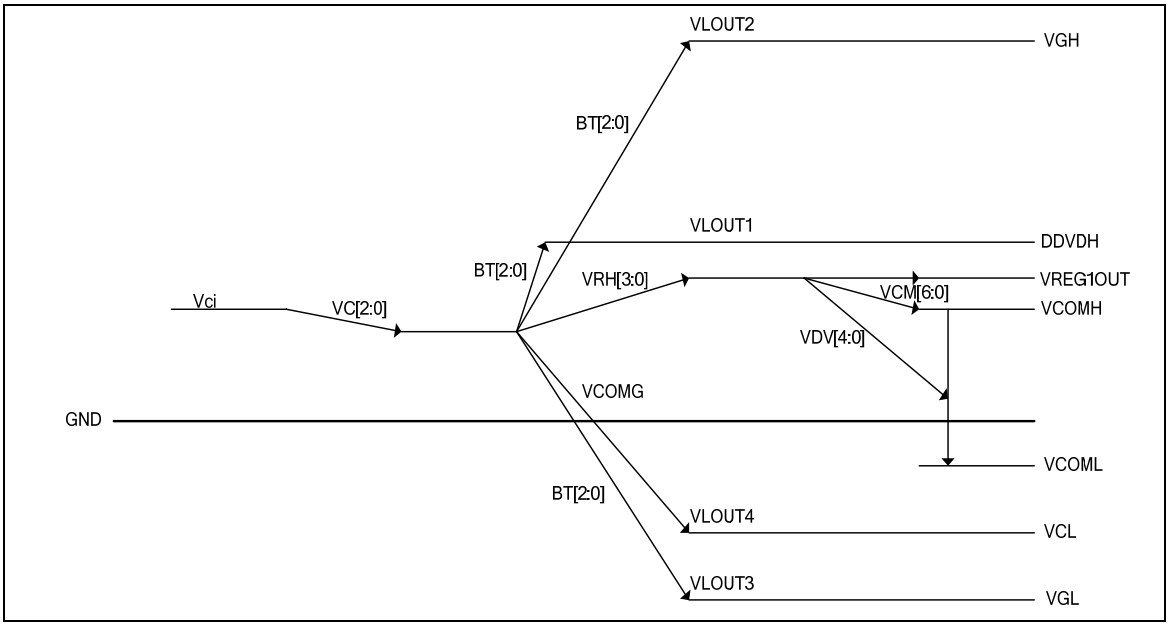


Figure 75 Pattern Diagram for Voltage Setting

Note Output voltages of DDVDH, VGH, VGL, and VCL drop from setting voltage(idea voltage) depending on the current consumption at output. (DDVDH – VREG1OUT) > 0.5V and (VCOML – VGL) > 0.5V are the relation to the actual voltage. When using the voltage in the large current consumption at the fast VCOM2 cycle(such as line-by-line inversion), check the voltage value

Power Supply Instruction Setting

The followings are the sequences for setting power supply ON/OFF. Make power supply ON/OFF settings according to the following sequences in Display ON/OFF, Standby set/exit, Sleep set/exit sequences.

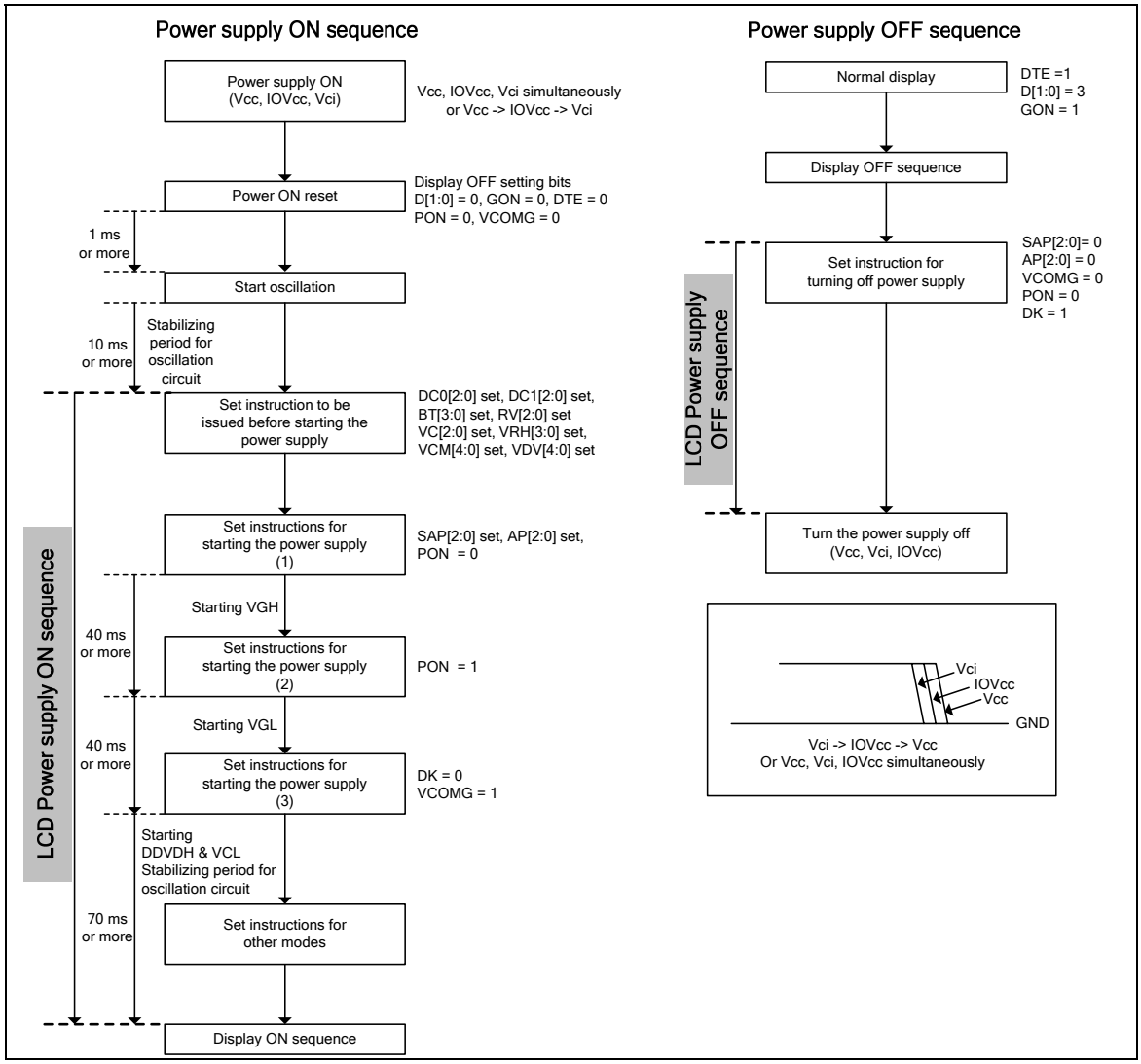


Figure 76

Instruction Setting

The following are the sequences for various instruction settings with the LGDP4551. When making the following instruction settings, follow the respective sequences below.

Display ON/OFF sequence

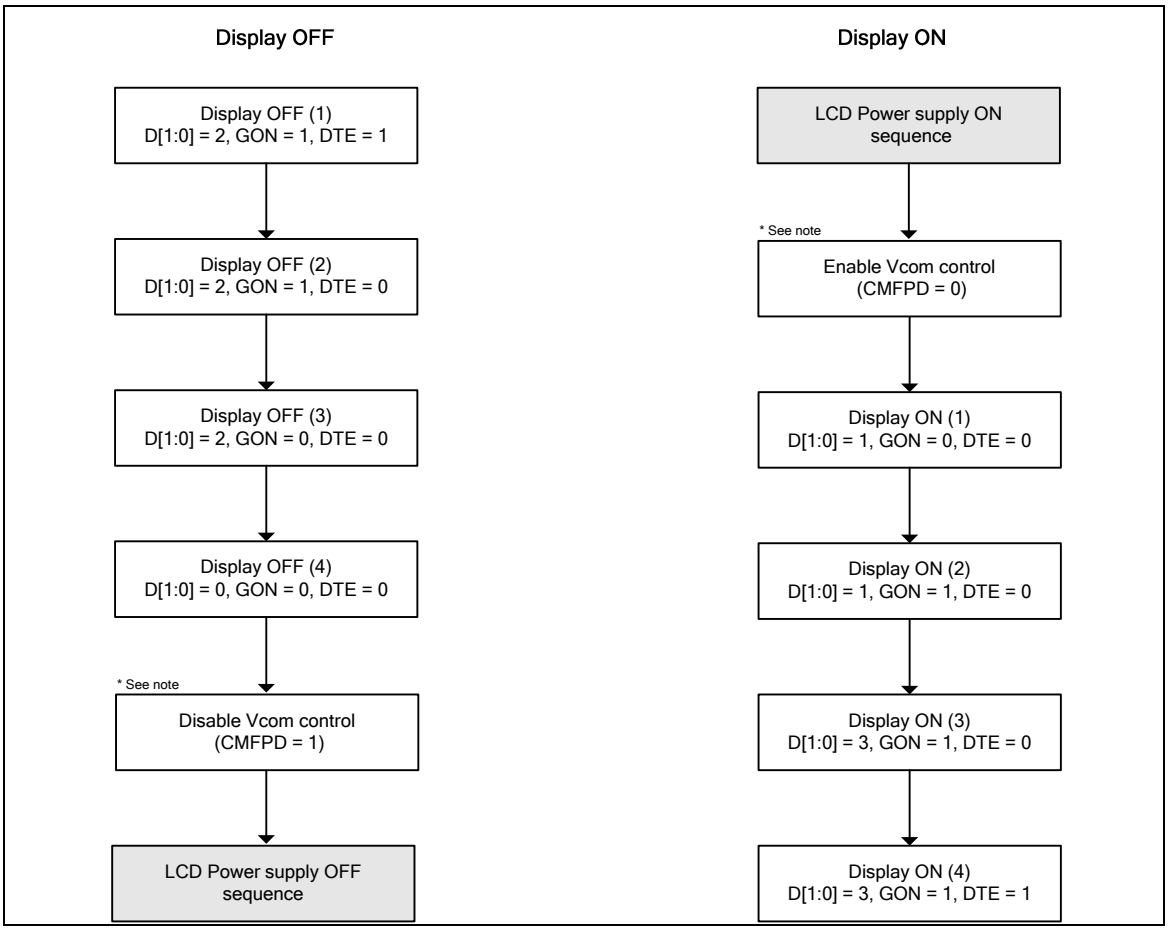


Figure 77

Note : When a line-inversion driving is set, exclude “Vcom feedback control ON/OFF” steps.

Standby / Sleep mode SET/EXIT sequences

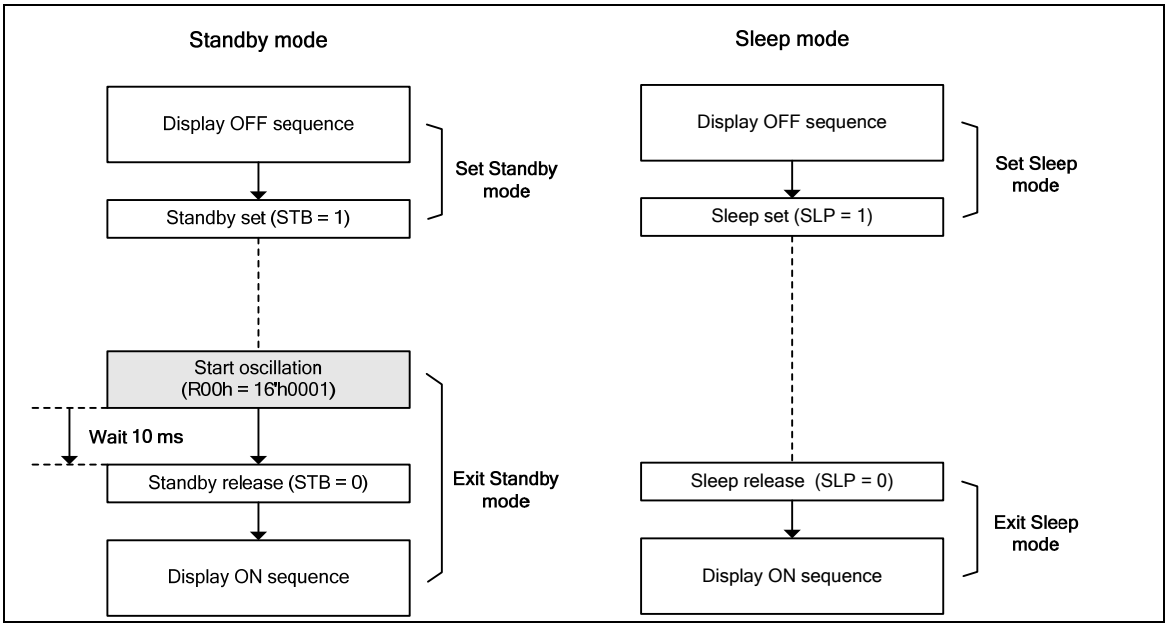


Figure 78

Note : “Display ON/OFF” sequences include “LCD Power Supply ON/OFF” sequences respectively. See “Display ON/OFF sequence” section.

Deep standby mode IN/EXIT sequences

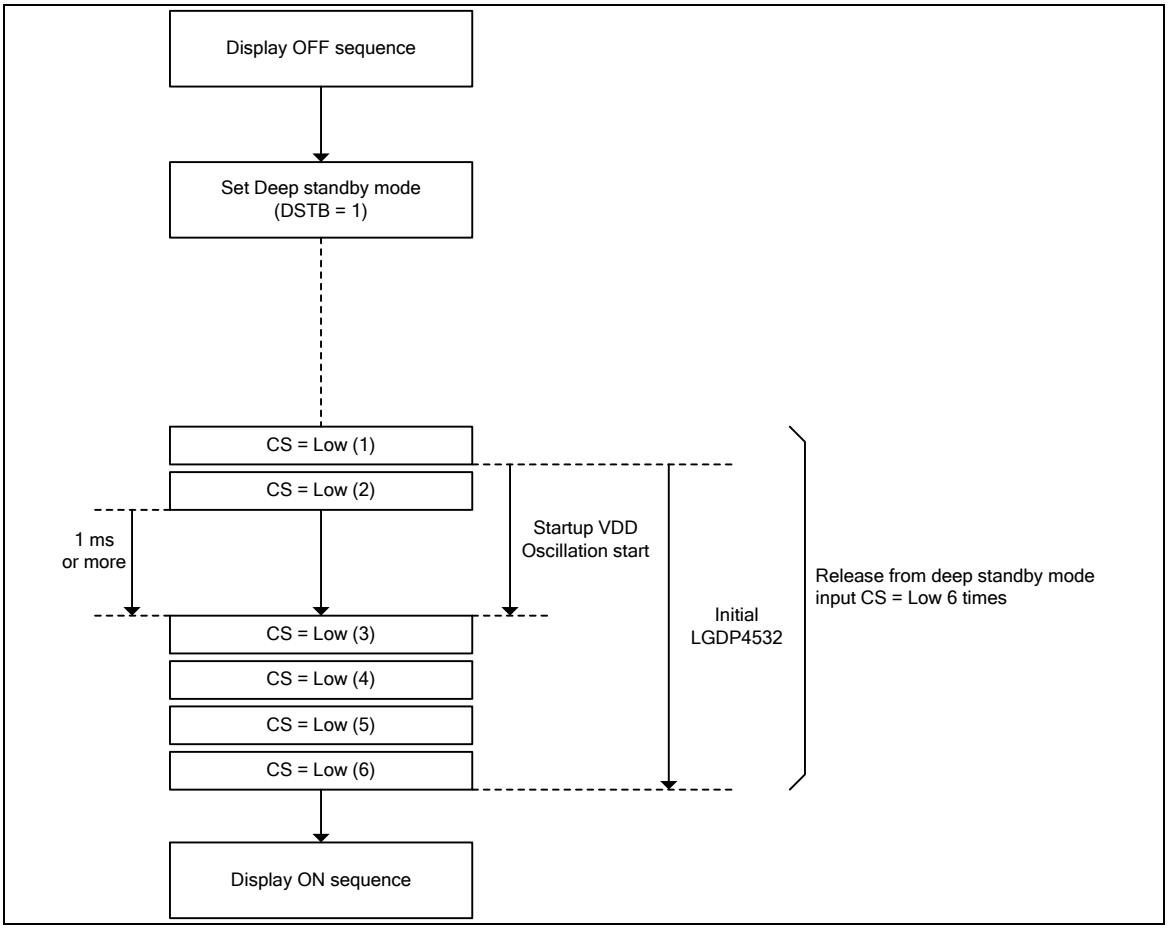


Figure 79

Note : “Display ON/OFF” sequences include “LCD Power Supply ON/OFF” sequences respectively.
See “Display ON/OFF sequence” section.

8-color mode setting

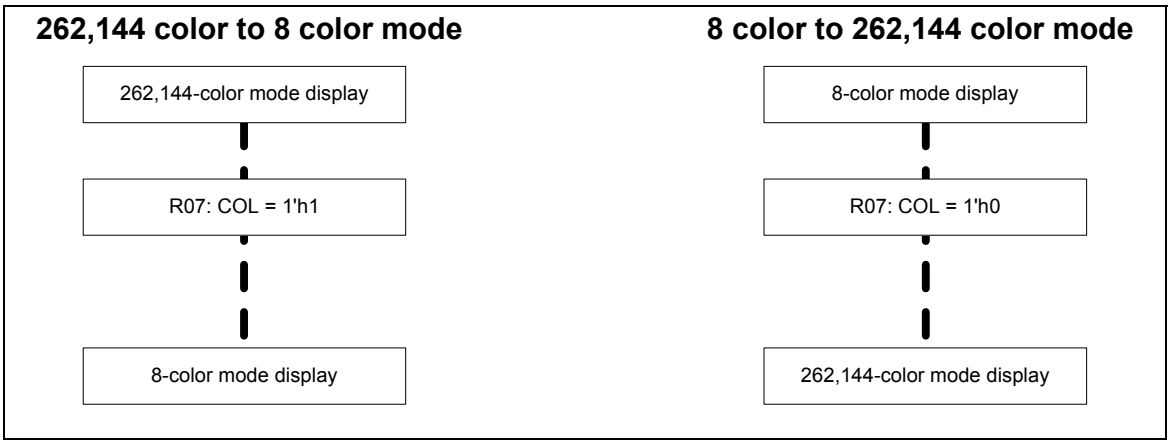


Figure 80

Parital Display setting

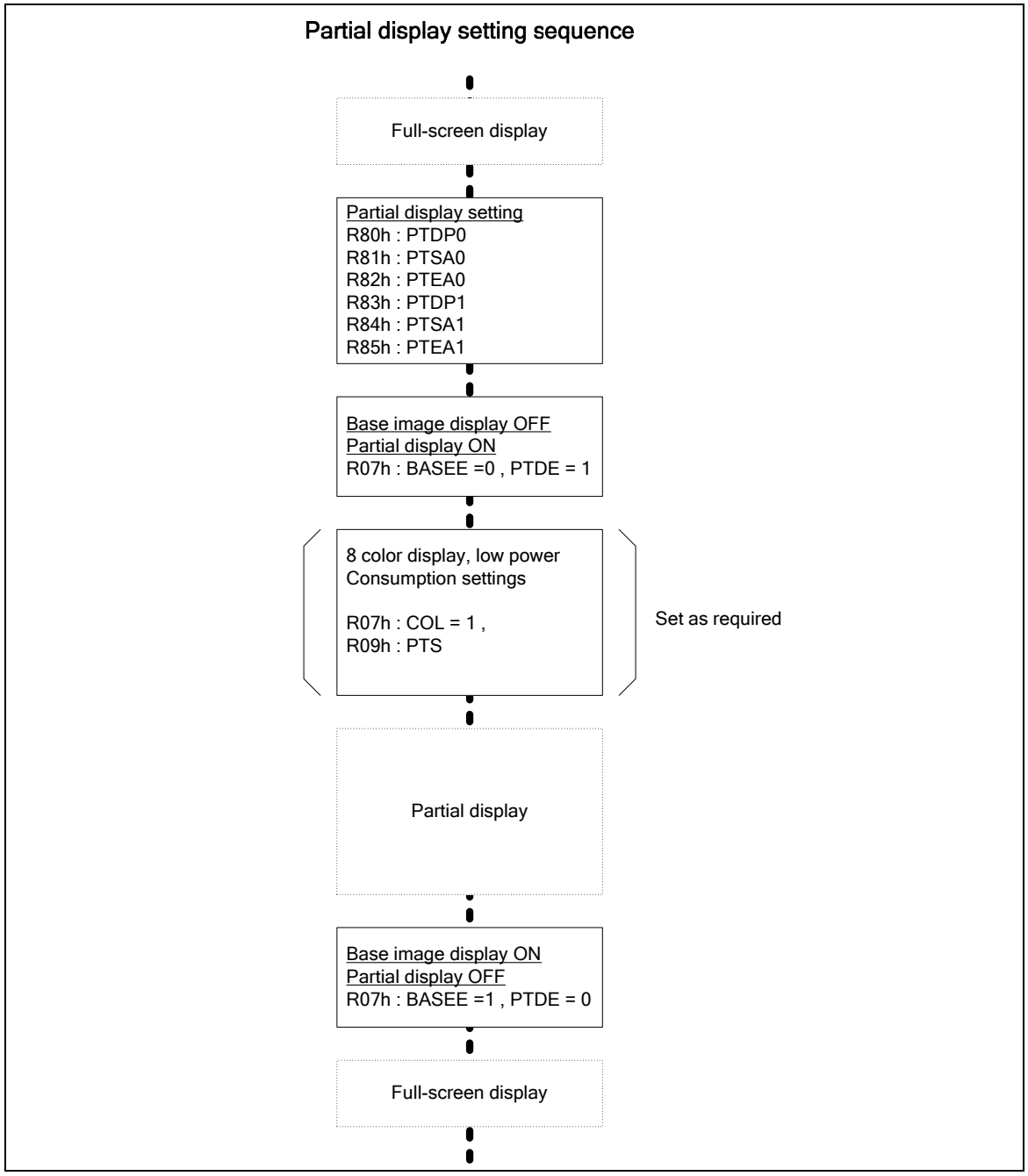


Figure 81

Absolute Maximum Ratings

Table 99

Item	Symbol	Unit	value	Notes
Power supply voltage (1)	Vcc, IOVcc	V	-0.3 ~ +4.5	1, 2
Power supply voltage (2)	Vci – AGND	V	-0.3 ~ +4.5	1, 3
Power supply voltage (3)	DDVDH – AGND	V	-0.3 ~ +8.0	1, 4
Power supply voltage (4)	AGND – VCL	V	-0.3 ~ +4.5	1
Power supply voltage (5)	DDVDH –VCL	V	-0.3 ~ +8.0	1, 5
Power supply voltage (6)	VGH – AGND	V	-0.3 ~ +18	1, 6
Power supply voltage (7)	AGND – VGL	V	-0.3 ~ +18	1, 7
Input voltage	Vt	V	-0.3~IOVcc+0.3	1
Operating temperature	Topr	˚C	-40 ~ +85	1, 8
Storage temperature	Tstg	˚C	-55 ~ +125	1

Note 1) If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.
Note 2) Make sure (High) Vcc ≥ GND (Low), (High) IOVcc ≥ GND (Low).
Note 3) Make sure (High) Vci ≥ GND (Low).
Note 4) Make sure (High) DDVDH ≥ AGND (Low).
Note 5) Make sure (High) DDVDH ≥ VCL (Low).
Note 6) Make sure (High) VGH ≥ AGND (Low).
Note 7) Make sure (High) AGND ≥ VGL (Low).
Note 8) The DC/AC characteristics of die and wafer products is guaranteed at 85 ℃.

Electrical Characteristics

DC Characteristics

Table 100

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Notes
Input high-level voltage	V_{IH}	V	IOVcc = 1.65 ~ 3.3V	0.8IOVcc		IOVcc	2,3
Input low-level voltage	V_{IL}	V	IOVcc = 1.65 ~ 3.3V	0		0.2IOVcc	2,3
Output high-level voltage (1) (DB17-0, SDO, FMARK)	V_{OH1}	V	IOVcc = 1.65 ~ 3.3V I_{OH} = 0.1mA	0.8IOVcc			2
Output lowlevel voltage (1) (DB17-0, SDO, FMARK)	V_{OL1}	V	IOVcc = 1.65~ 3.3V I_{OL} = 0.1mA			0.2IOVcc	2
I/O leakage current	I_{li}	µA	Vin = 0 ~ IOVcc	-1		1	4
Current consumption : Deep standby mode	I_{ST}	µA	IOVcc = Vcc = Vci = 2.8V , Ta ≈ 25°C		1	10	5

80-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 101 See Figure 83 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	t_{CYCW}	ns	70	-	-
		Read	t_{CYCW}	ns	350	-	-
Write “Low” level pulse width Read “Low” level pulse width		Write	PW_{LW}	ns	40	-	-
		Read	PW_{LR}	ns	200	-	-
Write “High” level pulse width Read “High” level pulse width		Write	PW_{HW}	ns	30	-	-
		Read	PW_{HR}	ns	150	-	-
Write/Read rise/fall time			t_{WRr} , t_{WRf}	ns		-	25
Setup time	Write (RS to CS*/ WR*)		t_{AS}	ns	0	-	-
	Read (RS to CS*/ RD*)				10	-	-
Address hold time			t_{AH}	ns	5	-	-
Write data setup time			t_{DSW}	ns	25	-	-
Write data hold time			t_{H}	ns	5	-	-
Read data delay time			t_{DDR}	ns	-	-	200
Read data hold time			t_{DHR}	ns	5	-	-

80-System Bus Interface Timing Characteristics (8/9-Bit Bus)

Table 102 See Figure 83 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	t_{CYCW}	ns	50	-	-
		Read	t_{CYCW}	ns	350	-	-
Write "Low" level pulse width Read "Low" level pulse width		Write	PW_{LW}	ns	25	-	-
		Read	PW_{LR}	ns	200	-	-
Write "High" level pulse width Read "High" level pulse width		Write	PW_{HW}	ns	25	-	-
		Read	PW_{HR}	ns	150	-	-
Write/Read rise/fall time			t_{WRr} , t_{WRf}	ns	-	-	25
Setup time	Write (RS to CS*/ WR*)		t_{AS}	ns	0	-	-
	Read (RS to CS*/ RD*)				10	-	-
Address hold time			t_{AH}	ns	5	-	-
Write data setup time			t_{DSW}	ns	25	-	-
Write data hold time			t_{H}	ns	5	-	-
Read data delay time			t_{DDR}	ns	-	-	200
Read data hold time			t_{DHR}	ns	5	-	-

Serial Peripheral Interface Timing Characteristics

Table 103 See Figure 84 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	50	-	-
	Read (transmitted)	t_{SCYC}	ns	350	-	-
Serial clock "High" level pulse width	Write (received)	t_{SCH}	ns	25	-	-
	Read (transmitted)	t_{SCH}	ns	150	-	-
Serial clock "Low" level pulse width	Write (received)	t_{SCL}	ns	25	-	-
	Read (transmitted)	t_{SCL}	ns	200	-	-
Serial clock rise/fall time		t_{scr} , t_{scf}	ns	-	-	20
Chip select setup time		t_{CSU}	ns	20	-	-
Chip select hold time		t_{CH}	ns	60	-	-
Serial input data setup time		t_{SISU}	ns	30	-	-
Serial input data hold time		t_{SIH}	ns	30	-	-
Serial output data delay time		t_{SOD}	ns	-	-	150
Serial output data hold time		t_{SOH}	ns	5	-	-

RGB Interface Timing Characteristics

Table 104 See Figure 85 (18/16-bit I/F, IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	ns	0	-	-
ENABLE setup time	tENS	ns	10	-	-
ENABLE hold time	tENH	ns	20	-	-
DOTCLK “Low” level pulse width	PWDL	ns	35	-	-
DOTCLK “High” level pulse width	PWDH	ns	35	-	-
DOTCLK cycle time	tCYCD	ns	70	-	-
Data setup time	tPDS	ns	10	-	-
Data hold time	tPDH	ns	25	-	-
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	-	-	25

Reset Timing Characteristics

Table 105 See Figure 86 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset “Low” level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	us	-	-	10

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following are the configurations of I pin, I/O pin, and O pin.

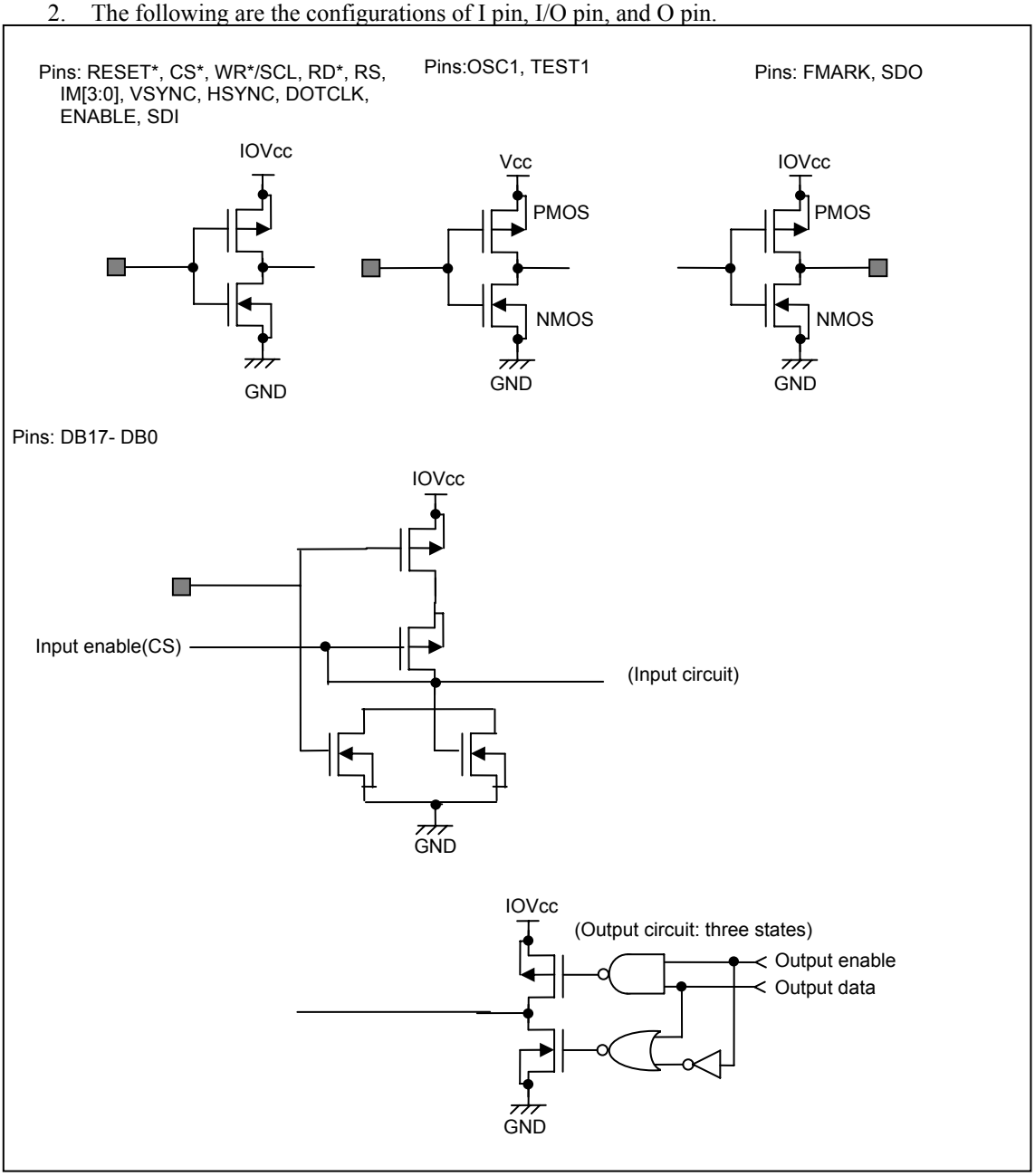


Figure 82

3. The TEST1 pin must be grounded (GND). The IM[3:0] pins must be fixed at either GND or the IOVcc level.
4. This excludes currents though the output drive MOS.
5. This excludes currents flowing through input/output units. Be sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CS* pin is set to “High” or “Low”.

Timing characteristic diagram

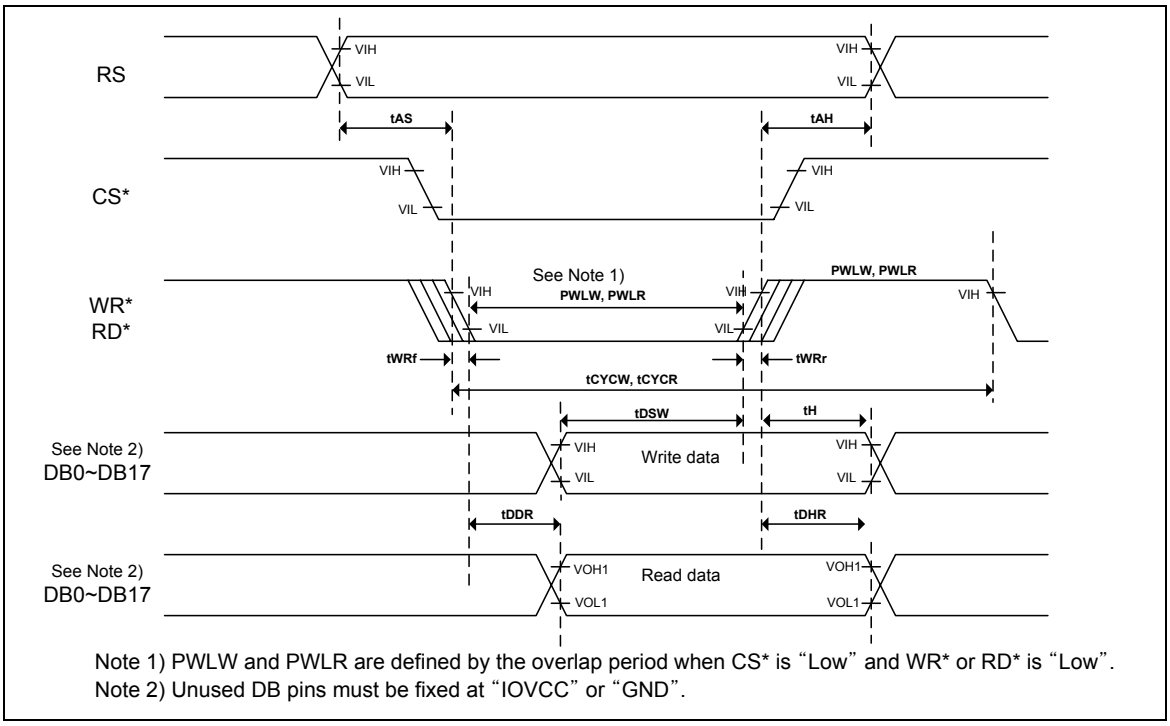


Figure 83 80-system bus interface operation

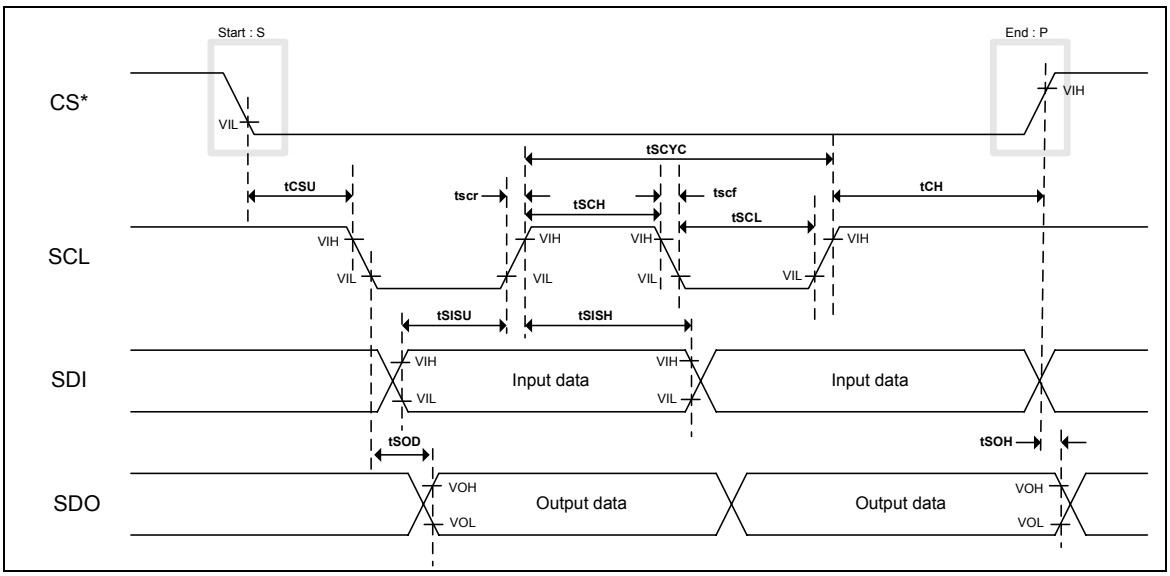


Figure 84 Serial Peripheral interface operation

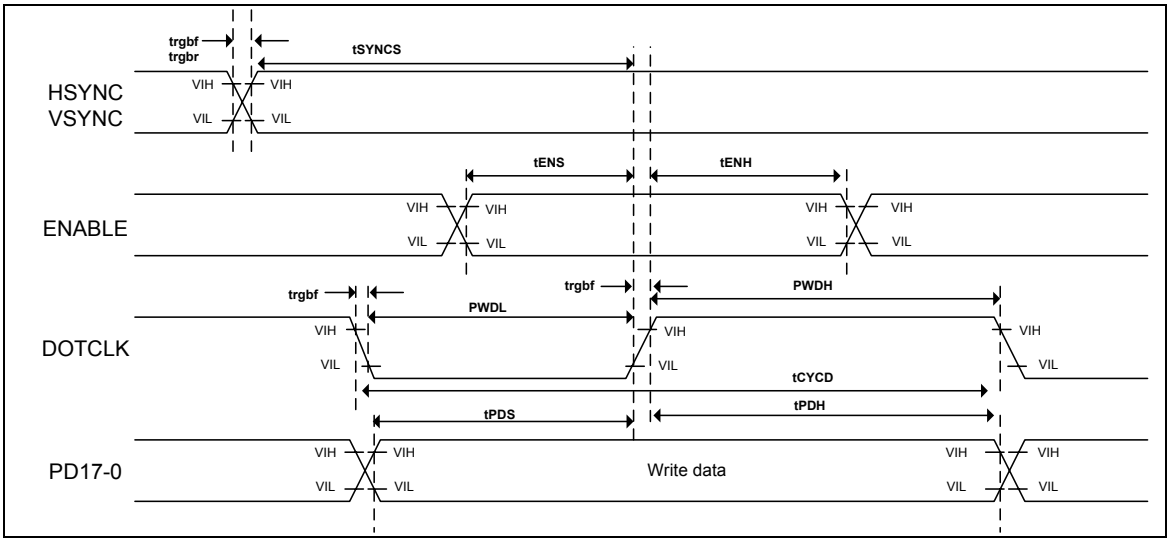


Figure 85 RGB interface operation

Figure 86 Reset operation

Revision History

Rev.	Date	Revision Description	Revised by
0.10	2007.10.15	Preliminary release	S.H. Koh
0.11	2007.10.31	p.78 Add OV, RS_RESET description	S.H. Koh
0.11	2007.10.31	p.7 Modify IM description	S.H. Koh
1.00	2008.03.21	p.76 Added a table of the ratio of oscillator frequency : Table 72	H.C. Kim
1.00	2008.03.21	p.156 ~ 158 Filled in the tables of timing characteristic : Table 101 ~ 105	S.H. Koh