Legend Silicon Corp.®

DMB-TH Demodulator ASIC
LGS-8913-B1
“Kona-Digital”

Product Specifications

DMB-TH

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Revision 1.1

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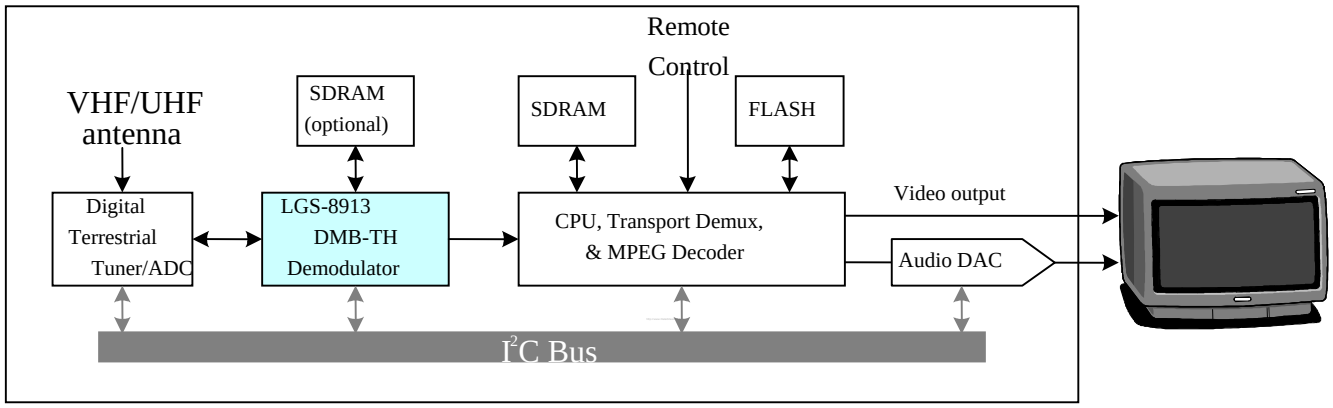
1. OVERVIEW

This LGS-8913-B1 is a single chip TDS-OFDM (Time Domain Synchronous – Orthogonal Frequency Division Multiplexing) demodulator. The demodulator is fully compliant with DMB-TH (Digital Multimedia Broadcasting – Terrestrial/Handheld) specifications and may be integrated into appropriate product designs such as television receivers or set top boxes. It uses a 1.8V core power supply. The device is also compatible with the China DTV standard, with minimal software intervention required (see Appendix for more details)

The chip takes Digital IF or Dual Base-band IQ signal as an input, converts and then performs the necessary demodulation, and then provides an MPEG-2 transport stream output in parallel or serial format. With optional time de-interleaver memory, a complete DMB-TH RF to MPEG front-end can be designed.

The following figure shows a typical receiver application using the LGS-8913-B1:



KEY FEATURES

- Optimized DMB-TH compliant single chip demodulator
- Optimized for maximum signal resiliency in all conditions (impulse noise, echoes, fading, etc.)
- Supports 64QAM, 16QAM and QPSK sub-carriers for both fixed and mobile applications
- FEC rates of 0.4, 0.6, or 0.8 and guard intervals of 420 (1/9) and 945 (1/4) symbols
- Time de-interleaver: 240 or 720 symbols
- MPEG-2 transport stream output in parallel or serial
- Automatic parameter discovery & update
- Integrated bit error rate and signal to noise monitoring
- Full I^2C bus support with up to eight addresses
- 128 pin LQFP (20 mm x 14 mm x 1.4 mm)

APPLICATIONS

- Digital terrestrial set-top boxes and televisions for home reception of SD/HD TV and related services
- Digital terrestrial receivers for mobile & portable reception of multimedia and related services

2. THEORY OF OPERATION

2.1 Summary

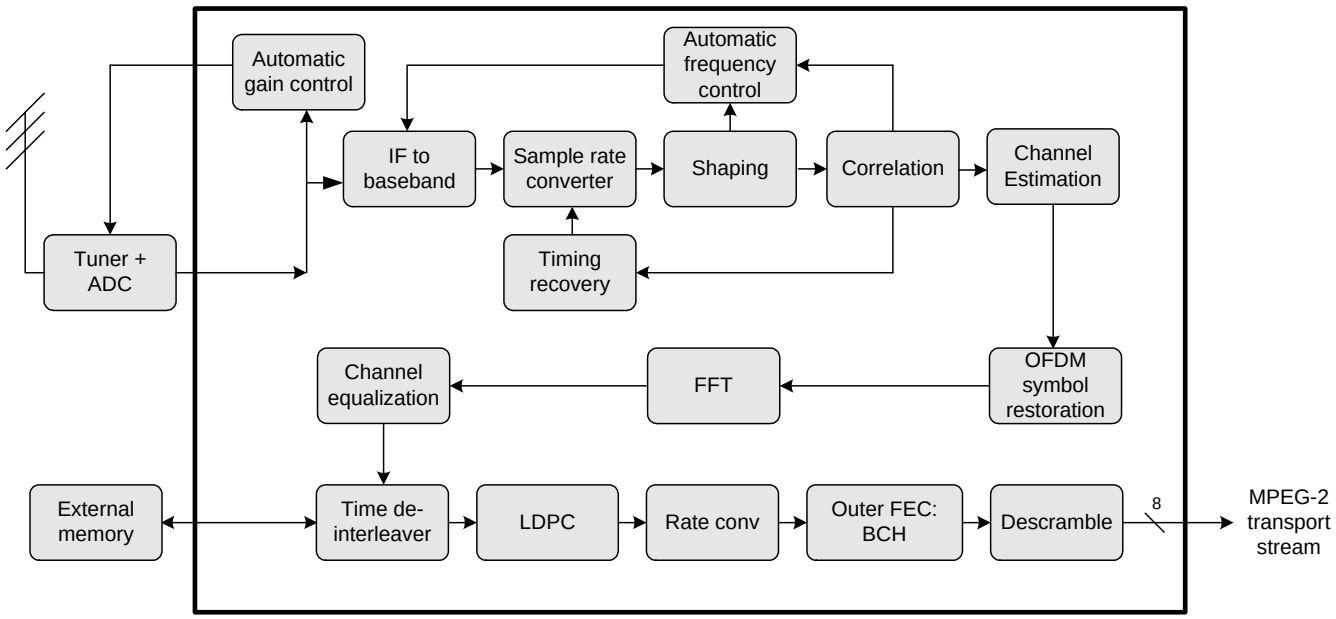
The LGS-8913-B1 in digital mode uses an external terrestrial tuner which converts the analog VHF/UHF signal through an external 10-bit analog to digital ADC(s). The digital output(s) of the ADC(s) is sent to ASIC. Following conversion to base-band, TDS-OFDM demodulation is performed according to the DMB-TH specifications. The output of the channel estimation/correction block is sent to a time de-interleaver and then to the FEC. The output is a parallel or serial MPEG-2 transport stream including data valid, sync, and clock.

LGS-8913 is a drop in replacement for LGS-8813 for boards designed to use Digital IF inputs.

The main parameters may be detected and configured automatically or they may be set manually. The main configurable parameters are:

- Sub-carrier demodulation: QPSK, 16QAM, or 64QAM
- Forward error correction rate: 0.4,0.6, or 0.8
- Guard interval: 420 (1/9) or 945 (1/4) symbols
- Time de-interleaver: 240 or 720 symbols
- Control frame detection
- Channel bandwidth: 6, 7, or 8 MHz (manual set only)

2.2 Block Diagram



2.3 Main DMB-TH Parameters for China DTV

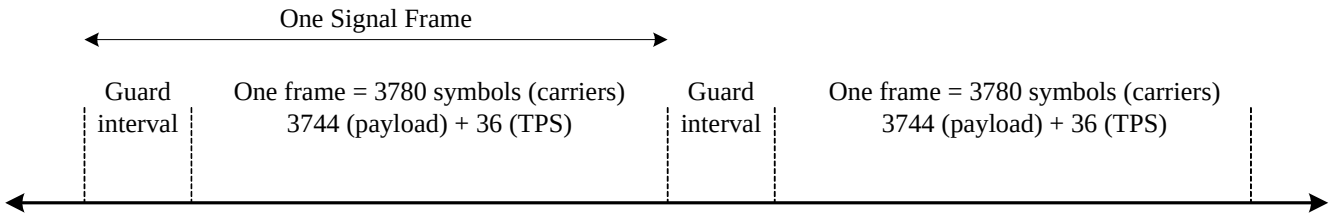
PARAMETER	SPECIFICATION	NOTES
DATA		
Payload format	MPEG-2 transport stream	188 bytes per packet
Payload rate formula	(188 bytes * 8 bits/byte * N) / (frame length + guard interval)	N = 2, 3, or 4 for 4QAM, 4, 6 or 8 for 16QAM, 6, 9 or 12 for 64QAM
FORWARD ERROR CORRECTION - OUTER		
Format	BCH	
FORWARD ERROR CORRECTION – INNER		
LDPC	(7493,3048 / 4752 / 6096)	
INTERLEAVING – INNER		
Time interleaving (inter-frame): transport stream data only	Symbol-wise convolutional, branches = 52	Tm 1: depth = 240 symbols Tm 2: depth = 720 symbols
Frequency interleaving (intra-frame): transport stream data and control data	Symbol-wise block	block size = 3780
TRANSMISSION PARAMETER SIGNALING (TPS)		
TPS frequency	each OFDM frame	
TPS length	72 bits	
TPS modulation	4QAM	36 symbols
OFDM FRAME STRUCTURE		
Symbols per frame	3780	3744 (FEC) + 36 (TPS)
Frame length	666.67, 571.43, or 500 µs	For 6, 7, or 8 MHz
Sub-carrier spacing	1.5, 1.75, or 2.0 kHz	For 6, 7, or 8 MHz
Guard interval duration	420 or 945 symbols (1/9 or 1/4 of 3780)	Time = 1/9 or 1/4 of frame length
Sub-carrier modulation	4QAM, 16QAM, or 64QAM	Uniform
RF		
Channel bandwidths	6 MHz, 7 MHz, or 8 MHz	
Occupied bandwidths	5.95 MHz, 6.95 MHz, or 7.94 MHz	
Pulse shaping filter	Square Root Raised Cosine	alpha = 0.05
Transmission network	Single Frequency Network or Multiple Frequency Network	

2.4 Framing Structure

DMB-TH signals are grouped in a series of hierarchical frames. The most basic element is the **frame**. In the frame there are 3744 symbols that carry the data and 36 symbols that carry the Transmission Parameter Signaling (TPS). The TPS carries information for the demodulator to automatically adapt to the incoming transmission such as: FEC inner code rate, time interleaver length, etc.

In an 8 MHz channel, the 3780 sub-carriers are spaced at 2 kHz for a total occupied bandwidth of 7.56 MHz. In a 7 MHz channel, the 3780 sub-carriers are spaced at 1.75 kHz for a total occupied bandwidth of 6.615 MHz. And in a 6 MHz channel , the 3780 sub-carriers are spaced at 1.5 kHz for a total occupied bandwidth of 5.67 MHz.

A **signal frame** consists of a frame plus a guard interval. The guard interval length can either be the frame length divided by 9 (420 symbols) or the frame length divided by 4 (945 symbols). See section 2.7 for more on the guard interval.



	6 MHz	7 MHz	8 MHz
Frame length	666.67 µs	571.43 µs	500 µs
420 symbol (1/9) guard interval length	74.07 µs	63.49µs	55.56µs
945 symbol (1/4) guard interval length	166.67 µs	142.86 µs	125µs
Signal frame groups per second	6	7	8

A super-frame duration is exactly one minute.

An optional control frame can be added to each signal frame group. Each control frame consists of two 188 byte MPEG-2 packets with PID 0x17. The control frame is different from the rest of the signal frames in the signal frame group because it is always modulated with QPSK and FEC 0.4 without any interleaving, even if the rest of the signal frames are being sent in 16QAM or 64QAM. The control frame is always designated as frame zero.

Channel Bandwidth	6 MHz	7 MHz	8 MHz
Control frame payload	18,048 bps	21,056 bps	24,064 bps

Channel Bandwidth	Guard Interval	Control Frame	Signal Frames per Super Frame Group	Signal Frames per Minuteframe
6 MHz	420	Yes	224	224*480*6/8
		No	225	225*480*6/8
	945	Yes	199	199*480*6/8
		No	200	200*480*6/8
7 MHz	420	Yes	224	224*480*7/8
		No	225	225*480*7/8
	945	Yes	199	199*480*7/8
		No	200	200*480*7/8
8 MHz	420	Yes	224	224*480
		No	225	225*480
	945	Yes	199	199*480
		No	200	200*480

Control frame packets are proposed to indicate the time slicing between T and H modes.

Payload Data Rates

8 MHz CHANNEL BANDWIDTH						
SUB-CARRIER MODULATION	**FEC**	**GUARD INTERVAL**			**PAYLOAD RATE**	**MPEG packets per minuteframe**
		Ratio	**Symbols**	**Time**		
4QAM	0.4	1/4	945	125 µs	4,812,800 bps	
		1/9	420	55.56 µs	5,414,400 bps	
	0.6	1/4	945	125 µs	7,219,200 bps	
		1/9	420	55.56 µs	8,121,600 bps	
	0.8	1/4	945	125 µs	9,625,600 bps	
		1/9	420	55.56 µs	10,828,800 bps	
16 QAM	0.4	1/4	945	125 µs	9,625,600 bps	
		1/9	420	55.56 µs	10,828,800 bps	
	0.6	1/4	945	125 µs	14,438,400 bps	
		1/9	420	55.56 µs	16,243,200 bps	
	0.8	1/4	945	125 µs	19,251,200 bps	
		1/9	420	55.56 µs	21,657,600 bps	
64 QAM	0.4	1/4	945	125 µs	14,438,400 bps	
		1/9	420	55.56 µs	16,243,200 bps	
	0.6	1/4	945	125 µs	21,657,600 bps	
		1/9	420	55.56 µs	24,364,800 bps	
	0.8	1/4	945	125 µs	28,876,800 bps	
		1/9	420	55.56 µs	32,486,400 bps	

For 8 MHz, the exact guard interval time for a guard interval of 420 is calculated by: 0.1 / (8 * 225) which rounds to 55.56 µs. For a guard interval of 945, the equation is: 0.2 / (8 * 200) which is 125 µs exactly.

2.5 Forward Error Correction

INNER

The inner FEC depends on three quasi-cyclic LDPC codes (QC-LDPC), LDPC(7493,3048); LDPC(7493,4752); and LDPC(7493,6096) corresponding to rates 0.4, 0.6 and 0.8

OUTER

BCH(762,752) is the shortened BCH code of BCH(1023,1013). The generator polynomial is x^10+x^3+1

RANDOMIZER

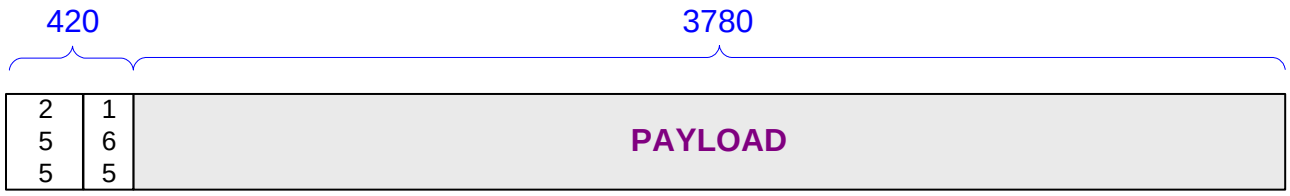
TDS-OFDM scrambles the payload with a pseudo-random binary sequence (PRBS or PN sequence) that is 32,767 symbols long (or PN-15). This is done in the modulator prior to the FEC encoding. In the demodulator, the PN-15 sequence is recovered and is used to decode the payload.

2.6 Guard Interval and PN Sequence

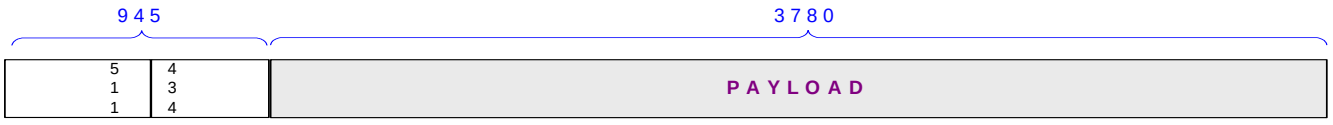
Traditionally, information on channel estimation and synchronization is mixed together with the payload but in TDS-OFDM this information is carried on a separate PN sequence and is transmitted separately in the guard interval.

A PN-9 sequence is used, which is 511 symbols long and then repeats within the frame. Each successive frame gets a new start value for the PN-9. There are two selectable guard interval lengths of 420 and 945, and the PN sequence fits into the guard intervals differently.

The 420 guard interval contains the 255 bit PN sequence followed by 165 symbols of the same PN sequence repeated.



The 945 guard interval contains the 511 bit PN sequence followed by the same PN repeated as above.



While the payload can be expressed in the frequency domain as 3780 sub-carriers spaced 1.5, 1.75 or 2 kHz apart (respectively for 6, 7, or 8 MHz channel bandwidth), the guard interval information is only relevant in the time domain. From the frequency domain perspective, the guard interval has a flat spectrum within the occupied bandwidth.

2.7 Time De-Interleaver Modes

Time interleaving and de-interleaving also increases the resilience to spurious noise, and thus improves overall system performance in noisy environments. It requires the use of an external DRAM memory on the receiver.

Symbol Depth	Max Memory (symbols)	Max Demodulator Memory (bits)	Signal Frames of Delay	GUARD INTERVAL		Time Interleave & De-Interleave Time Delay		
				Ratio	Symbols	6 MHz	7 MHz	8 MHz
240	318,240	7,637,760	170	1/4	945	141.67 ms	121.43 ms	106.25 ms
720	954,720	22,913,280	510	1/9	420	125.93ms	107.94 ms	94.44 ms
				1/4	945	425 ms	364.29 ms	318.75 ms
				1/9	420	377.78 ms	323.81 ms	283.33 ms

The delay in signal propagation caused by the symbol-wise convolutional time interleaving and de-interleaving is calculated by: B * (B-1) * M where B is the number of branches (52) and M is the depth. This delay includes the interleaving and de-interleaving times. If byte interleaving and de-interleaving is also on, then the delay values from section 2.8 must be added to the above numbers to get the total delay due to time and byte interleaving/de-interleaving.

The amount of memory required to support the de-interleaving is equal to half of the depth. At maximum interleaving depth of 720, from the above table 954,720 symbols are required in memory and thus the delay will be twice that or 1,909,440 symbols. This is then divided by 3744 symbols per frame (TPS is not interleaved) to get 510 signal frames of delay.

At its maximum time de-interleaving, the DMB-TH demodulator uses 954,720 symbols x 24 = 22,913,280 bits. External DRAM memory capable of supporting this interleaving size must be included with the demodulator ASIC if time de-interleaving is to be used. Note that if the modulator is using time interleaving, then the demodulator must use time de-interleaving. See Section 4.8 for implementing the time de-interleaving memory using external memory chips.

2.8 Automatic Parameter Detection

When put into auto-detect mode, the demodulator automatically detects the following parameters:

- Sub carrier modulation type: QPSK, 16QAM, 64QAM
- Guard interval: 420 or 945 symbols
- Control frames

When put into auto-detect from TPS mode, the demodulator automatically detects the following parameters from the TPS:

- FEC rate: 0.4, 0.6 and 0.8
- Time interleaver mode: 240 or 720 symbols

3. PIN INFORMATION

3.1 Pin Map – Top View

3.2 Pin Table

- All signal pins are 3.3V LVTTL compatible.
- All input/output (IO) and output (O) pins can drive 4 mA, unless noted otherwise below.

I^2C Interface (see Sections 4.1 & 4.2)

Pin #	Name	Type	Description
70	SCL	I	I^2C clock
71	SDA	IO	I^2C data (open drain)
66	SCLT	O	I^2C clock pass-through for tuner
67	SDAT	IO	I^2C data pass-through for tuner
24, 72, 73	CE_A2, CE_A1, CE_A0	I	I^2C address selection (3 bits)

Clocks and Resets (see Section 4.3)

Pin #	Name	Type	Description
33	XTALIN	Analog	external clock, use 60.8 XO
34	XTALOUT	Analog	Reserved for 60.8XO
28	$\overline{\text{RESET}}$	I	Hardware reset, active low

Front End & Tuner Interface (see Sections 4.4 through 4.7)

Pin #	Name	Type	Description
62	AGC	O	AGC output to tuner (PWM format)
49, 50, 51, 52, 53, 56, 57, 58, 59, 60	IF9 – IF0	I	IF input from ADC –or- I input from ADC in Baseband mode
39, 40, 41, 42, 43, 44, 45, 46, 47, 48	Q9-Q0	I	Drive to constant value in IF mode –or- Q input from ADC in baseband mode
61	IFCLK	I	IF clk @ 30.4 Mhz

Time De-Interleaver Memory Interface (see Section 4.8)
(The pin ordering is optimized to facilitate trace routing to the SDRAM)

Pin #	Name	Type	Description
84, 93, 83, 80, 79, 78, 77, 76, 87, 90, 91, 92	TI_A11 – TI_A0	O	Time de-interleaver memory address selection (12 bits, A11 is MSB)
112, 111, 110, 107, 106, 116, 117, 118, 121, 122, 123, 126, 127	TI_D12 – TI_D0	IO	Time de-interleaver memory data (13 bits, D12 is MSB)
96, 97	TI_BA1, TI_BA0	O	Time de-interleaver memory bank select
100	$\overline{\text{TI\_CS}}$	O	Time de-interleaver memory chip select (active low)
101	$\overline{\text{TI\_RAS}}$	O	Time de-interleaver memory row address strobe (active low)
86	TI_DQM	O	Time de-interleaver memory data mask
85	TI_CLK	O	Time de-interleaver memory clock
102	$\overline{\text{TI\_CAS}}$	O	Time de-interleaver memory column address strobe (active low)

105	$\overline{\text{TI\_WE}}$	O	Time de-interleaver memory write enable (active low)

MPEG Interface (see Section 4.9)

Pin #	Name	Type	Description
6, 7, 10, 11,12, 15, 16, 17	MPEG_D7 – MPEG_D0	O	MPEG data outputs (8 bits, D7 is MSB)
5	MPEG_CLK	O	MPEG clock output
4	MPEG_VALID	O	MPEG data valid signal
3	MPEG_SYNC	O	MPEG sync signal

Test Pins & Indicators (see Section 4.10)

Pin #	Name	Type	Description
128	BLKERRN	O	LDPC Block error indicator, active low
20	GPIO0	O	BCH Block error indicator, active low
25	LOCK	O	Demodulator lock signal, active high
65	IFTEST	I	Reserved, connect to DGND through 4.7 kΩ resistor
30	SM	I	Reserved, connect to DGND
115	BIST	I	Reserved, connect to DGND
29	TESTCLK	I	Reserved, connect to DGND
26, 27	BP1, BP2	I	To enable Digital clock conn, connect to VDD
21, 22	GPIO1, GPIO2	O	GPIO1 provides 30.4Mhz clk output; GPIO2 is Reserved, do not connect
23	GPIO3	I	Reserved, connect to DGND through 4.7 kΩ resistor

Power and Ground

Pin #	Name	Type	Description
8, 18, 54, 68, 81, 94, 103, 124	VDD3.3	Supply	3.3V power for digital I/O (8 pins)
1, 13, 31, 63, 74, 88, 98, 108, 119	VDD1.8	Supply	1.8V power for digital core (9 pins)
2, 9, 14, 19, 38, 55, 64, 69, 75, 82, 89, 95, 99, 104, 109, 113, 114, 120, 125	DGND	Ground	Digital ground (19 pins)
35	VCCXTAL1.8	Supply	1.8V analog oscillator supply
32	GNDXT	Ground	1.8V analog oscillator ground
36	PLLVDD1.8	Supply	1.8V analog PLL supply
37	PLLGND	Ground	1.8V analog PLL ground

4. FUNCTIONAL DESCRIPTION

4.1 I²C Interface

There are eight possible I²C slave addresses for each ASIC. Three bits of the address are selected by CE_A2, CE_A1 & CE_A0. Inside the chip, the registers are accessed in two different sections. Each section has its own I²C section address, but they share CE_A2, CE_A1 & CE_A0. The LSB of the address should be set to zero for writing and one for reading. **Section1 & Section0 are hard-coded as: 01 for Demod, & 11 for Fec.**

SECTION ADDRESS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	**0**	**CE_A2**	**CE_A1**	**CE_A0**	**Section1**	**Section0**	**R/W***

For more details on the I²C specification, please visit the Philips website: www.semiconductors.philips.com/i2c

WRITE OPERATION – SINGLE BYTE

A normal single-byte write operation using I²C control is done by:

```
I2C_Start                          'generate an I2C start condition, with clock hi make data go hi→lo
WriteByte (section_write_address)  ' write the byte "section_write_address" (LSB is zero)
GetACK                             ' check that I2C data line is pulled low, signals transfer OK
WriteByte (register_address)       ' write the byte "register_address" with the desired register
GetACK
WriteByte (write_data)             ' write the byte "write_data" with the desired data
GetACK
I2C_Stop                           'generate an I2C stop condition, with clock hi make data go lo→hi
```

READ OPERATION – SINGLE BYTE

A normal single-byte read operation using I²C control is done by:

```
I2C_Start
WriteByte (section_write_address)
GetACK
WriteByte (register_address)
GetACK
I2C_Stop

I2C_Start
WriteByte (section_read_address)   ' write the byte "section_read_address" (LSB is one)
GetACK
ReadByte (read_data)               ' read the desired data into "read_data"
I2C_Stop
```

WRITE OPERATION – MULTIPLE BYTES

Multiple bytes can be written into consecutive registers by using the following:

```
I2C_Start                       ‘ generate an I2C start condition, with clock hi make data go hi→lo
WriteByte (section_write_address)‘ write the byte “section_write_address” (LSB is zero)
GetACK                          ‘ check that I2C data line is pulled low, signals transfer OK
WriteByte (register_address)    ‘ write the byte “register_address” with the desired register
GetACK
WriteByte (write_data0)         ‘ write the byte “write_data0” with the desired data, goes into “register_address”
GetACK
WriteByte (write_data1)         ‘ write the byte “write_data1” with the desired data, goes into “register_address+1”
GetACK
WriteByte (write_data2)         ‘ write the byte “write_data2” with the desired data, goes into “register_address+2”
GetACK
I2C_Stop                        ‘ generate an I2C stop condition, with clock hi make data go lo→hi
```

Can continue as long as the register address is valid

READ OPERATION – MULTIPLE BYTES

Multiple bytes can be read from consecutive registers by using the following:

```
I2C_Start
WriteByte (section_write_address)   ‘ write the byte “section_write_address” (LSB is zero)
GetACK
WriteByte (register_address)
GetACK
I2C_Stop

I2C_Start
WriteByte (section_read_address)    ‘ write the byte “section_read_address” (LSB is one)
GetACK
ReadByte (read_data0)               ‘ read the desired data from “register_address” into “read_data0”
DoACK (0)                           ‘ send an ACK signal (pull SDA low)
ReadByte (read_data1)               ‘ read the desired data from “register_address+1” into “read_data1”
DoACK (0)
ReadByte (read_data2)               ‘ read the desired data from “register_address+2” into “read_data2”
I2C_Stop
```

Can continue as long as the register address is valid. Follow the last read with I2C_Stop.

PULL-UP RESISTORS

The SCL, SDA, SCLT, and SDAT pins should each be pulled up to 3.3V with 4.7 kΩ resistors.

4.2 Tuner I²C Interface

In order to isolate the tuner from a potentially noisy I²C bus, there are dedicated I²C lines between the demodulator and the tuner. The demodulator is connected to the main I²C bus on pins SDA and SDL. Rather than connect the main I²C bus to the tuner, the SDAT and SDLT lines should be connected between the demodulator and the tuner.

The demodulator intercepts all I^2C traffic, keeping the I^2C noise from interfering with tuner performance. To write to or read from the tuner, the register 0x01 must be set prior to issuing the I^2C command. The register must then be cleared after the communication with the tuner is complete.

Example: read the tuner lock flag from a tuner with I^2C address 0xC0:

```
I2C_Start
WriteByte (section_write_address)
GetACK
WriteByte (0x01)                    ‘ register address for the tuner I2C control
GetACK
WriteByte (0xE0)                    ‘ turn on the tuner I2C bus and specify address 0xC0 for the tuner,
                                    subsequent I2C commands are echoed on the SDAT & SCLT pins
GetACK
I2C_Stop

I2C_Start
WriteByte (0xC1)                    ‘ tuner read address
GetACK
ReadByte (locked)                   ‘ read the tuner data into “locked”
I2C_Stop

I2C_Start
WriteByte (section_write_address)
GetACK
WriteByte (0x01)
GetACK
WriteByte (0x00)                    ‘ now turn off the tuner I2C bus; SDAT & SCLT shut off
GetACK
I2C_Stop
```

4.3 Clock Management

It is recommended that a 60.8 Mhz XO be connected to the XTALIN pin. If this is used, then the BP1, BP2 , pins#26, 27 external PLL and XTAL bypass pins need to be set high.

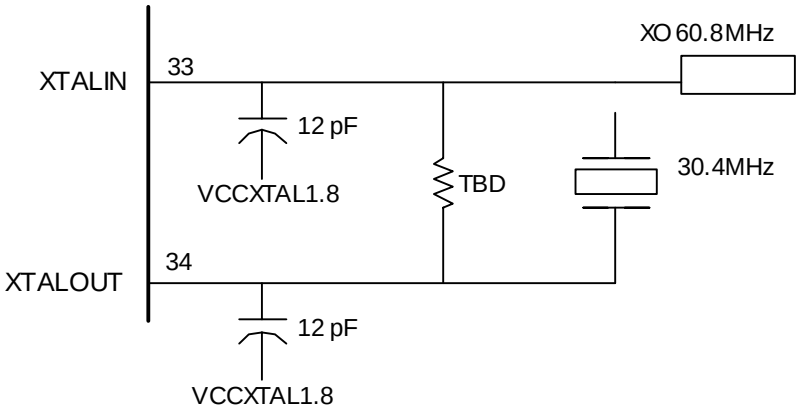
Example 60.8 XO devices are M-tron (www.mtron.com) M3H16FCD-60.800Mhz 25ppm

Improper usage of crystal with internal PLL may lead to lower performance, so use this mode after testing to see if performance is satisfied. In this mode an external parallel resonant crystal may be connected between XTALIN (pin 33) and XTALOUT (pin 34) with external 12 pF capacitors as shown, or an external clock may be forced onto the XTALIN pin. A 50 ppm or better crystal or clock source is recommended. Inside the ASIC, a 2x clock is generated for most of the digital logic. The ADC uses a 1x clock to sample the IF input. The value of the crystal depends on the desired channel bandwidth.

Channel Bandwidth	6 MHz	7 MHz	8 MHz
Crystal Fundamental Frequency	**30.4 MHz**	**30.4 MHz**	**30.4 MHz**

Surface mount 30.4 MHz fundamental parallel resonant crystals are available from:
Fox Electronics (www.foxonline.com): manufacturers part number: HC49SD 278-30.4-1 or
M-tron (www.mtron.com): manufacturer’s part number: ATSM49-30.4000MHz/12pf/fund

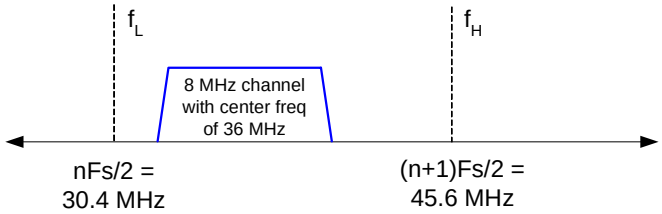
The TBD resistor is in case the oscillator has a start-up problem. The pads should be on the board in case the resistor is needed. Note the bypass caps are not to ground.



GPIO1 (pin21) provides a 30.4Mhz output clock which can be connected to the CLK pin of an external ADC

4.4 ADC

Using the IF inputs, the external 10 bit ADC samples the analog IF input at the crystal clock rate, or 30.4 MHz. Note that the input signal sampling will be non-coherent, and Nyquist's theorem applies to the bandwidth of the signal, not the highest frequency. This is why a 30.4 MHz sample rate can be used on the tuner IF signal which is typically 36 MHz. Using the universal rule for noncoherent sampling, the total energy of the signal must be contained in a continuous spectrum of width $W = (f_H - f_L)$, and a sampling frequency F_S must be chosen so that the interval f_L to f_H falls within two adjacent harmonics of $F_S/2$. With F_S = 30.4 MHz, we can see below that the entire energy of the signal must fall between 30.4 MHz and 45.6 MHz. In all cases, the resultant baseband signal will have a center frequency determined by the IF frequency minus the sampling frequency.



A tuner with a 36 MHz IF frequency will present all of its energy in the 8 MHz bandwidth from 32 MHz to 40 MHz, which falls well within the range above. The resultant baseband center frequency will be 36 MHz – 30.4 MHz = 5.6 MHz.

4.5 IF Tuner Selection

The following requirements should be observed when selecting a tuner for use with this demodulator:

- Designed for digital terrestrial applications, such as DVB-T
- VHF/UHF 75 Ω antenna input (with antenna loop through depending on the application)
- Bandwidth set to 6, 7, or 8 MHz accordingly
- Fixed IF output center frequency of 36 MHz (36.125 & 36.167 MHz also OK)
- Differential output level of 1 V peak-to-peak into 1 kΩ load

- For Can tuner: Has one or two internal SAW filters
- Maximum noise figure of 8 dB
- Has an internal RF AGC that requires no intervention, but uses an external input for the IF AGC control
- Can be controlled via I^2C
- Example tuners: Thomson DTT 7578 (vertical mount) or Thomson 7579 (horizontal mount) for 7 or 8 MHz or the Thomson DTT 7581 for 6 MHz and Analog Devices Silicon Tuners.

4.6 BB Tuner Selection

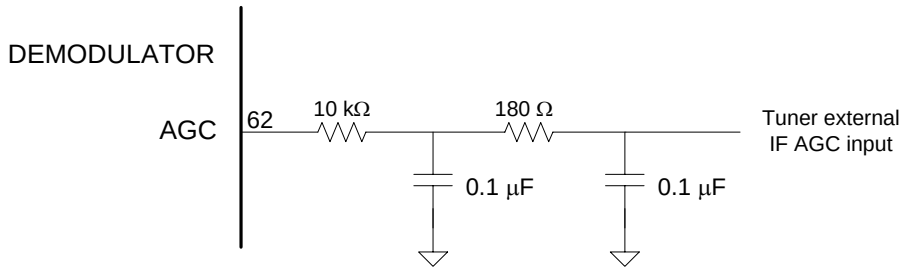
The following requirements should be observed when selecting a Baseband Silicon tuner for use with this demodulator:

- Designed for digital terrestrial applications, such as DVB-T
- Bandwidth set to 6, 7, or 8 MHz accordingly
- Differential output level of 1 V peak-to-peak into 1 kΩ load
- Maximum noise figure of 8 dB
- Has an internal RF AGC that requires no intervention, but uses an external input for the IF AGC control
- Can be controlled via I^2C
- Examples are tuners from ADI, Maxim, Freescale and Microtune

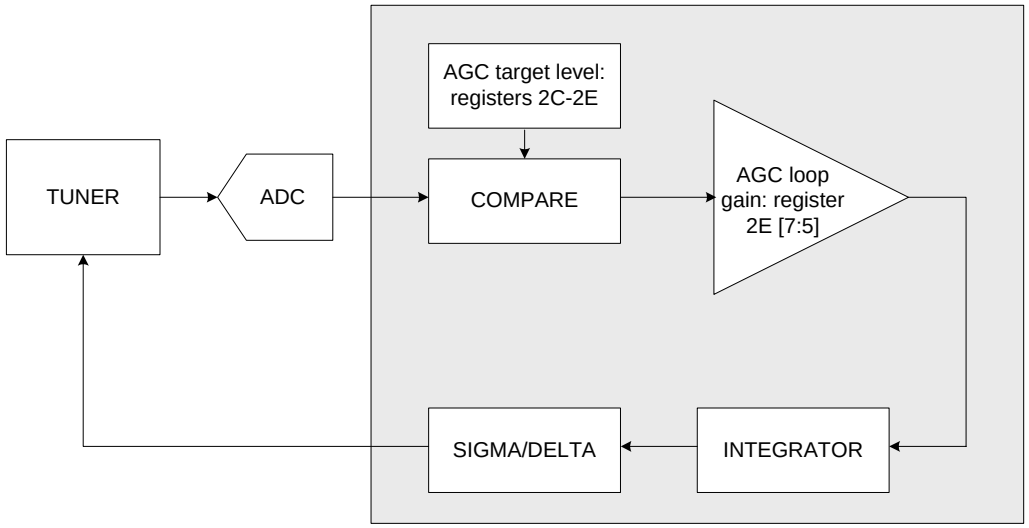
Using Baseband Silicon tuners, there is a requirement for dual 10-bit external ADC.

4.7 AGC Tuner Interface

In order to control the signal amplification from the tuner, a pulse width modulated (PWM) signal is presented on the output pin AGC (pin 62). By comparing the ADC input to a target AGC level (programmed by a set of registers), this signal increases when the demodulator determines that the tuner should provide more gain, and correspondingly decreases when the gain is too large. This pin should be connected to the AGC input of the tuner by using the following low pass filter circuit. The device does not support RFAGC, so the tuner's RFAGC needs to be controlled separately.



The following block diagram is an overview of the complete AGC circuit. See Section 5 for more detail on setting the AGC related registers.



4.8 Time De-Interleaver Memory Interface

As described in Section 2.7, at its maximum time de-interleaving the demodulator uses 954,720 symbols x 24 = 22,913,280 bits. The data is broken up into 13 bit wide words in 1,909,400 locations in order to fit into 16 bit wide commercial DRAMs. A 2M x 16 external DRAM is thus required to support time de-interleaving. The memory must be capable of running at 100 MHz (access time < 10 ns).

The 2M x 16 DRAM requirement can be satisfied using a 4M x 16 device available from the following manufacturers (less than $1.75 in volume):

- Samsung: k4s641632f-tc75/tl75: 133 MHz
- Micron: MT48LC4M16A2-7: 133 MHz

When selecting a DRAM, be sure to enquire with the manufacturer about the end-of-life because these memories change frequently.

4.9 MPEG-2 Interface

The demodulator provides a DVB common interface compliant bitstream in either parallel or serial format.

PARALLEL OUTPUT (bit 0 of register C2 is set to zero)

- The MPEG-2 transport stream data output is presented in parallel on the eight pins MPEG_D7 (MSB) to MPEG_D0 (LSB).
- The MPEG_SYNC pin goes high during the first byte of each packet (0x47), and low otherwise.
- The MPEG_VALID pin is high only when the data is valid, and low otherwise.
- The MPEG_CLK pin presents the clock that should be used to latch the parallel data. The polarity of this signal can be switched by toggling bit 0 of register C2. By default, MPEG_CLK is gated with the MPEG_VALID signal internally so it shuts off when the data is not valid. This ensures compatibility in receiver designs that do not use the MPEG_VALID signal. It can be changed to a free running clock by setting bit 2 of register CE to one.

SERIAL OUTPUT (bit 0 of register C2 is set to one)

- The MPEG-2 transport stream data output is presented serially on MPEG_D7, MSB first.
- The MPEG_SYNC pin goes high during the first bit of the first byte of each packet (0x47), and low otherwise.

- The MPEG_VALID pin is high only when the data is valid, and low otherwise.
- The MPEG_CLK pin presents the clock that should be used to shift and latch the serial data. The polarity of this signal can be switched by toggling bit 0 of register C2. By default, MPEG_CLK is gated with the MPEG_VALID signal internally so it shuts off when the data is not valid. This ensures compatibility in receiver designs that do not use the MPEG_VALID signal. It can be changed to a free running clock by setting bit 2 of register CE to one.

The following is a mapping of the MPEG-2 output pins to the DVB Common Interface (DVB-CI) specification:

LGS-8913-XX PIN NAME	DVB-CI PIN NAME
MPEG_D7 to MPEG_D0	MDI [7:0]
MPEG_SYNC	MISTRT
MPEG_VALID	MIVAL
MPEG_CLK	MCLKI

Use the following table to connect the MPEG-2 parallel output of the LGS-8913-xx to the STMicroelectronics STi5514, STi5516, or STi5517 MPEG-2 decoders. For serial mode, only connect data bit 7 (MSB).

LGS-8913-XX PIN NAME	STi5514/6/7 PIN NAME
MPEG_D7 to MPEG_D0	TSINxDATA [7:0]
MPEG_SYNC	TSINxPACKETCLK
MPEG_VALID	TSINxBYTECLKVALID
MPEG_CLK	TSINxBYTECLK

Use the following table to connect the MPEG-2 parallel output of the LGS-8913-xx to the STMicroelectronics STi5518 MPEG-2 decoder.

LGS-8913-XX PIN NAME	STi5518 BVx /CVx (parallel) PIN NAME (NUMBER)
MPEG_D7 to MPEG_D0	PIO3 [7:0] (13:6)
MPEG_SYNC	FEC_ERROR (19)
MPEG_VALID	FEC_P_CLK (18)
MPEG_CLK	FEC_B_CLK (17)

For serial mode, only connect data bit 7 (MSB).

LGS-8913-XX PIN NAME	STi5518 Serial PIN NAME (NUMBER)
MPEG_D7 (MSB)	FEC_DATA (16)
MPEG_SYNC	FEC_ERROR (19)
MPEG_VALID	FEC_P_CLK (18)
MPEG_CLK	FEC_B_CLK (17)

PACKET ERROR INDICATION

The demodulator inserts the transport_error_indicator in the MPEG-2 transport stream header (bit 9 of the transport packet header, right after the sync byte) if the packet is bad (has uncorrectable errors).

4.10 Indicators

The following indicator signals are available on pins:

INDICATOR NAME	PIN NUMBER	LOGIC	DESCRIPTION
$\overline{\text{BLKERR}}$	128	Active low	Block error: low if uncorrectable LDPC errors are present
GPIO0	20	Active low	BCH error: low if uncorrectable bit BCH errors are present
LOCK	25	Active high	Demodulator lock: High if locked

The LOCK pin indicates that the demodulator has locked onto a signal, but to ensure a valid signal the $\overline{\text{BLKERR}}$ pin should be off. The GPIO0 pin indicates that there are errors in the signal that the forward error correction is fixing. The threshold of visibility (when the video signal will start to show artifacts) is reached at a bit error rate of approximately 3E-6. This can be estimated by seeing the GPIO0 light constantly on, but seeing the $\overline{\text{BLKERR}}$ light off or flickering ever so slightly.

The actual number of bit and byte errors can be read from the registers. See the descriptions for registers 0xD0 to 0xDB in section 5 for more detail. These registers can be used to get an approximation of the bit error rate during operation (true bit error rate requires a pseudo-random sequence to be transmitted).

4.11 Power-Up Sequence

The device should be powered-up according to the following sequence:

1) Bring up the 1.8V and 3.3V power supplies.

2) Perform a hard reset. An active low pulse should be applied to $\overline{\text{RESET}}$ (pin 28) for at least 500 µs while the clock is stable and free running.

3) Perform a soft reset. Register 0x02 bit [0] should be set to zero via I^2C control for at least 10 µs and then reset back to one.

4) Wait for demodulator to settle.

5. REGISTER DESCRIPTIONS

The following registers are accessible via the I^{2}C interface as described in Section 4.1. Each register has a:

- Section address: The ASIC is divided into two sections. Each register falls into one of these sections, as indicated in the register detail below.
- Register address: After sending the section address, the register address within that section is specified. All register addresses are unique.

The term **NC** means that the bits are not connected and thus should be ignored when reading from the register. When writing a register with **NC** bits, write zero into those bits.

The term **RES** means that the bits are reserved for future use and thus ignored when reading and should be preserved when writing to the register. When writing a register with **RES** bits, retain the read back values into those bits.

The power up & reset mode of the ASIC is currently:

- **64QAM, FEC=0.6, guard interval=420, constant PN=on, time de-interleaver=off, output=parallel**

Once auto-detect mode is debugged & verified, the power-up and reset mode will change to:

- **Auto-detect on (sub-carrier, FEC type & rate, guard interval, time de-interleaver), output=parallel**

Demod REGISTERS: 0x00 to 0xBF: Section Write Address: 0x02, Section Read Address: 0x03

VERSION NUMBER								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	**VERSION_NUM [7:0]**							

Register address: **0x00**
Type: **Read Only**
Reset value: **0x0B**
Description: **VERSION_NUM [7:0]:** Contains the version number of the chip.

TUNER I2C CONTROL								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	**TUN_I2C_EN**	**TUN_I2C_ADDR [6:0]**						

Register address: **0x01**
Type: **Read/Write**
Reset value: **0x60**
Description: **[7] TUN_I2C_EN:**

0	Tuner I^{2}C echo is off (default)
1	Tuner I^{2}C echo is on (send I^{2}C commands to SDAT, SCLT)

[6:0] TUN_I2C_ADDR: Contains the seven MSBs of the tuner I^{2}C address (usually 0xC0)

SOFT RESET								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**SRST**

Register address: **0x02**
Type: **Read/Write**
Reset value: **0x01**
Description: **[0] SRST:** 0 Perform soft reset
1 Do not perform soft reset (default)

AUTO DET GI								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**AD_GI**

Register address: **0x03**
Type: **Read/Write**
Reset value: **0x01**
Description: **[0] AD_GI:** 0 No GI Auto-detection
1 Enable GI Auto-detection (default)
Refer to Application note on how to use Auto-detection of GI.

GI_SEL								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	**NC**		**NC**	**NC**	**NC**	**NC**	**GI_SEL**	**GI_SEL**

Register address: **0x04**
Type: **Read/Write**
Reset value: **0x00**
Description: Guard Interval selection

[1:0] GI_SEL: 00 Set guard interval to 420, if auto-detect is off (default)
10 Set guard interval to 945, if auto-detect is off

CH B/W								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	**CH_BW**		**NC**	**NC**	**NC**	**NC**	**NC**	**NC**

Register address: **0x06**
Type: **Read/Write**
Reset value: **0x00**
Description:

[7:6] CB [1:0]: 00 8 MHz channel bandwidth (default)
01 7 MHz channel bandwidth
10 6 MHz channel bandwidth

IF CONFIG								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	**EXT_ADC**	**NC**	**NC**	**1**	**BB_SEL**	**IF_SEL**	**IF_SIGN**	**1**

Register address: **0x07**
Type: **Read/Write**
Reset value: **0x93**
Description:

[7] EXT_ADC: 0 Internal pipelined ADC used (default)
1 External pipelined ADC used

[3] BB_SEL: 0 IF (default)
1 Baseband, requires I/Q inputs to be driven

[2] IF_SEL: 0 Spectrum inversion (default)
1 No spectrum inversion

[1] IF_SIGN: 0 output straight binary (use with internal ADC) (default)
1 output two's-complement

AFC								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	**NC**	**NC**	**RES**		**AFC_CFE**	**RES**	**RES**	

Register address: **0x08**
Type: **Read/Write**
Reset value: **0x1C**
Description: Automatic Frequency Control. Coarse Frequency Estimation

[3] AFC_CFE: 0 AFC CFE disabled (default)
1 AFC CFE enabled

INITIAL IF FREQUENCY								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	**AFC_PHASE_INIT [7:0]**							
0x0A	**AFC_ PHASE _INIT [15:8]**							
0x0B	**AFC_ PHASE _INIT [23:16]**							
0x0C	**AFC_ PHASE _INIT [31:24]**							

Register addresses: **0x09, 0x0A, 0x0B, 0x0C**
Type: **Read/Write**
Reset values: **0xCB, 0x6B, 0x28, 0x2F**
Description: **AFC_ PHASE _INIT [31:0]:** This 32 bit number, spread over four registers, sets the initial IF frequency of the automatic frequency control. This is determined by taking the tuner IF output frequency and subtracting the IF clock frequency. The default is 5.6 MHz.

Formula (1): **AFC_ PHASE _INIT** = Initial IF frequency (in MHz) * 2^32 / IF_CLK (in MHz)

Formula (2): Initial IF frequency (in MHz) = **AFC_ PHASE _INIT** * IF_CLK (in MHz) / 2^32

Example: A tuner with an output frequency of 36 MHz is used, and the IF_CLK for 8 MHz is the standard 30.4 MHz. The desired initial IF frequency value is 36 MHz – 30.4 MHz = 5.6 MHz. To calculate the proper value for the registers, use formula (1):

AFC_ PHASE _INIT = 5.6 * 2^32 / 30.4, which reduces to 791,178,186. Converting this number to hexadecimal gives us the values for the registers.

For 8 MHz with a 36 MHz output tuner, use **0xCB, 0x6B, 0x28, 0x2F**. For 7 MHz with a 36 MHz output tuner, use **0x9D, 0x56, 0x77, 0x5A**.

AGC TARGET LEVEL								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2C	**AGC_REF [7:0]**							
0x2D	**AGC_REF [15:8]**							
0x2E	**1**	**0**	**1**	**AGC_REF [20:16]**				

Register addresses: **0x2C, 0x2D, 0x2E**
Type: **Read/Write**
Reset values: **0x00, 0x00, 0xA2**
Description: **AGC_REF [20:0]:** This 21 bit number, spread over three registers, sets the AGC voltage threshold for the tuner. The default is 6.25% of full scale. This value is dependent on the tuner being used. To determine the value for any given tuner, provide the tuner with a low power RF signal that approximates the tuner's input sensitivity specification. While the demodulator stays locked, monitor the AGC pin on the tuner with a voltmeter and adjust the **AGC_REF** registers so that the AGC pin voltage is somewhere between 0V and 3.3V. The AGC is ensured to be in proper operation if the voltage on the AGC pin is in between the rails and not held all the way high or low. Then repeat this for the high end of the tuner's input sensitivity, applying a very strong RF signal, and see if any changes are needed to the **AGC_REF** registers to allow the desired sensitivity range. Note for a strong input signal the AGC voltage will likely be zero volts as the AGC only kicks in when it needs the tuner to apply some gain.

Formula (1): AGC value as a percentage of full scale = **AGC_REF** / 2^21

Note: The AGC adjustment is done automatically and the input signal strength is not displayed in current devices.

AFC PHASE								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x45	**AFC_PHASE [7:0]**							
0x46	**AFC_PHASE [15:8]**							
0x47	**AFC_PHASE [23:16]**							
0x48	**AFC_PHASE [31:17]**							

Register address: **0x45, 0x46, 0x47, 0x48**
Type: **Read Only**
Reset value: **0xAD,0x43,0x2B,0x2F**

Description: **AFC_PHASE [31:0]:** These registers return the numerically controlled oscillator (NCO) phase. The difference between the ideal tuner IF frequency and the resultant tuner IF frequency can be calculated using these registers. See registers 0x09 to 0x0C for more detail on the initial AFC frequency (example, for a tuner with a 36 MHz IF frequency, subtract the 30.4 MHz sample frequency to get the initial AFC frequency of 5.6 MHz).

Formula (1): AFC_FREQ = **AFC_PHASE * sample_freq** / 2^32, where sample_freq = 30.4 MHz

Example: If AFC_PHASE = 792011293, AFC_FREQ = 792011293 * 30.4E6 / 2^32 = 5.60589677 MHz. So the actual IF frequency is off by 5.89677 kHz.

CA LOCK								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4B	**CA_LOCK**	**RES**	**NC**	**RES[4:0]**				

Register addresses: **0x4B**
Type: **Read Only**
Reset values: **0x03**
Description: **CA_LOCK**

[7] CA_LOCK:
0 Code acquisition not locked
1 Code acquisition locked. This signal also appears on pin 25 (LOCK) as active-high.

PN945_ADJUST								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x73								

Register addresses: **0x73**
Type: **Read/Write**
Reset values: **0x0C**
Description:
For PN945, change the value to 0x3A.

TPS								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x7C	**SC**	**NC**	**NC**		**RES**	**RES**	**ITER**	**PNC**

Register address: **0x7C**
Type: **Read/Write**
Reset value: **0x03**
Description:

[7] SC: 0 modulator is not transmitting single carrier (default) i.e Multicarrier mode
1 modulator is transmitting single carrier

[1]ITER: 0 iteration OFF
1 iteration ON (default)

[0] PNC: 0 ph noise comp off
1 ph noise comp on (default)

MANUAL DEMOD OPCON								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x7D	**CTL_FRM**	**RES[1:0]**		**MODE[2:0]**			**RATE[1:0]**	

Register address: **0x7D**
Type: **Read/Write**
Reset value: **0x71**
Description: Demod Operating condition. IF AUTO DETECT OFF (0x7E)

[7] CTL FRM : 1 Control Frame Enable

[6:5] RESERVED [1:0]:

[4:2] MODE [2:0]: 000 set for 4QAM, if auto-detect is off
010 set for 16QAM, if auto-detect is off
100 set for 64QAM, if auto-detect is off (default)

[1:0] RATE [1:0]: 00 set for 0.4, if auto-detect is off
01 set for 0.6, if auto-detect is off (default)
10 set for 0.8, if auto-detect is off

AUTO_DET								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x7E	**NC[6:0]**							**AD[0:0]**

Register address: **0x7E**
Type: **Read/Write**
Reset value: **0x01**
Description: AutoDetect Enable

[0] AD : 1 Auto-detection Enable (For FEC-mode, FEC-rate, and FEC time de-interleaver)
0 Manual detection

SIGNAL STRENGTH BIN ADDRESS								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x83	**SS_BIN_ADDR [7:0]**							
0x84	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**SS_BIN_ADDR [9:8]**	

Register address: **0x83, 0x84**
Reset values: **0x00, 0x00**
Type: **Read/Write**
Description: This 10 bit number, spread over two registers, is the address for the signal strength bin. Use with register 0x94 to read the signal strength for SFN alignment. For guard interval of 420, the address range is 0 to 419. For guard interval of 945, the address range is 0 to 944.

SIGNAL STRENGTH								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x94	**SIGNAL_STRENGTH [7:0]**							

Register address: **0x94**
Type: **Read Only**
Reset value: **0x00**
Description: This register contains the signal strength for the bin number set by registers 0x83 and 0x84.

AVG NOISE MAG								
		Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x95	**AVE NOISE MAG [7:0]**							

Register address: **0x95**
Type: **Read/Wr**
Reset value: **0x1E**
Description: Each sub-carrier (after equalization) goes through a slicer, the difference between the input and output of the slicer can tell how noisey the channel is. Reg_0x95 is the average of these differences for all sub-carriers.

Recommended values for good signal quality QPSK = 0x02h; 16QAM = 0x10h; 64QAM = 0x20h

AUTO DET RESULT								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xA2	**CTL_FRM**	**RES**	**TIM_SGN**	**MODE[2:0]**			**RATE[1:0]**	

Register address: **0xA2**
Type: **Read Only**
Reset value: **0x00**
Description: This register contains the results of auto-detection. The TIM_SGN displayed result is the XOR of the QPSK MAP in register 0xC6 and the actual results.

[7] CTL FRM : 1 Control Frame Detected

[5] TIM_SGN : 0 China DTV mode time de-interleaver: B = 52, M = 720 (default), Auto detect mode
1 China DTV mode time de-interleaver: B = 52, M = 240

[4:2] MODE [2:0]:
000 4QAM
010 16QAM
100 64QAM

[1:0] RATE [1:0]:
00 rate 0.4
01 rate 0.6
10 rate 0.8

AUTO DECTECT STATUS								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xA4	**NC**	**NC**	**NC**	**NC**	**F_CF**	**DONE_CF**	**F_AUTO**	**DONE_AUT**

Register address: **0xA4**
Type: **Read Only**
Reset value: **0x05**
Description:

[3] F_CF: 0 Control frame auto-detect passed
1 Control frame auto-detect failed

[2] DONE_CF: 0 Control frame auto-detect not done
1 Control frame auto-detect done

[1] F_AUTO: 0 Sub-carrier, etc auto-detect did not fail
1 Sub-carrier,etc auto-detect failed

[0] DONE_AUTO:
0 Auto-detect for sub-carrier, etc in progress
1 Auto-detect for sub-carrier, etc complete

FEC REGISTERS: 0xC0 to 0xFF: Section Write Address: 0x06, Section Read Address: 0x07

FEC MANUAL OPCON								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC0	**NC**	**TIM**	**TIM**	**SC**	**SC**	**SC**	**RATE**	**RATE**

Register address: **0xC0**
Type: **Read/Write**
Reset value: **0x11**
Description: FEC operating condition if FEC Auto detection is turned off 0xC1[0].

[6:5] TIM [1:0]: 10 set time de-interleaver: B = 52, M =240, delay = 636,480 symbols, memory =318,240 symbols, if auto-detect is off
11 set time de-interleaver: B = 52, M = 720, delay = 1,909,440 symbols, memory = 954,720 symbols, if auto-detect is off

Time de-interleaver setting:

0xC0[6:5]	Combined Setting	Time De-interleaver
10	0xA2[5] ^ 0xC6[0] = 0	240
11	0xA2[5] ^ 0xC6[0] = 1	720

[4:2] FEC_MODE [2:0]: 000 FEC set for 4QAM, if auto-detect is off
010 FEC set for 16QAM, if auto-detect is off
100 FEC set for 64QAM, if auto-detect is off (default)

[1:0] FEC_RATE [1:0]: 00 FEC set for 0.4, if auto-detect is off
01 FEC set for 0.6, if auto-detect is off (default)
10 FEC set for 0.8, if auto-detect is off

FEC AUTO / MANUAL								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC1	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**FEC_AD**

Register address: **0xC1**
Type: **Read/Write**
Reset value: **0x01**
Description:

[0] FEC_AD
0 FEC sub-carrier, FEC rate, time de-interleaver settings manual
1 FEC sub-carrier, FEC rate, time de-interleaver settings come from Demod (default)

MISC								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC2	**RES**	**RES**	**RES**	**RES**	**RES**	**MPEGCLK**	**MCLKPOL**	**SERIAL**

Register address: **0xC2**
Type: **Read/Write**
Reset value: **0x0A**
Description:

[2] MPEGCLK:	0	MPEG_CLK is internally gated by MPEG_VALID (default)
	1	MPEG_CLK is free running
[1] MCLKPOL:	0	MPEG output clock (pin 2) normal
	1	MPEG output clock (pin 2) inverted (default) (for parallel video)
[0] SERIAL:	0	Parallel output of MPEG-2 data enabled (default)
	1	Serial output of MPEG-2 data enabled (on D7 the MSB)

CONTROL FRAMES								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC3	**NC**		**NC**	**BER**	**NC**	**NC**	**NC**	**CF_DEC**

Register address: **0xC3**
Type: **Read/Write**
Reset value: **0x01**
Description:

[0] CF_DEC:	0	Control frames ignored(default)
	1	Control frames decoded
[4] BER:	0	Normal operation(default)
	1	Set to enable PN-23 test using BER

FEC SELF RESET								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC5	**RES[4:0]**			**FEC_RST[4:0]**				

Register address: **0xC5**
Type: **Read/Write**
Reset value: **0x06**
Description:

[2:1] FEC_RST[1:0]:	00000	FEC self reset is never activated.
	00110	(default) FEC self reset activated.

PACKET COUNTER CONTROL								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC6	**PKTRUN**	**PKTCLR**	**NC**		**RES**	**RES**	**RES**	**QPSK_MAP**

Register address: **0xC6**
Type: **Read/Write**
Reset value: **0x00.** **Needs to be programmed to 0x01 for China DTV standard compatibility.**
Description:

[7] PKTRUN: 0 Packet and error counters are running and can be cleared (default)
1 Packet and error counters are stopped and can be read but not cleared

[6] PKTCLR: 0 Packet and error counters normal (default)
1 Packet and error counters cleared

[0] QPSK_MAP: 0 QPSK symbol to LDPC is not inverted (default)
1 QPSK symbol to LDPC is inverted
For China DTV standard compatibility, program this bit to '1'.

LDPC PARTIAL ITER								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC8	**NC**	**ITER**	**NC**	**RES**	**RES**	**RES**	**RES**	**RES**

Register address: **0xC8**
Type: **Read/Write**
Reset value: **0xE2**
Description: Enable Partial Iteration mode for lower power operation. Use if required.

[6] ITER: 1 Full iteration
0 Partial iteration

TOTAL LDPC PACKET COUNT								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xD0	**LDPC_TPACK [7:0]**							
0xD1	**LDPC_TPACK [15:8]**							
0xD2	**LDPC_TPACK [23:16]**							
0xD3	**LDPC_TPACK [31:24]**							

Register addresses: **0xD0, 0xD1, 0xD2, 0xD3**
Type: **Read Only**
Reset values: **0x00, 0x00, 0x00, 0x00**
Description: **LDPC_TPACK [31:0]:** This 32 bit number, spread over four registers, is the total number of LDPC packets that passed through the demodulator since the last packet counter clear (see register 0xC6).

TOTAL LDPC PACKET ERROR COUNT								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xD4	**LDPC_EPACK [7:0]**							
0xD5	**LDPC_EPACK [15:8]**							
0xD6	**LDPC_EPACK [23:16]**							
0xD7	**LDPC_EPACK [31:24]**							

Register addresses: **0xD4, 0xD5, 0xD6, 0xD7**
Type: **Read Only**
Reset values: **0x00, 0x00, 0x00, 0x00**
Description: **LDPC_EPACK [31:0]:** This 32 bit number, spread over four registers, is the total number of LDPC error packets that passed through the demodulator since the last packet counter clear (see register 0xC6).

The **LDPC_TPACK** and **LDPC_EPACK** registers can be used to approximate the uncorrected bit error rate coming out of the ASIC. Since both registers are in packets, instead of bits, the ratio **LDPC_EPACK/ LDPC_TPACK** doesn't reflect true bit error rate and an adjustment factor needs to be applied. While performing lab testing with a hardware bit error rate tester (BERT) and using a pseudo random 2^23 (PN23) input, we've empirically found that multiplying the ratio by an adjustment of 0.01 closely approximates the results of the BERT.

To perform this in software, execute the following by modifying the packet counter start, stop, and clear controls in register 0xC6:

- Start the packet counters (set 0xC6 bit 7 to zero)
- Clear the packet counters (set 0xC6 bit 5 to one)
- Remove the clear signal (set 0xC6 bit 5 to zero)
- Wait for the desired period of time, being careful not to overflow (<=30 seconds for 64QAM, <=135 seconds for 4QAM)
- Stop the packet counters (set 0xC6 bit 7 to one)
- Read all **LDPC_TPACK** and **LDPC_EPACK** registers

Bit error rate = 0.01 * **LDPC_EPACK / LDPC_TPACK** (this represents the approximate average BER over the time period that was waited)

6. REGISTER SETTINGS & APPLICATION INFORMATION

Procedure switching auto-detection to manual:

(1) set 0xC5[2:1] ← "2'b00"
(2) set 0xC6[0] ← "1"
(3) read until 0xA4[0] = "1" - - auto detection is done
(4) read 0xA2[4:0], then write its valueto 0xC0[4:0]
read 0xA2[5]:
if "0", then write 0xC0[6:5] ← "2'b11"
if "1", then write 0xC0[6:5] ← "2'b10"
(5) set 0xC1[0] ← "0"
(6) set 0xC5[2:1] ← "2'b11"

LGS-8913 support for China DTV standard

Working with a default DMB-TH transmitter no changes are required, but to work with a China DTV standard transmitter, minor changes are required through firmware

1) Change QPSK symbol polarity to inverted, Write register 0xC6[0] with '1'.

Auto-detection of Guard Intreval (PN)

DMB-TH protocol defines 2 possible Guard Interval setting for the protocol, PN420 and PN945.

Kona family of devices (LGS-8913) have the provision of manually setting the required Guard Interval to prevent the receiver to quickly locking and settling in a low signal quality environment. This is the recommended approach.

However, Legend Silicon demodulator's provide the option for automatic detection of Guard Interval by the receiver where software intervention is not required. This is only recommended for a high signal quality environment.

To enable this feature, the following 3 registers are required

AUTO DETECT GI	0x03
AUTO DETECT GI SEARCH TIME	0x3C
AUTO DETECT GI RESULT	0x44

PN AUTO SEARCH TIME								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3C								

Register address: **0x3C**
Type: **Read/Write**
Reset value: **0x20**
Description: Search Time for PN Auto detection (in Frame Length intervals * 16). Change to 0xE0 to extend the search time in low signal quality environments

PN AUTO RESULT								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x44								**GI_AD_RES**

Register address: **0x44**
Type: **Read Only**
Description: Results of PN Auto detection

[0] GI_AD_RES [0]: 0 indicates PN420

1 indicates PN945

6.1 Switching to Manual Mode after Auto-Detect is Complete

The ASIC auto-detects four TDS-OFDM parameters: guard interval, sub carrier modulator, forward error correction rate, and time de-interleaving. Once auto-detect has been completed, there are two options:

1. Leave auto-detect on. This does not cause any performance degradation, but if a large amount of interference is present then the auto-detect algorithm might temporarily lose one or more of the four parameters. The parameters would return to their proper settings after the interference is removed, but a visible interruption in the MPEG-2 transport stream could occur.

2. Once the parameters have been detected, set them so they can't be changed and turn off auto-detect. This is the preferred method, as the ASIC will not try to automatically change parameters in the presence of high amounts of interference. This could be done during the first channel change or EPG activation after power-up.

Switching off auto-detect is a three-step process. First the registers that contain the status of the four auto-detected parameters should be read. Then the registers that control the manual settings of the four parameters should be set accordingly. Finally, auto-detect is turned off and the manual settings take effect.

The following register reads and writes can be used to take the ASIC from auto-detect mode to manual-detect mode.

```
//Check the status of the demodulator: CA Locked, AFC Locked and that auto-detect has done ***

// Read the status of the four auto-detect parameters: sub carrier modulator (sc),
        forward error correction (fec) rate, and time de-interleaving (tdl) ***
// Compute the values to be programmed in manual mode
        // Set the sub-carrier ***
        // Set the forward error correction rate***
        // Set the time de-interleaver,
        // Set the control frame,


// Turn off auto-detect, manual settings take effect ***
        WriteReg(Auto Detect Enable, off);

        // Done ***
```

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Parameter	Description	Value
$VDD_{3..3}$	Max 3.3V power supply voltage	3.5V
VDD1.8	Max 1.8V power supply voltage	1.9V
V_I	Min/Max voltage on input pins	-0.5V to $VDD_{3.3}$ + 0.5V
V_O	Min/Max voltage on output pins	-0.5V to $VDD_{3.3}$ + 0.5V

7.2 Thermal Data

NO EXPOSED PAD (Engineering samples LGS-8913-B1 estimated)

Parameter	Description	Value
T_{stg}	Min/Max storage temperature	-40°C to 150°C
R_{thjaNP}	Junction-ambient thermal resistance	34.2 °C/W: two layer PCB 30.3 °C/W: four layer PCB
$T_{oper2NP}$	Min/Max operating ambient temperature, two layer PCB, no air flow	-10°C to 45°C
$T_{oper4NP}$	Min/Max operating ambient temperature, four layer PCB, no air flow	-10°C to 52°C

7.3 DC Electrical Characteristics

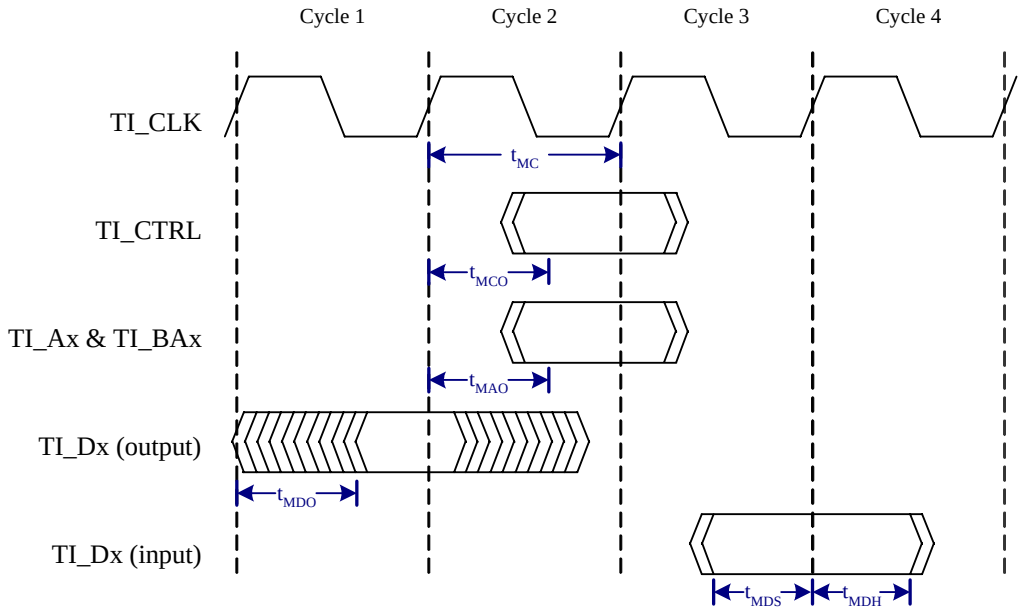
$VDD_{3.3}$ = 3.3V, VDD1.8 = 1.8V, and an ambient temperature of 25°C unless otherwise specified.

Operational power is dependent on Mode and rate settings. It is recommended to use Partial iteration mode to save power.

Parameter	Description	Test Conditions	Min	Typical	Max	Unit
$VDD_{3.3}$	I/O operating voltage		3.1	3.3	3.5	V
VDD1.8	Core operating voltage		1.7	1.8	1.9	V
$I_{DD3.3}$	I/O power supply current	Demodulator operating		33		mA
$I_{DD1.8}$	Core power supply current	Demodulator operating		0.4		A
P_{OPER}	Power consumption, operation	Demodulator operating		800		mW
P_{STBY}	Power consumption, standby mode	Demodulator **not** operating		200		mW
V_{IL} V_{IH}	Low level input voltage High level input voltage		 2.0		0.8	V V
V_{OL} V_{OH}	Low level output voltage High level output voltage		 3.0		0.4	V V

7.4 SDRAM Interface Timing Characteristics

The synchronous DRAM interface is designed to work with industry standard SDRAM components per the following timing diagram.



Note: TI_CTRL = $\overline{\text{TI\_RAS}}$, $\overline{\text{TI\_CAS}}$, $\overline{\text{TI\_WE}}$, $\overline{\text{TI\_CS}}$, & TI_DQM

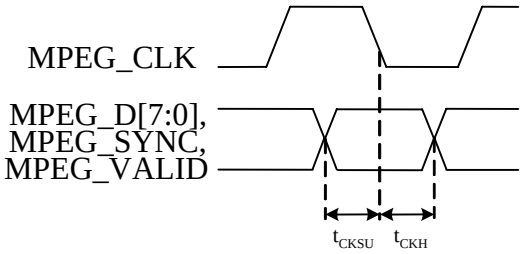
Parameter	Description	Min	Typical	Max	Unit
t_{MC}	Cycle Time		16.4		ns
t_{MCO}	Control signal output	3	7	11	ns
t_{MAO}	Address output	3	7	11	ns
t_{MDS}	Data setup	8			ns
t_{MDH}	Data hold	1			ns
t_{MDO}	Data output	3	7	11	ns

7.5 MPEG Interface Timing Characteristics

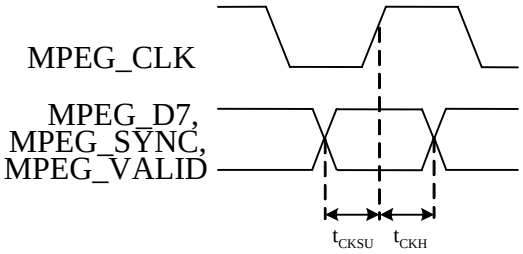
The MPEG output is designed to be compatible with the DVB standards.

Parameter	Description	Min	Typical	Max	Unit
f_{CLK}	Core operating clock frequency:				
	8 MHz channel bandwidth, using 60.8 MHz XTAL		60.8		MHz
	7 MHz channel bandwidth		53.2		MHz
	6 MHz channel bandwidth		45.6		MHz
t_{CLK}	Core operating clock period (1/ f_{CLK})				
	8 MHz channel bandwidth		16.4		ns
	7 MHz channel bandwidth		18.8		ns
	6 MHz channel bandwidth		21.9		ns
$t_{MPEGCLK}$	MPEG_CLK duty cycle	40	50	60	%
Parallel output timing: register 0xC2 bit [0] = 0					
t_{CKS}	MPEG_D[7:0], MPEG_SYNC, MPEG_VALID stable before MPEG_CLK falling edge	2* t_{CLK}			ns
t_{CKH}	MPEG_D[7:0], MPEG_SYNC, MPEG_VALID stable after MPEG_CLK falling edge	2* t_{CLK}			ns
Serial output timing: register 0xC2 bit [0] = 1					
t_{CKS}	MPEG_D7, MPEG_SYNC, MPEG_VALID stable before MPEG_CLK rising edge	2			ns
t_{CKH}	MPEG_D[7:0], MPEG_SYNC, MPEG_VALID stable after MPEG_CLK rising edge	3			ns

PARALLEL OUTPUT TIMING



SERIAL OUTPUT TIMING



7.6 I²C Interface Characteristics

The ASIC supports the normal I²C operation in Fast-mode (up to 400 kbps). See Section 4.1 for more details on I²C programming.

The following table applies to pins SCL, SDA, SCLT, & SDAT.

Parameter	Description	Test Conditions	Min	Typical	Max	Unit
V_{IL} V_{IH}	Low level input voltage High level input voltage	10 kΩ pull-up to 3.3V	-0.5 2.0		0.8 3.6	V
V_{OL} V_{OH}	Low level output voltage High level output voltage	10 kΩ pull-up to 3.3V			0.4 3.6	V
I_{LK}	Input leakage current	V_{IN} = 0V to 3.3V	-10		10	µA
I_{OL}	Output sink current	V_{OL} = 0.5V		10		mA
Fast Mode						
f_{SCL} t_{SCL}	SCL clock frequency SCL clock period	Fast Mode Fast Mode	 2.5		400	kHz µs
t_{BUF}	Bus free time required between a STOP and START condition			1.3		µs
t_{STO}	Setup time for STOP condition			600		ns
t_{DAT}	Setup time for data			100		ns
$t_{R,}$ t_F	Rise and fall times				300	ns

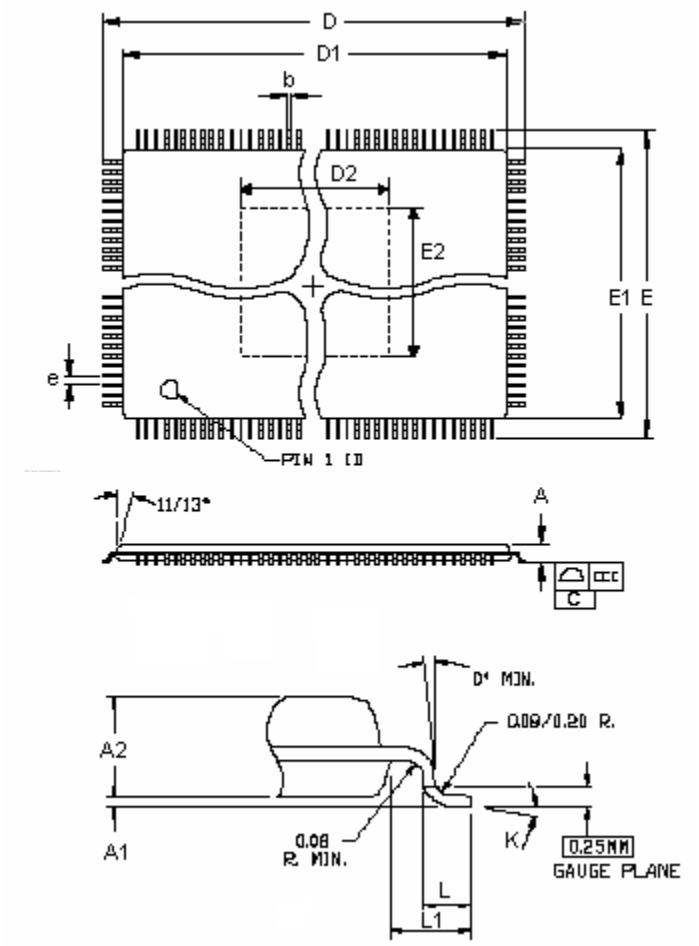
8. PACKAGE MECHANICAL DATA

The ASIC is housed in a 128 pin LQFP with dimensions of 20mm x 14mm x 1.4mm. With the pins included, the total dimensions become 22mm x 16mm x 1.6mm. There is an exposed pad underneath the chip with dimensions 9.8 mm x 9.8 mm. When the exposed pad is soldered to a matching square pad on the circuit board (connected to the digital ground plane of the board), the thermal performance is improved per Section 7.2. Note that engineering samples LGS-8913-B1 do not have an exposed pad.

An OrCAD symbol of the LGS-8913-B1 is available from Legend Silicon to facilitate schematic entry and PCB design.

REF	TYP	MIN	MAX
A			1.600
A1		0.050	0.150
A2	1.400	1.350	1.450
b	0.220	0.170	0.270
D	22.000		
D1	20.000		
D2	9.800		
E	16.000		
E1	14.000		
E2	9.800		
e	0.500		
L	0.600	0.450	0.750
L1	1.000		
K		0.000°	7.000°

All dimensions in mm except K.



9. PACKAGE HANDLING GUIDELINES

The devices are packed onto trays and vacuum-sealed for delivery. Each tray can hold up to 72 of the 128 LQFP devices and there can be up to six trays sealed together in one box for a total of 432 devices per box.

The shelf life of an unopened sealed bag is 12 months at < 40°C and < 90% relative humidity. After the bag is opened, if the devices are to be used in a reflow board assembly process (225°C max peak package body temp), then they must be mounted within a certain time limit (described below) or stored with < 10% relative humidity. This is to ensure the devices don't contain excess moisture that could lead to package cracking or other defects when exposed to the heat of the reflow process during board assembly. The devices comply with JEDEC moisture sensitivity level 3. For more details, see the document IPC/JEDEC J-STD-033A at www.jedec.org.

When to re-bake:

- Inside the vacuum-sealed container there is desiccant to absorb any extra moisture and also a humidity sensor card. If the humidity sensor card is > 10% when read at 23°C ± 5°C then re-bake before reflow.

- If the devices are out of the bag (floor life) for more than one week at <= 30°C & 60% relative humidity, then re-bake before reflow.

How to re-bake:

The devices should be re-baked for 12 hours at 125°C.

ELECTRO-STATIC DISCHARGE

The ESD susceptibility is guaranteed to conform to the Human Body Model with 2 kV discharged through a 1.5 kΩ resistor as illustrated in the following diagram: