National Semiconductor

LH0032/LH0032C Ultra Fast FET Operational Amplifier

General Description

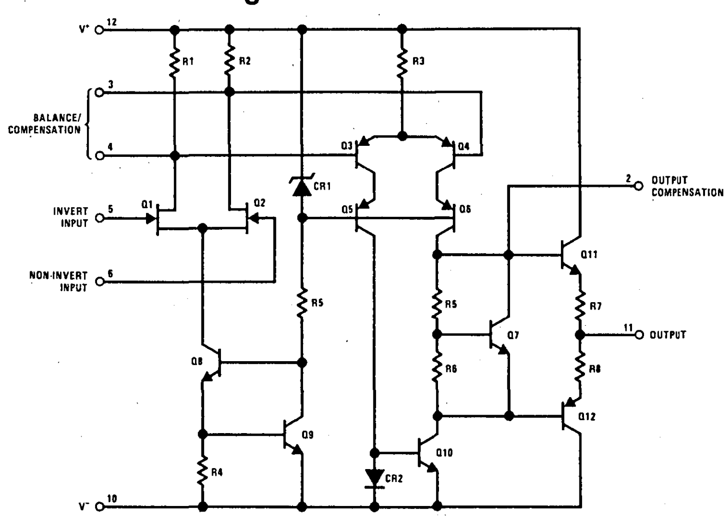
The LH0032/LH0032C is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

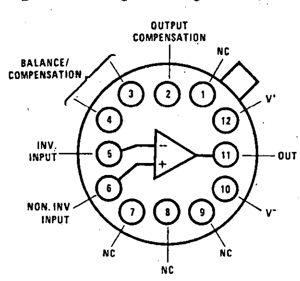
Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- 5 mV max. input offset voltage
- FET input
- Offset null with single pot
- No compensation for gains above 50
- Peak output current to 100 mA

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed over the temperature range −55°C to +125°C and the LH0032C is guaranteed from −25°C to +85°C.

Schematic and Connection Diagrams





Order Number LH0032G or LH0032CG
See NS Package H12B

Absolute Maximum Ratings

Supply Voltage, V_S	±18V
Input Voltage, V_{IN}	$\pm V_S$
Differential Input Voltage	±30V or $\pm 2V_S$
Power Dissipation, P_D	
$T_A = 25°C$	1.5W, derate 100°C/W to 125°C (Note 1)
$T_C = 25°C$	2.2W, derate 70°C/W to 125°C (Note 1)
Operating Temperature Range, T_A	
LH0032G	−55°C to +125°C
LH0032CG	−25°C to +85°C
Operating Junction Temperature, T_J	175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter		Test Conditions		LH0032G			LH0032CG			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage		$T_A = T_J = 25°C$ (Note 2)		2	5 10		2	15 20	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift				25			25		μV/°C
I_{OS}	Input Offset Current	$V_{IN} = 0$	$T_J = 25°C$ (Note 2) $T_A = 25°C$ (Note 3) $T_J = T_A = T_{MAX}$			25 250 25			50 500 5	pA pA nA
I_B	Input Bias Current		$T_J = 25°C$ (Note 2) $T_A = 25°C$ (Note 3) $T_J = T_A = T_{MAX}$			100 1 50			500 5 15	pA nA nA
V_{INCM}	Input Voltage Range			±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = 10V$		50	60		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	$V_O = \pm 10V$, f = 1 kHz	$T_J = 25°C$	60	70		60	70		dB
		$R_L = 1 k\Omega$		57			57			
V_O	Output Voltage Swing	$R_L = 1 k\Omega$		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_J = 25°C$, $I_O = 0$			18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	$\Delta V_S = 10V$		50	60		50	60		dB

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1 k\Omega$, $T_J = 25°C$

Parameter		Conditions		Min.	Typ.	Max.	Units
S_R	Slew Rate	$A_V = +1$	$\Delta V_{IN} = 20V$	350	500		V/μs
t_S	Settling Time to 1% of Final Value	$A_V = -1$,			100		
t_S	Settling Time to 0.1% of Final Value				300		ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$			8	20	
t_D	Small Signal Delay time				10	25	

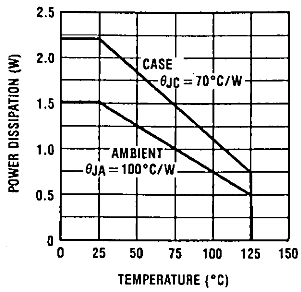
Note 1: In order to limit maximum junction temperature to +175°C, it may be necessary to operate with $V_S < \pm 15V$ when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See Applications Notes AN277, "Applications of Wide-Band Buffer Amplifiers" and AN253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

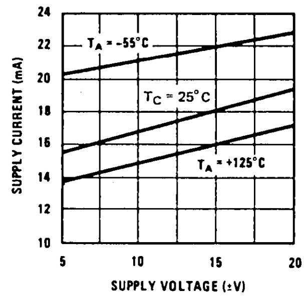
Note 3: Measured in still air 7 minutes after application of power.

Typical Performance Characteristics

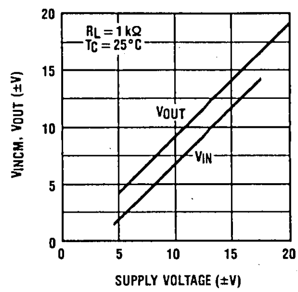
Maximum Power Dissipation



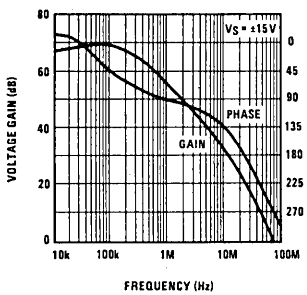
Supply Current vs. Supply Voltage



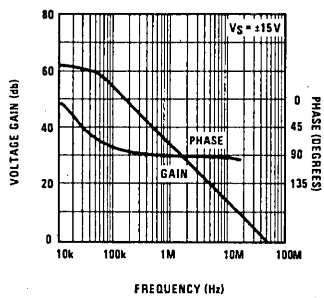
Input Voltage Range and Output Voltage vs. Supply Voltage



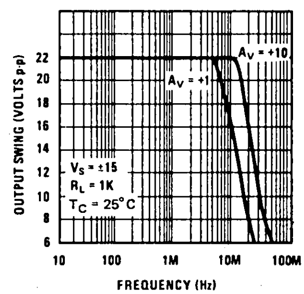
Bode Plot (Uncompensated)



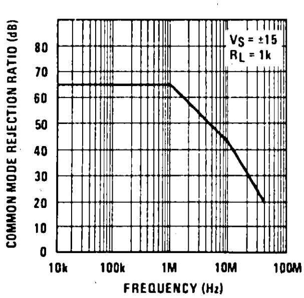
Bode Plot (Unity Gain Compensation)



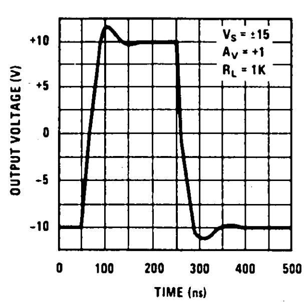
Large Signal Frequency Response



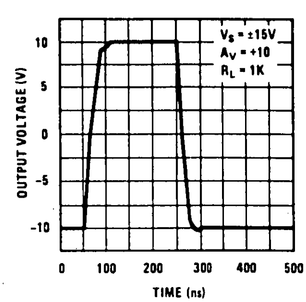
Common Mode Rejection Ratio vs. Frequency



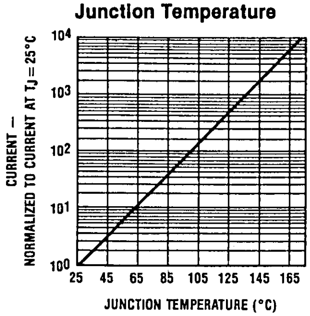
Large Signal Pulse Response



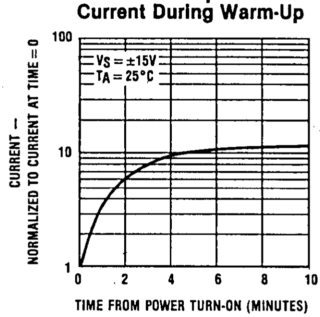
Large Signal Pulse Response



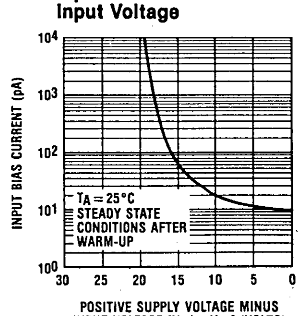
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up

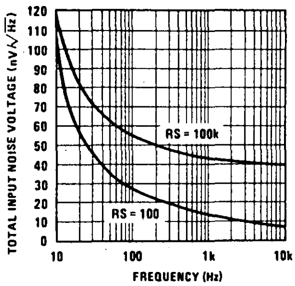


Input Bias Current vs. Input Voltage



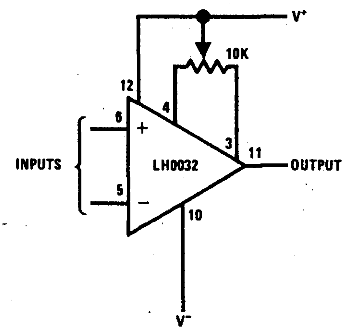
Auxiliary Circuits

Total Input Noise Voltage vs. Frequency*

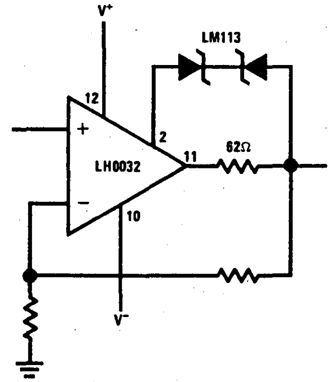


* Noise voltage includes contribution from source resistance.

Offset Null

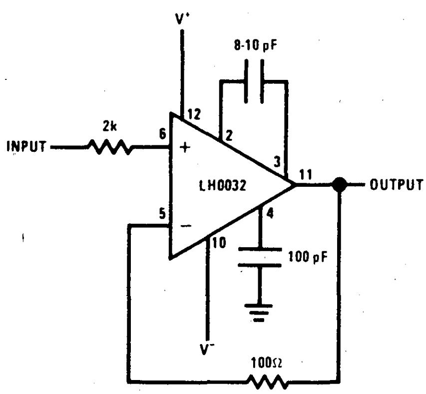


Output Short Circuit Protection



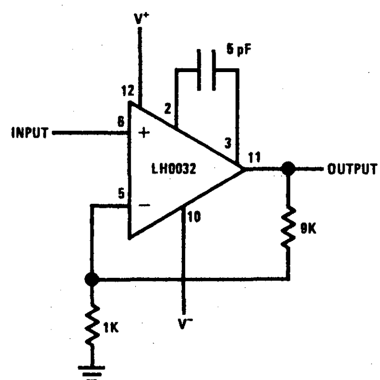
Typical Applications

Unity Gain Amplifier



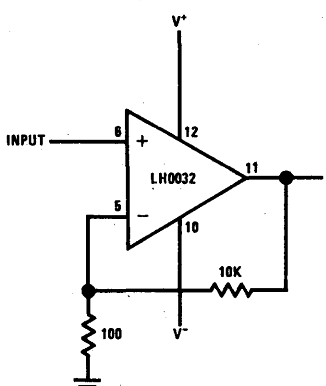
TYP. $BW_{3dB} = 45$ MHz

10X Buffer Amplifier



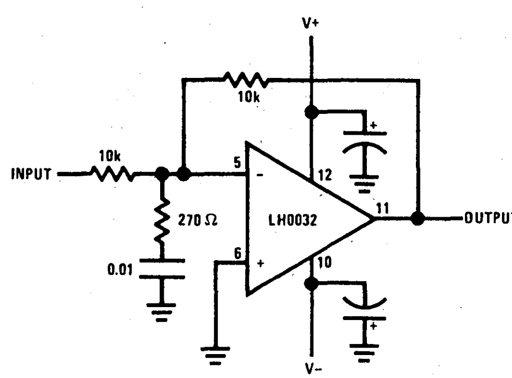
TYP. $BW_{3dB} = 10$ MHz

100X Buffer Amplifier



TYP. $BW_{3dB} = 5$ MHz

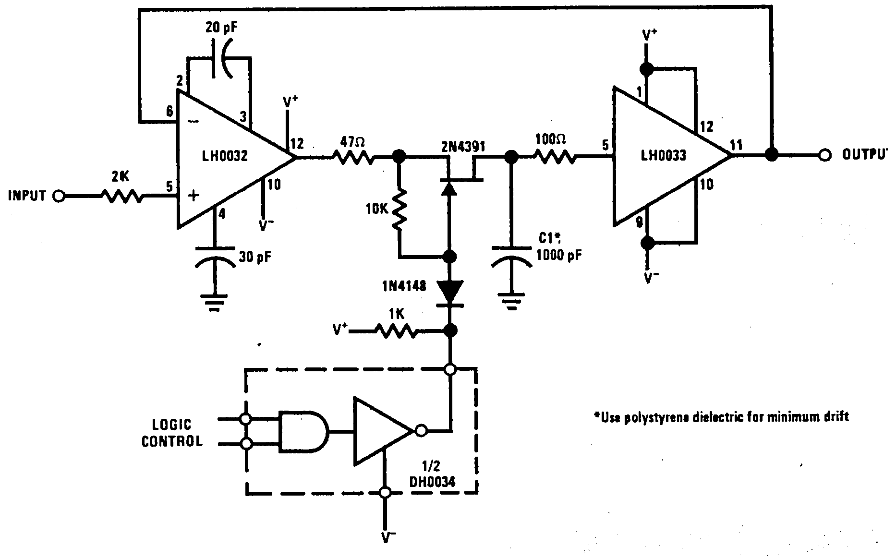
Non-Compensated Unity Gain Inverter



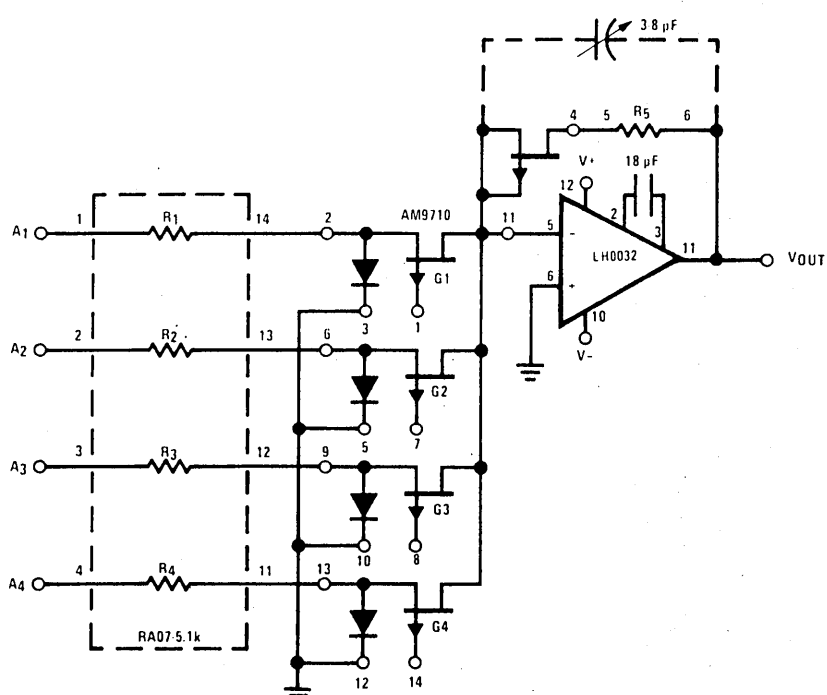
TYP. $BW_{3dB} = 70$ MHz

Typical Applications (cont'd)

High Speed Sample and Hold



High Speed Current Mode MUX



Applications Information

Power Supply Decoupling

The LH0032/LH0032C, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40-60°C above free-air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5-10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leqslant \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the LH0032/LH0032C is typically 5 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

Heat Sinking

While the LH0032/LH0032C is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information see Application Note AN-253.