National Semiconductor

LH0086/LH0086C Digitally-Programmable-Gain Amplifier

General Description

The LH0086 is a self-contained, high-accuracy, digitally-programmable-gain amplifier. It consists of a FET-input operational amplifier, a precision resistor ladder, and a digitally-programmable switch network. A three-bit TTL-compatible digital input selects accurate gain settings of 1, 2, 5, 10, 20, 50, 100, or 200.

The LH0086 exhibits low offset voltage, high input impedance, fast settling, high power supply rejection ratio, and excellent gain accuracy and gain non-linearity.

The LH0086 is specified for operation from −55°C to +125°C. The LH0086C is specified from −25°C to +85°C. Both devices are hermetically sealed in a 14-lead dual-in-line metal package.

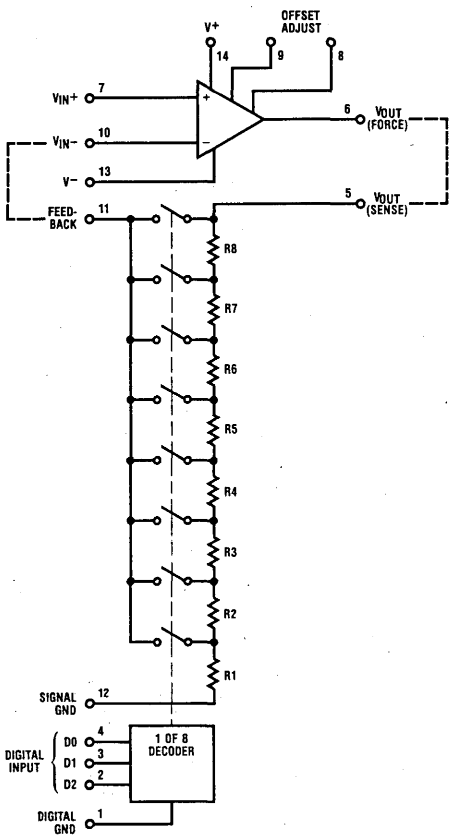
Features

- 0.01% gain accuracy at gain = 1
- 0.005% gain non-linearity
- 1 ppm/°C typical gain drift
- $10^{10}\Omega$ input impedance
- 80 dB minimum PSRR.
- TTL-compatible digital inputs
- 2 μs settling to 0.01%

Applications

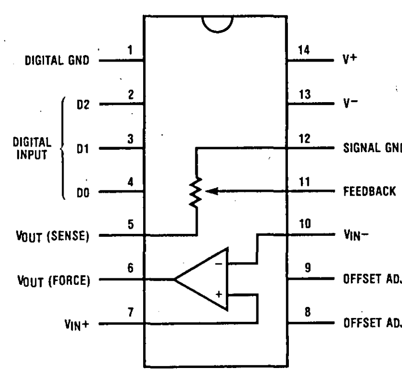
- Data acquisition systems
- Auto range DVMs
- Adaptive servo loops

Simplified Schematic



Connection Diagram

Dual-In-Line Package



CASE IS ELECTRICALLY ISOLATED

Top View

Order Number LH0086D or LH0086CD
See NS Package D14F

Absolute Maximum Ratings

V_S	Supply Voltage (Note 1)	±18V
V_{IN}	Analog Input Voltage (Note 2)	±15V
$V_{IL(H)}$	Digital Input Voltage	$-4V, +V_S$
P_D	Power Dissipation	500 mW
	Output Short Circuit Duration	Continuous
T_A	Operating Temperature Range:	
	LH0086	−55°C to +125°C
	LH0086C	−25°C to +85°C
T_{STG}	Storage Temperature	−65°C to +150°C
	Lead Temperature (soldering, 20 seconds)	+300°C

DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 10 k\Omega$, $T_{MIN} \leqslant T_A \leqslant T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting)

Parameter		Conditions		LH0086			LH0086C			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage		$T_J = 25°C$		0.3	5.0		0.3	10	mV
						7.0			13	mV
$V_{OS}/\Delta T$	Input Offset Voltage Change with Temperature	$V_{IN} = 0V$			10			10		μV/°C
I_B	Input Bias Current	(Notes 3, 4)	$T_J = 25°C$		100	500		100	500	pA
						500			100	nA
R_{IN}	Input Resistance				10			10		GΩ
V_{IN}	Input Voltage Range			±10	±11.5		±10	±11.5		V
A_V	Voltage Gain	See Table 1, p. 5, for Digital Gain-Control Codes			1.0			1.0		V/V
					2.0			2.0		
					5.0			5.0		
					10			10		
					20			20		
					50			50		
					100			100		
					200			200		
	Gain Error	$A_V = 1$	$T_A = 25°C$		0.003	0.01		0.003	0.03	%
		$A_V = 2,5$	$T_A = 25°C$		0.03	0.05		0.05	0.1	
		$A_V = 10,20$	$T_A = 25°C$		0.05	0.1		0.1	0.2	
		$A_V = 50,100,200$	$T_A = 25°C$		0.1	0.2		0.15	0.3	
		$A_V = 1$			0.003	0.02		0.003	0.06	
		$A_V = 2,5$			0.03	0.1		0.05	0.2	
		$A_V = 10,20$			0.1	0.2		0.1	0.3	
		$A_V = 50,100,200$			0.15	0.3		0.15	0.4	
	Gain Non-Linearity	$A_V = 1$	$T_A = 25°C$		0.002			0.002		%
					0.005			0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient	$A_V = 1$			1.0			1.0		ppm/°C
PSRR	Power Supply Rejection Ratio	$\pm 8V \leqslant V_S \leqslant \pm 18V$		80	90		70	90		dB
V_O	Output Voltage Swing	$R_L \geqslant 10 k\Omega$		±10	±12		±10	±12		V

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection Section under Applications Information.

Note 2: For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

Note 3: Due to short production test time, these parameters are specified at junction temperature, $T_J = 25°C$. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of the internal power dissipation, PD. $T_J = T_A + \theta_{jA} \times PD$ where θ_{jA} is the thermal resistance from junction to ambient (typically 65°C/W).

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in junction temperature.

DC Electrical Characteristics (cont'd)

$V_S = \pm 15V$, $R_L = 10 k\Omega$, $T_{MIN} \leq T_A \leq T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting).

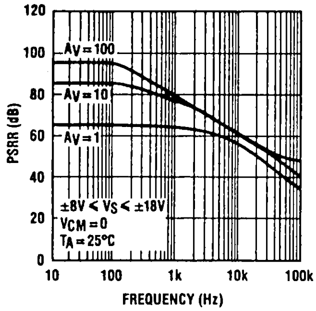
Parameter		Conditions		LH0086			LH0086C			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{SC}	Output Short-Circuit Current		$T_A = 25°C$	±5	±18	±30	±5	±18	±30	mA
				±2		±30	±2		±30	mA
R_O	Output Resistance	$A_{VCL} = 1$			0.05			0.05		Ω
V_{IL}	Digital "0" Input Voltage					0.7			0.7	V
V_{IH}	Digital "1" Input Voltage			2.0			2.0			V
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$			1.5	4.0		1.5	4.0	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$			0.01			0.01		μA
V_S	Supply Voltage Range			±8.0		±18	±8.0		±18	V
$I_S^{(+)}$	Positive Supply Current	$V_S = \pm 18V$			8.5	15.5		8.5	15.5	mA
$I_S^{(-)}$	Negative Supply Current	$V_S = \pm 18V$			−4.5	−8.5		−4.5	−8.5	mA

AC Electrical Characteristics

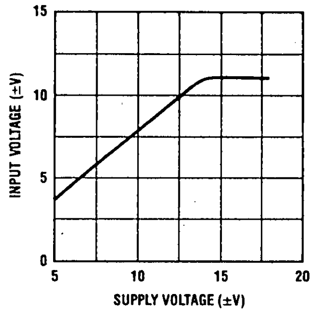
$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10 k\Omega$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting)

Parameter		Conditions		Min.	Typ.	Max.	Units
BW	Small Signal Bandwidth	−3dB	$A_V = 1$		3000		kHz
			$A_V = 50$		60		
			$A_V = 200$		15		
		−1%	$A_V = 1$		425		
			$A_V = 50$		8.5		
			$A_V = 200$		2		
PBW	Power Bandwidth	$V_O = \pm 10V$			159		kHz
SR	Slew Rate	$V_O = \pm 10V$			10		V/μs
t_S	Settling Time (Figure 7) 0.01%	$\Delta V_O = 20V$	$A_V = 1$		2.5		μs
			$A_V = 50$		20		
			$A_V = 200$		75		
t_S	Settling Time After Gain Change				10		μs
$\overline{e}_N$	Equivalent Input Noise Voltage (Figure 6)	$R_S = 100\Omega$, $A_V = 100$	BW = 0.1–10Hz		3		μV_{P-P}
			f = 1kHz		25		$nV/\sqrt{Hz}$
$\overline{i}_N$	Equivalent Input Noise Current	$R_S = 100\Omega$, $A_V = 100$	f = 1kHz		0.01		$pA/\sqrt{Hz}$

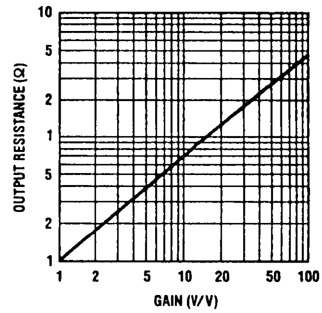
Power Supply Rejection



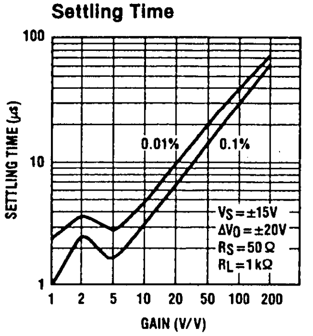
Input Voltage Range



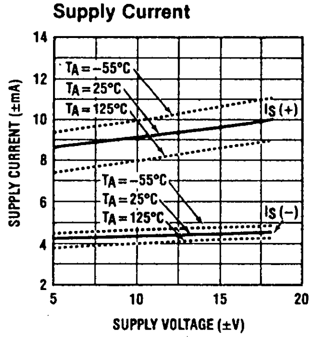
Closed Loop Output Resistance



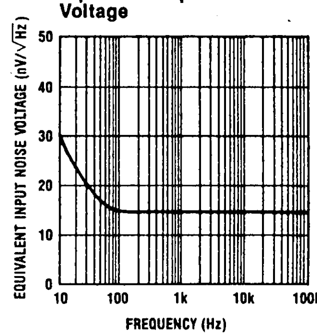
Settling Time



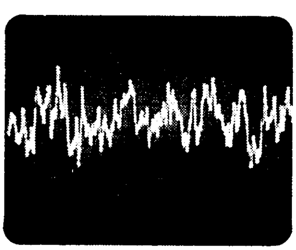
Supply Current



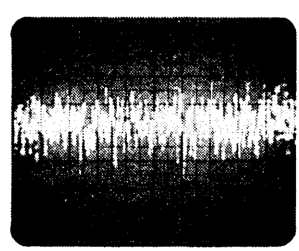
Equivalent Input Noise Voltage



Wideband Noise



$R_S = 50\Omega$. Bandwidth = 0.1 Hz to 10 Hz
1 μV/division Vertical, 5 seconds/division Horizontal



$R_S = 50\Omega$. Bandwidth = 10 Hz to 10 kHz
5 μV/division Vertical, 1 ms/division Horizontal

Applications Information

Theory of Operation

The LH0086 is a digitally programmable gain amplifier with 3-bit digital gain control. It contains a FET-input operational amplifier, a precision resistor ladder, and a digitally programmable switch network.

The LH0086 was designed for use in a non-inverting configuration, thus the following discussion covers the LH0086 as used as a non-inverting amplifier. The gain of the LH0086 is given by the familiar gain equation of a non-inverting amplifier.

$$A_V = 1 + \frac{R_F}{R_S}$$

Each gain step is set by the ratio of the ladder resistors. The resistor ladder is constructed with high stability, low temperature-coefficient resistors precision laser-trimmed to the required values. FET switches are used to select the desired ratio. Since the FET switches are in series with the operational amplifier input, their "on resistance" and temperature drift do not degrade amplifier accuracy. The FET switches are selected by a 1 of 8 decoder, by applying the proper logic levels at digital inputs D0, D1, and D2. The gains are set as given in Table 1.

Table 1. Gain-Control Codes

Gain	D2	D1	D0
1	0	0	0
2	0	0	1
5	0	1	0
10	0	1	1
20	1	0	0
50	1	0	1
100	1	1	0
200	1	1	1

Power Supply Connection

Proper power supply connections are shown in Figure 1. The power supplies should be bypassed to ground as close as possible to device supply pins. For most applications, the bypass capacitor should be 0.1μF.

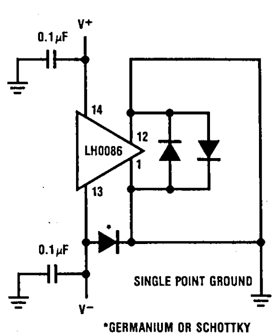


Figure 1. Power Supply and Ground Connections

Care must be taken in the power-on sequence. The LH0086 may suffer irreversible damage if the V^+ supply is applied prior to the powering on of the V^- supply. In most applications using dual-tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V^- pin as shown in Figure 1.

Grounding Considerations

Care should be taken in the connection of digital and analog grounds. Digital switching currents can introduce noise on the analog ground pin. If possible, both grounds should go to a ground plane beneath the device, otherwise each ground should be run separately to a single point ground. The idea is to keep digital current from passing through the analog ground line. If long ground leads are used, diode clamps should be placed as close to the device as possible (Figure 1).

Programmable Attenuator

The LH0086 may be used as a programmable attenuator when connected as in Figure 2. The accuracy of this attenuator will be typically 0.1%.

Note: Max. $V_{IN} = \pm 11$ Volts.

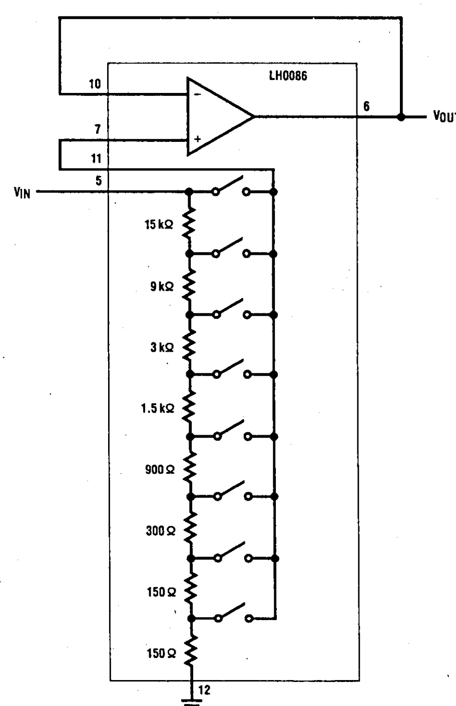


Figure 2. Programmable Attenuator

Table 2. Attenuator Codes

D2	D1	D0	Attenuation
0	0	0	1
0	0	1	2
0	1	0	5
0	1	1	10
1	0	0	20
1	0	1	50
1	1	0	100
1	1	1	200

Table 3. Inverting Gain Chart

D2	D1	D0	Gain	R_{IN} (Ω)
0	0	0	$A_V = 0$	30k
0	0	1	$A_V = 1$	15k
0	1	0	$A_V = 4$	6k
0	1	1	$A_V = 9$	3k
1	0	0	$A_V = 19$	1.5k
1	0	1	$A_V = 49$	600
1	1	0	$A_V = 99$	300
1	1	1	$A_V = 199$	150

Inverting Mode

The LH0086 may be used in the inverting mode, however, there are several design considerations.

1. Input resistance is low at high gains (see gain chart for input resistance at each gain).
2. Each gain step gets a one subtracted from the non-inverting gain. (See inverting gain chart for available gains.)
3. The first gain step (digital code of 000) cannot be used because the output will remain at virtual ground regardless of the input.

Remote Output Sense

The V_{OUT} sense pin of the LH0086 should be connected at the load in order to eliminate errors due to lead resistance. In any case the output sense and output force must be tied together at some point. See Figure 4.

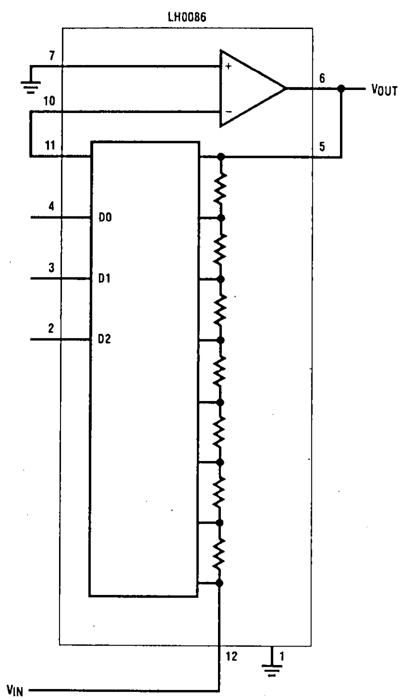


Figure 3. LH0086 Inverting Gain Configuration

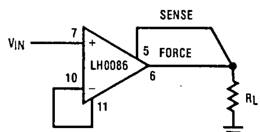


Figure 4. Remote Output Sense

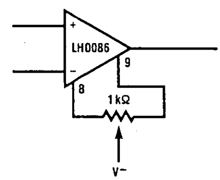


Figure 5. Offset Adjustment

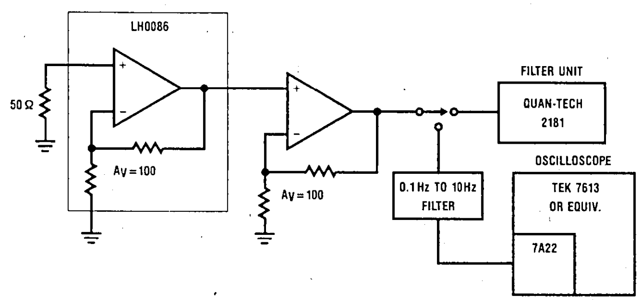


Figure 6. Noise Measurement Circuit

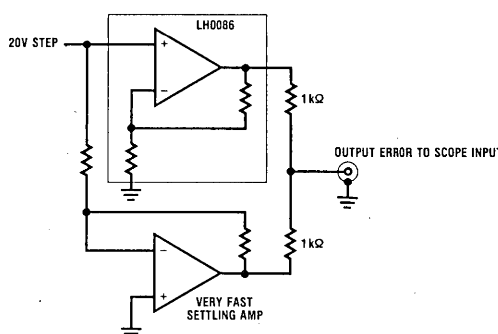


Figure 7. Settling Time Test Circuit

Definition of Terms

V_{OS} **Offset Voltage:** The voltage that must be applied to force the output to 0 volts.

I_B **Input Bias Current:** The current into Pin 7 with the device connected in the non-inverting configuration.

R_{IN} **Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

V_{IN} **Input Voltage Range:** The voltage range for which the device is operational.

PSRR **Power Supply Rejection Ratio:** The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

A_V **Voltage Gain:** The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full scale (10V for operation with ±15V supplies). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

V_O **Output Voltage Swing:** The peak output voltage swing referenced to ground into specified load.

$I_{O(SC)}$ **Output Short-Circuit Current:** The current supplied by the device with the output connected directly to ground.

R_O **Closed Loop Output Resistance:** The ratio of change in output voltage to change to output current at a specific gain.

V_S **Supply Voltage Range:** The supply voltage range for which the device is operational.

I_S **Supply Current:** The current required from the supply to operate the device with no load and with the analog as well as the digital inputs at 0V.

P_D **Power Dissipation:** The power dissipated in the device with no load and with the analog as well as the digital inputs at 0V.

V_{IH} **Digital "1" Input Voltage:** Minimum voltage required at the digital input to guarantee a high logic state.

V_{IL} **Digital "0" Input Voltage:** The current into a digital input at specified logic level.

$\Delta V_{OS}/\Delta T$ **Average Input Offset Voltage Drift:** The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

$\Delta A_V/\Delta T$ **Average Gain Temperature Coefficient:** The ratio in gain from 25°C to either temperature extreme divided by the temperature range.

BW **Bandwidth:** The frequency at which the voltage gain is reduced to 3 dB below the low frequency value.

PBW **Power Bandwidth:** Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

SR **Slew Rate:** The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

t_S **Settling Time:** The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

e_N **Equivalent Input Noise Voltage:** The rms or peak noise voltage referred to the input (RTI) over a specified frequency band.

i_N **Equivalent Input Noise Current:** The rms or peak noise current referred to the input (RTI) over a specified frequency band.