SHARP

LH168B/LH168G

324 Outputs 64 Gradations
TFT-LCD Source Driver

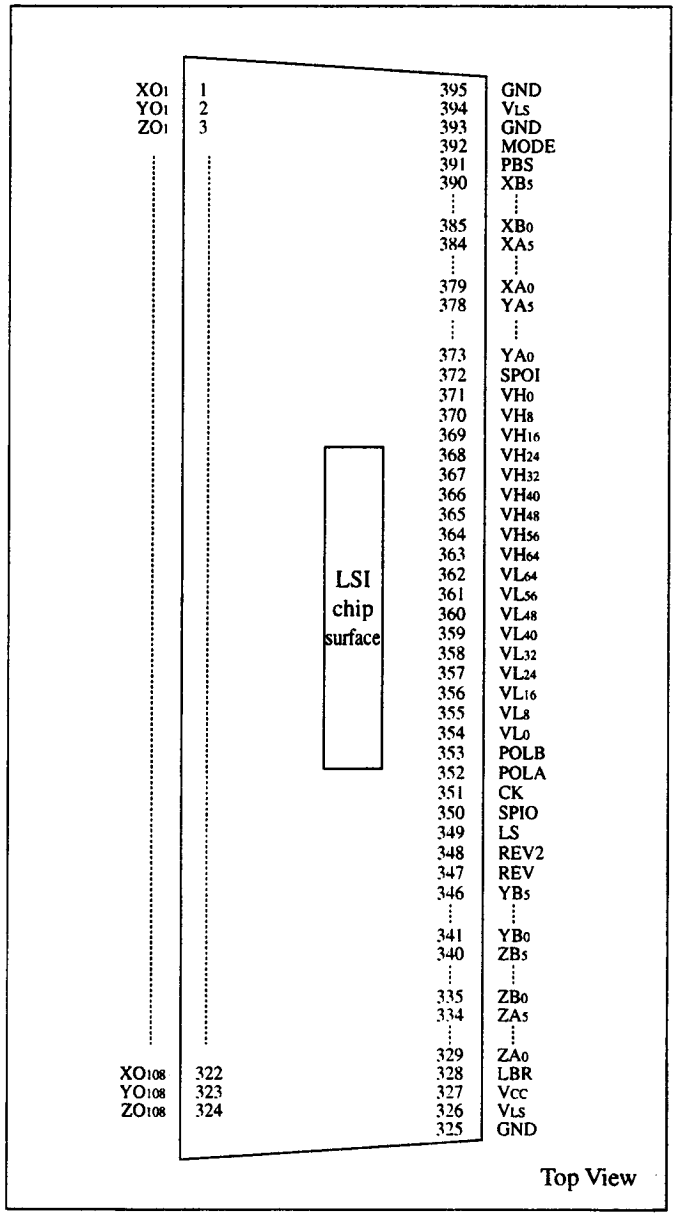
■ Description

The LH168B/LH168G are a source driver with 324 LCD drive outputs, and are used for the TFT LCD unit which can simultaneously display 262 144 colors in 64 gradations.

■ Features

1. The LH168B/LH168G are a driver which incorporates a 6-bit digital input DAC.
2. The LH168B/LH168G are a Dot-Inversion driver that the LCD drive pin inverted gradational voltage at the next LCD drive pins.
3. The number of LCD drive output is 324 outputs and they can change to 321 outputs, 312 outputs and 309 outputs.
4. The circuit of data input have two port inputs at the number of LCD drive outputs is 324 outputs and 312 outputs. They can sample & hold display data of two pixels at the sametime. And the circuit of data input have one port inputs at the number of LCD drive outputs is 321 outputs or 309 outputs.
5. The basic voltage input of 18 gradations can display 262 144 colors in 64 gradations. This basic voltage input corresponds to γ correction and the intermediate basic voltage input can be abbreviated.
6. Shift clock frequency is 55 MHz (MAX.).
7. The LH168B/LH168G have the function of cascade connection.
8. It is possible to switch the output directivity of LCD drive output.
   (XO_1, YO_1, $ZO_1 \rightarrow XO_{108}$, YO_{108}, ZO_{108} and ZO_{108}, YO_{108}, $XO_{108} \rightarrow ZO_1$, YO_1, XO_1)
9. Supply voltage V_{CC} for the digital system : 2.7 to 3.6 V
10. Supply voltage V_{LS} for the analog system : 8.0 to 13.0 V
11. Package SST

■ Pin Connections



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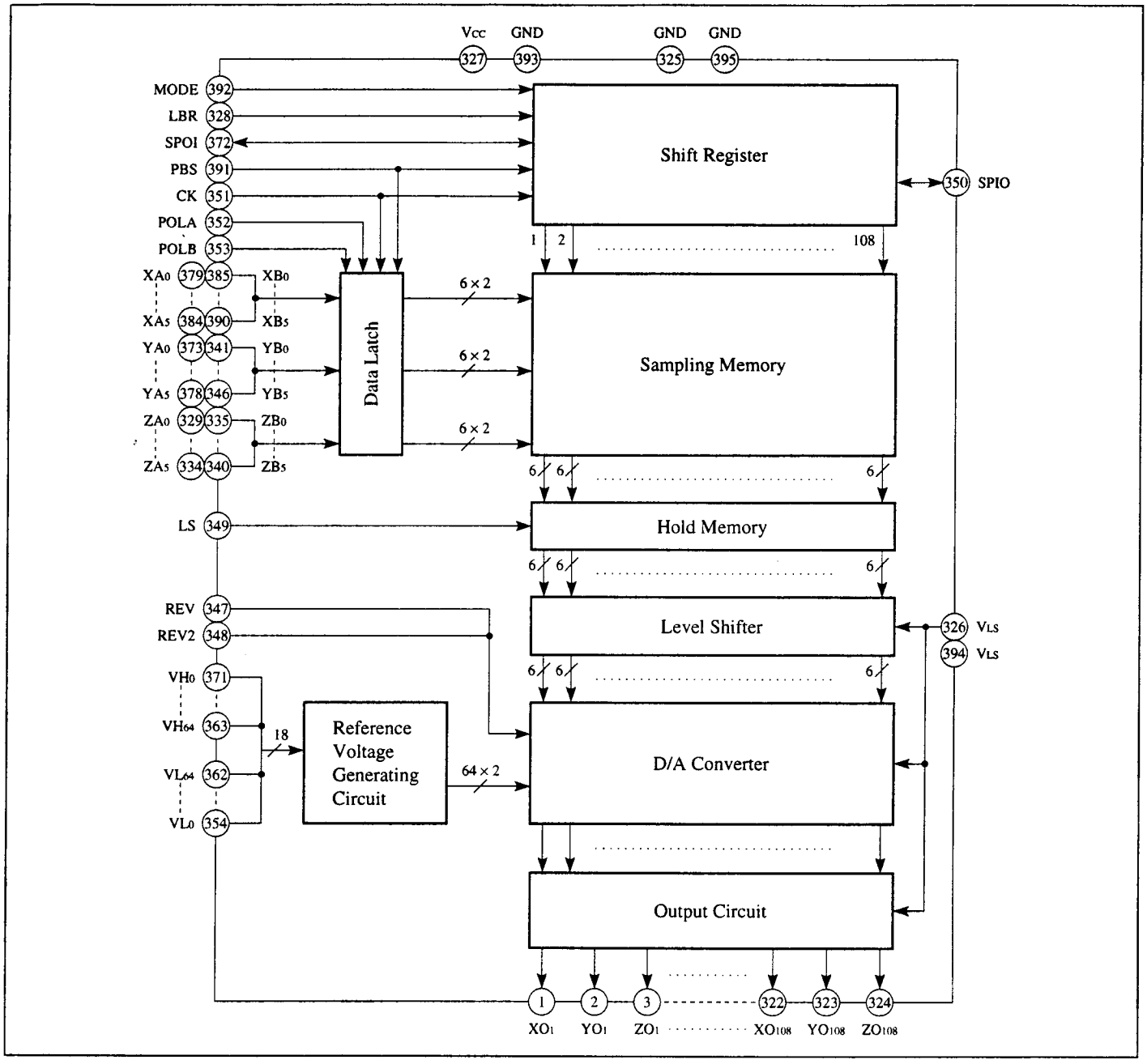
■ Pin Description

No.	Symbol	I/O	Pin name
1-324	XO_1-ZO_{108}	O	LCD drive output pins
325	GND	—	GND
326	V_{LS}	—	Power supply pin for analog circuit
327	V_{CC}	—	Power supply pin for digital circuit
328	LBR	I	Shift direction switching input pin
329-334	ZA_0-ZA_5	I	Data input pins
335-340	ZB_0-ZB_5	I	Data input pins
341-346	YB_0-YB_5	I	Data input pins
347	REV	I	LCD drive output polarity exchange input pin
348	REV_2	I	LCD drive output polarity exchange input pin
349	LS	I	Latch input pin
350	SPIO	I/O	Start pulse input/cascade output pin
351	CK	I	Shift clock input pin
352	POLA	I	Input data polarity exchange input pin
353	POLB	I	Input data polarity exchange input pin
354-362	VL_0-VL_{64}	I	Reference voltage input pins
363-371	VH_{64}-VH_0	I	Reference voltage input pins
372	SPOI	I/O	Start pulse input/cascade output pin
373-378	YA_0-YA_5	I	Data input pins
379-384	XA_0-XA_5	I	Data input pins
385-390	XB_0-XB_5	I	Data input pins
391	PBS	I	2 ports/1 port switching input pin
392	MODE	I	Number of LCD drive output switching input pin
393	GND	—	GND
394	V_{LS}	—	Power supply pin for analog circuit
395	GND	—	GND

■ Block Diagram



■ Block Function

Block name	Block function
Shift register	Used as a bi-directional shift register, which performs the shifting operation by CK and selects bits for data sampling.
Data latch	Used to temporarily latch the input data, which is sent to the sampling memory.
Sampling memory	Used to sample the data to be entered by time sharing.
Hold memory	Used for temporary latch processing of data in the sampling memory by LS input.
Level shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and send the shifted data to D/A converter.
Reference voltage generating circuit	Used to generate a 64 × 2-level voltage corrected of gamma by the resistance split circuit.
D/A converter	Used to generate analog signal according to the displayed data and send the signal to the output circuit.
Output circuit	Used as a voltage follower configured with an operational amplifier and an output buffer, which outputs analog signals of 64 × 2 gradations to LCD drive output pin.

■ Description of Functions and Operations

(1) Pin function

Symbol	I/O	Function
V_{CC}	—	Used as power supply pin for digital circuit (Use in the range of 2.7 to 3.6 V.)
V_{LS}	—	Used as power supply pin for analog circuit (Use in the range of 8 to 13V.)
GND	—	Used as GND pin, which must be connected to 0 V.
SPIO SPOI	I/O	Used as input pin of start pulse and is also used as output pin for cascade connection. When "High" is input into start pulse input pin, data sampling is started. On completion of sampling, "High" pulse is output to output pin for cascade connection. Pin functions are switched by LBR. For relations of switching, refer to "(2) Operation of function".
LBR	I	Used as input pin for switch shift register directivity. For relations of switching, refer to "(2) Operation of function".
LS	I	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at rising edge and output from LCD drive output pin.
CK	I	Used as shift clock input pin. Data is latched into sampling memory from data input pin at rising edge.
VH_0-VH_{64} VL_0-VL_{64}	I	Used as basic voltage input pin. Hold the basic potential before outputting gradation voltage. For relation between displayed data and output voltage value, refer to "(4) Output voltage value". For internal gamma correction, refer to "(5) Gamma correction value". Observe the following relation for input potential. $V_{LS} > VH_0 > VH_8 > \cdots > VH_{64} > VL_{64} > VL_{56} > \cdots > VL_0 > GND$.
XA_0-XA_5 YA_0-YA_5 ZA_0-ZA_5 XB_0-XB_5 YB_0-YB_5 ZB_0-ZB_5	I	Used as data input pin of R, G, and B colors. Takes in 6-bits data from data pin at rising edge of CK. When PBS is "Low", taken in 2-pixels data at the sametime from XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5 and XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5. When PBS is "High", taken in 1-pixel data from XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5. Fix XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5 to "Low" or "High". For relation between input data and output, refer to "(4) Output voltage value". Correlate data to be entered into X, Y, and Z according to picture element arrays of the panel used.
MODE	I	Used as input pin for switch number of LCD drive output, which sets up operation mode with PBS pin. When "Low" is entered, it is 324 outputs/2 ports input mode becomes enable at PBS pin is "Low" or 321 outputs/1 port input mode becomes enable at PBS pin is "High". When "High" is entered, it is 312 outputs/2 ports input mode becomes enable at PBS pin is "Low" or 309 outputs/1 port becomes enable at PBS pin is "High". For relations of switching number or LCD drive output, refer to "(3) Operation mode and output polarity".
PBS	I	Used as 2 ports/1 port exchange input pin to take in data. When "Low" is entered, it is 2 ports input mode becomes enable and takes in 2-pixels data at the sametime. When "High" is entered, it is 1 port input mode becomes enable.
XO_1-XO_{108} YO_1-YO_{108} ZO_1-ZO_{108}	O	Used as LCD drive output pin, which outputs the voltage corresponding to the input of data input pin. In the case of 321 outputs mode, 3 outputs (XO_{54}-ZO_{54}) is invalid. In the case of 312 outputs mode, 12 outputs (XO_{55}-XO_{58}, YO_{55}-YO_{58}, ZO_{55}-ZO_{58}) is invalid. In the case of 309 outputs mode, 15 outputs (XO_{54}-XO_{58}, YO_{54}-YO_{58}, ZO_{54}-ZO_{58}) is invalid. Invalid output pins must be open. Data of XO_1-XO_{108} correspond to XA_0-XA_5, XB_0-XB_5. Data of YO_1-YO_{108} correspond to YA_0-YA_5, YB_0-YB_5, and data of ZO_0-ZO_{108} correspond to ZA_0-ZA_5, ZB_0-ZB_5. For relation of switching and input data, refer to "(2) Operation of function" and "(4) Output voltage value".

Symbol	I/O	Function
POLA POLB	I	Used as input pin for input data polarity exchange, POLA corresponds to XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, POLB corresponds to XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5. When "Low" is entered, displayed data is normal mode becomes enable. When "High" is entered, input data is polarity exchange mode becomes enable. For relation between input data and output, refer to "(4) Output voltage value". This pins are pull-down at the inside.
REV REV_2	I	Used as polarity exchange pin of LCD drive output. Takes in data at the term that LS is "High", decides output polarity of LCD drive output pin. Function of REV is the sames as function of REV_2. Input polarity exchange signal to REV pin and REV_2 is used to fix to "Low" or be open in generally. In the case of 321 outputs/309 outputs mode, it is possible to exchange output polarity between next driver by REV_2 is fixed to "Low" or "High" according to position on panel. For switching relation, refer to "(3) Operational mode and output polarity". REV_2 pin is pull-down at the inside.

(2) Operation of function

The following describes the relation between data input pin and output direction.

○PBS = "Low"

Data input pin	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5	XB_0-XB_5	YB_0-YB_5	ZB_0-ZB_5	.....	XB_0-XB_5	YB_0-YB_5	ZB_0-ZB_5
Output direction	XO_1	YO_1	ZO_1	XO_2	YO_2	ZO_2	.....	XO_{108}	YO_{108}	ZO_{108}

○PBS = "High"

Data input pin	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5	.....	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5
Output direction	XO_1	YO_1	ZO_1	XO_2	YO_2	ZO_2	.....	XO_{108}	YO_{108}	ZO_{108}

The following describes the relation between LBR pin, SP pin and output direction.

Pin	RIGHT SHIFT (Shift register directivity)	LEFT SHIFT (Shift register directivity)
LBR	"High"	"Low"
SPOI	Input	Output
SPIO	Output	Input
Output direction	XO_1, YO_1, ZO_1 (first clock) → XO_{108}, YO_{108}, ZO_{108} (last clock)	ZO_{108}, YO_{108}, XO_{108} (first clock) → ZO_1, YO_1, XO_1 (last clock)

Note. Color data corresponding to X, Y and Z vary depending on RIGHT SHIFT/LEFT SHIFT.

(3) Operational mode and output polarity

The following describes the relation between operational mode, REV pin, REV_2 pin and output polarity of LCD drive output pin.

	In the case of REV = "Low", REV_2 = "Low" or REV = "High", REV_2 = "High"				In the case of REV = "High", REV_2 = "Low" or REV = "Low", REV_2 = "High"			
MODE	"Low"	"Low"	"High"	"High"	"Low"	"Low"	"High"	"High"
PBS	"Low"	"High"	"Low"	"High"	"Low"	"High"	"Low"	"High"
Operation	324 out	321 out	312 out	309 out	324 out	321 out	312 out	309 out
XO_1	–	–	–	–	+	+	+	+
YO_1	+	+	+	+	–	–	–	–
ZO_1	–	–	–	–	+	+	+	+
XO_2	+	+	+	+	–	–	–	–
YO_2	–	–	–	–	+	+	+	+
ZO_2	+	+	+	+	–	–	–	–
.....								
XO_{53}	–	–	–	–	+	+	+	+
YO_{53}	+	+	+	+	–	–	–	–
ZO_{53}	–	–	–	–	+	+	+	+
XO_{54}	+	NA	+	NA	–	NA	–	NA
YO_{54}	–	NA	–	NA	+	NA	+	NA
ZO_{54}	+	NA	+	NA	–	NA	–	NA
XO_{55}	–	+	NA	NA	+	–	NA	NA
YO_{55}	+	–	NA	NA	–	+	NA	NA
ZO_{55}	–	+	NA	NA	+	–	NA	NA
XO_{56}	+	–	NA	NA	–	+	NA	NA
YO_{56}	–	+	NA	NA	+	–	NA	NA
ZO_{56}	+	–	NA	NA	–	+	NA	NA
XO_{57}	–	+	NA	NA	+	–	NA	NA
YO_{57}	+	–	NA	NA	–	+	NA	NA
ZO_{57}	–	+	NA	NA	+	–	NA	NA
XO_{58}	+	–	NA	NA	–	+	NA	NA
YO_{58}	–	+	NA	NA	+	–	NA	NA
ZO_{58}	+	–	NA	NA	–	+	NA	NA
XO_{59}	–	+	–	+	+	–	+	–
YO_{59}	+	–	+	–	–	+	–	+
ZO_{59}	–	+	–	+	+	–	+	–
.....								
XO_{107}	–	+	–	+	+	–	+	–
YO_{107}	+	–	+	–	–	+	–	+
ZO_{107}	–	+	–	+	+	–	+	–
XO_{108}	+	–	+	–	–	+	–	+
YO_{108}	–	+	–	+	+	–	+	–
ZO_{108}	+	–	+	–	–	+	–	+

Note. + : The gradation voltage corresponding to the basic voltage VH_0-VH_{64} is output.
– : The gradation voltage corresponding to the basic voltage VL_0-VL_{64} is output.
NA : Non active. Must be open.

(4) Output voltage value

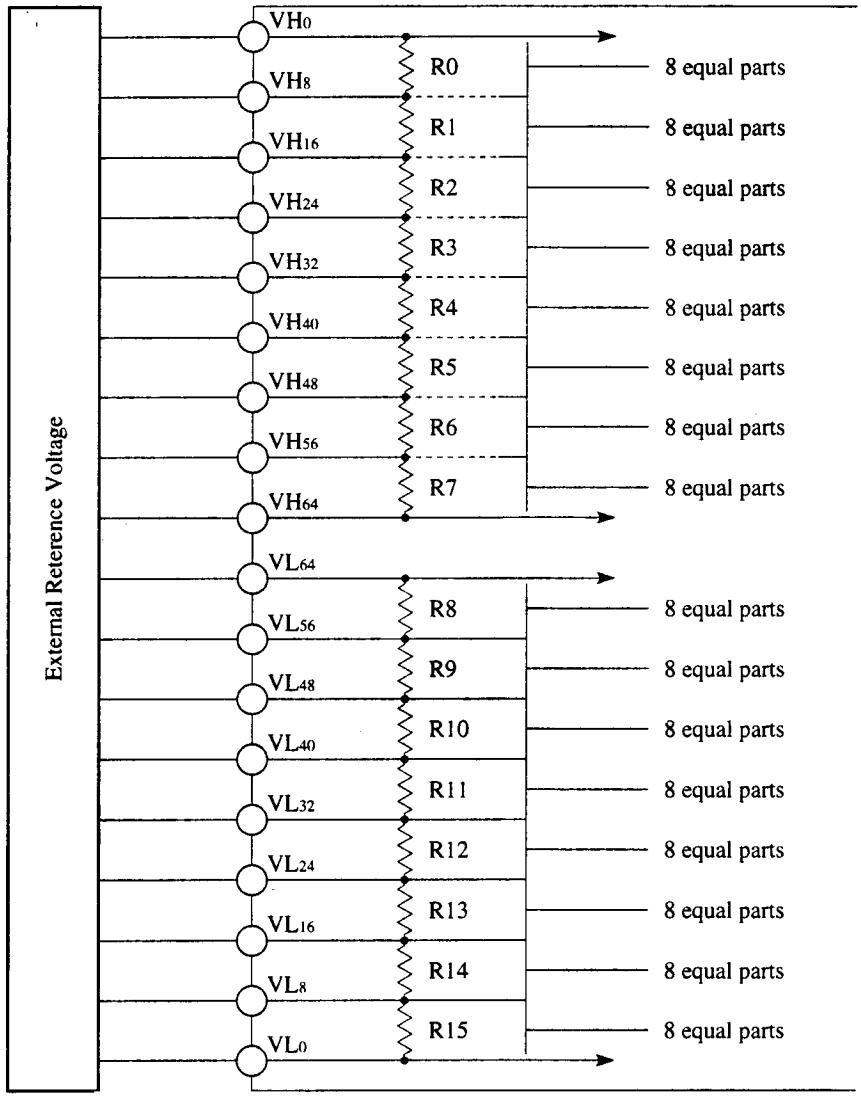
Of the 6-bit data (D_5, D_4, D_3, D_2, D_1 and D_0) taken in by time sharing, two reference voltages of reference voltage input V_0 to V_{64} are selected by upper 3 bits (D_5, D_4 and D_3) and interpolation value divided two reference voltage into equal parts are determined by lower 3 bits (D_2, D_1, and D_0). The basic voltage V_i is referance voltage (VH_i or VL_i) that determined by polarity exchange input (REV, REV_2). Relation between input data and output voltage values is shown below.

Input data	Output voltage		Input data	Output voltage	
	POLA (POLB) = "Low"	POLA (POLB) = "High"		POLA (POLB) = "Low"	POLA (POLB) = "High"
0	V_0	$V_{64} + (V_{56} - V_{64}) \times 1/8$	20	V_{32}	$V_{32} + (V_{24} - V_{32}) \times 1/8$
1	$V_8 + (V_0 - V_8) \times 7/8$	$V_{64} + (V_{56} - V_{64}) \times 2/8$	21	$V_{40} + (V_{32} - V_{40}) \times 7/8$	$V_{32} + (V_{24} - V_{32}) \times 2/8$
2	$V_8 + (V_0 - V_8) \times 6/8$	$V_{64} + (V_{56} - V_{64}) \times 3/8$	22	$V_{40} + (V_{32} - V_{40}) \times 6/8$	$V_{32} + (V_{24} - V_{32}) \times 3/8$
3	$V_8 + (V_0 - V_8) \times 5/8$	$V_{64} + (V_{56} - V_{64}) \times 4/8$	23	$V_{40} + (V_{32} - V_{40}) \times 5/8$	$V_{32} + (V_{24} - V_{32}) \times 4/8$
4	$V_8 + (V_0 - V_8) \times 4/8$	$V_{64} + (V_{56} - V_{64}) \times 5/8$	24	$V_{40} + (V_{32} - V_{40}) \times 4/8$	$V_{32} + (V_{24} - V_{32}) \times 5/8$
5	$V_8 + (V_0 - V_8) \times 3/8$	$V_{64} + (V_{56} - V_{64}) \times 6/8$	25	$V_{40} + (V_{32} - V_{40}) \times 3/8$	$V_{32} + (V_{24} - V_{32}) \times 6/8$
6	$V_8 + (V_0 - V_8) \times 2/8$	$V_{64} + (V_{56} - V_{64}) \times 7/8$	26	$V_{40} + (V_{32} - V_{40}) \times 2/8$	$V_{32} + (V_{24} - V_{32}) \times 7/8$
7	$V_8 + (V_0 - V_8) \times 1/8$	V_{56}	27	$V_{40} + (V_{32} - V_{40}) \times 1/8$	V_{24}
8	V_8	$V_{56} + (V_{48} - V_{56}) \times 1/8$	28	V_{40}	$V_{24} + (V_{16} - V_{24}) \times 1/8$
9	$V_{16} + (V_8 - V_{16}) \times 7/8$	$V_{56} + (V_{48} - V_{56}) \times 2/8$	29	$V_{48} + (V_{40} - V_{48}) \times 7/8$	$V_{24} + (V_{16} - V_{24}) \times 2/8$
A	$V_{16} + (V_8 - V_{16}) \times 6/8$	$V_{56} + (V_{48} - V_{56}) \times 3/8$	2A	$V_{48} + (V_{40} - V_{48}) \times 6/8$	$V_{24} + (V_{16} - V_{24}) \times 3/8$
B	$V_{16} + (V_8 - V_{16}) \times 5/8$	$V_{56} + (V_{48} - V_{56}) \times 4/8$	2B	$V_{48} + (V_{40} - V_{48}) \times 5/8$	$V_{24} + (V_{16} - V_{24}) \times 4/8$
C	$V_{16} + (V_8 - V_{16}) \times 4/8$	$V_{56} + (V_{48} - V_{56}) \times 5/8$	2C	$V_{48} + (V_{40} - V_{48}) \times 4/8$	$V_{24} + (V_{16} - V_{24}) \times 5/8$
D	$V_{16} + (V_8 - V_{16}) \times 3/8$	$V_{56} + (V_{48} - V_{56}) \times 6/8$	2D	$V_{48} + (V_{40} - V_{48}) \times 3/8$	$V_{24} + (V_{16} - V_{24}) \times 6/8$
E	$V_{16} + (V_8 - V_{16}) \times 2/8$	$V_{56} + (V_{48} - V_{56}) \times 7/8$	2E	$V_{48} + (V_{40} - V_{48}) \times 2/8$	$V_{24} + (V_{16} - V_{24}) \times 7/8$
F	$V_{16} + (V_8 - V_{16}) \times 1/8$	V_{48}	2F	$V_{48} + (V_{40} - V_{48}) \times 1/8$	V_{16}
10	V_{16}	$V_{48} + (V_{40} - V_{48}) \times 1/8$	30	V_{48}	$V_{16} + (V_8 - V_{16}) \times 1/8$
11	$V_{24} + (V_{16} - V_{24}) \times 7/8$	$V_{48} + (V_{40} - V_{48}) \times 2/8$	31	$V_{56} + (V_{48} - V_{56}) \times 7/8$	$V_{16} + (V_8 - V_{16}) \times 2/8$
12	$V_{24} + (V_{16} - V_{24}) \times 6/8$	$V_{48} + (V_{40} - V_{48}) \times 3/8$	32	$V_{56} + (V_{48} - V_{56}) \times 6/8$	$V_{16} + (V_8 - V_{16}) \times 3/8$
13	$V_{24} + (V_{16} - V_{24}) \times 5/8$	$V_{48} + (V_{40} - V_{48}) \times 4/8$	33	$V_{56} + (V_{48} - V_{56}) \times 5/8$	$V_{16} + (V_8 - V_{16}) \times 4/8$
14	$V_{24} + (V_{16} - V_{24}) \times 4/8$	$V_{48} + (V_{40} - V_{48}) \times 5/8$	34	$V_{56} + (V_{48} - V_{56}) \times 4/8$	$V_{16} + (V_8 - V_{16}) \times 5/8$
15	$V_{24} + (V_{16} - V_{24}) \times 3/8$	$V_{48} + (V_{40} - V_{48}) \times 6/8$	35	$V_{56} + (V_{48} - V_{56}) \times 3/8$	$V_{16} + (V_8 - V_{16}) \times 6/8$
16	$V_{24} + (V_{16} - V_{24}) \times 2/8$	$V_{48} + (V_{40} - V_{48}) \times 7/8$	36	$V_{56} + (V_{48} - V_{56}) \times 2/8$	$V_{16} + (V_8 - V_{16}) \times 7/8$
17	$V_{24} + (V_{16} - V_{24}) \times 1/8$	V_{40}	37	$V_{56} + (V_{48} - V_{56}) \times 1/8$	V_8
18	V_{24}	$V_{40} + (V_{32} - V_{40}) \times 1/8$	38	V_{56}	$V_8 + (V_0 - V_8) \times 1/8$
19	$V_{32} + (V_{24} - V_{32}) \times 7/8$	$V_{40} + (V_{32} - V_{40}) \times 2/8$	39	$V_{64} + (V_{56} - V_{64}) \times 7/8$	$V_8 + (V_0 - V_8) \times 2/8$
1A	$V_{32} + (V_{24} - V_{32}) \times 6/8$	$V_{40} + (V_{32} - V_{40}) \times 3/8$	3A	$V_{64} + (V_{56} - V_{64}) \times 6/8$	$V_8 + (V_0 - V_8) \times 3/8$
1B	$V_{32} + (V_{24} - V_{32}) \times 5/8$	$V_{40} + (V_{32} - V_{40}) \times 4/8$	3B	$V_{64} + (V_{56} - V_{64}) \times 5/8$	$V_8 + (V_0 - V_8) \times 4/8$
1C	$V_{32} + (V_{24} - V_{32}) \times 4/8$	$V_{40} + (V_{32} - V_{40}) \times 5/8$	3C	$V_{64} + (V_{56} - V_{64}) \times 4/8$	$V_8 + (V_0 - V_8) \times 5/8$
1D	$V_{32} + (V_{24} - V_{32}) \times 3/8$	$V_{40} + (V_{32} - V_{40}) \times 6/8$	3D	$V_{64} + (V_{56} - V_{64}) \times 3/8$	$V_8 + (V_0 - V_8) \times 6/8$
1E	$V_{32} + (V_{24} - V_{32}) \times 2/8$	$V_{40} + (V_{32} - V_{40}) \times 7/8$	3E	$V_{64} + (V_{56} - V_{64}) \times 2/8$	$V_8 + (V_0 - V_8) \times 7/8$
1F	$V_{32} + (V_{24} - V_{32}) \times 1/8$	V_{32}	3F	$V_{64} + (V_{56} - V_{64}) \times 1/8$	V_0

(5) γ (gamma) correction value

Between reference voltage input pin VH_0 and VH_{64}, 64 resistors are connected in series. And between reference voltage input pin VL_0 and VL_{64}, 64 resistors are connected in series. And between reference voltage input pin VH_{64} and VL_{64}, a resistor isn't connected. The γ correction curve is broken line connected between intermediate voltage input (VH_8, VH_{16}, VH_{24}, VH_{32}, VH_{40}, VH_{48}, VH_{56}, VL_8, VL_{16}, VL_{24}, VL_{32}, VL_{40}, VL_{48} and VL_{56}). Between the intermediate voltage input. it is individed into 8 parts by the same resistor.

LH168B/LH168G



The following shows the ratio of g correction resistance, when R0 equals 1.

R0	1.00
R1	0.50
R2	0.50
R3	0.50
R4	0.50
R5	0.50
R6	0.50
R7	1.00

R8	1.00
R9	0.50
R10	0.50
R11	0.50
R12	0.50
R13	0.50
R14	0.50
R15	1.00

■ Absolute Maximum Ratings

Parameter		Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	V_{CC}	Ta = 25 °C	–0.3 to +7.0	V
	V_{LS}	V_{LS}	Ta = 25 °C	–0.3 to +15.0	V
Input voltage	VH_0-VL_0	V_I	Ta = 25 °C	–0.3 to V_{LS} + 0.3	V
	Other	V_I	Ta = 25 °C	–0.3 to V_{CC} + 0.3	V
Output voltage	SPIO, SPOI	V_O	Ta = 25 °C	–0.3 to V_{CC} + 0.3	V
	XO_1-ZO_{108}	V_O	Ta = 25 °C	–0.3 to V_{LS} + 0.3	V
Storage temperature		T_{stg}		–45 to +125	°C

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{CC}	2.7		3.6	V	
	V_{LS}	8.0		13.0	V	
Reference voltage input	VH_0-VH_{64}	0.5V_{LS}		V_{LS} – 0.1	V	1
	VL_0-VL_{64}	+0.1		0.5V_{LS}	V	
Clock frequency	f_{CK}			55	MHz	
LCD drive output load capacity	C_L			150	pF	
Operating temperature	T_{opr}	–20		75	°C	

Note 1. Observe the following relation for the potential of the reference voltage input.
$V_{LS} > VH_0 > VH_8 > VH_{16} > VH_{24} > VH_{32} > VH_{40} > VH_{48} > VH_{56} > VH_{64} \geq 0.5V_{LS} \geq VL_{64} > VL_{56} > VL_{48} > VL_{40} > VL_{32} > VL_{24} > VL_{16} > VL_8 > VL_0 > GND$

Note 2. Observe the following sequence of switching power supply on the device.
V_{CC} → Logic input → V_{LS}, VH_0-VH_{64}, VL_{64}-VL_0
Observe the contrary sequence of switching power supply off the device.

■ DC Electrical Characteristics

(V_{CC} = 2.7 to 3.6 V, V_{LS} = 8.0 to 13 V, Ta = –20 to +75 °C)

Parameter	Symbol	Measuring condition	Applicable pin	MIN.	TYP.	MAX.	Unit
Input "Low" current	I_{ILL}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR, REV, REV_2, POLA, POLB, MODE, PBS			10	µA
Input "High" current	I_{ILH1}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR, REV, MODE, PBS			10	µA
	I_{ILH2}		POLA, POLB, REV_2			400	µA
Input "Low" voltage	V_{IL}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR, REV, REV_2, POLA, POLB, MODE, PBS	GND		0.3V_{CC}	V
Input "High" voltage	V_{IH}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR, REV, REV_2, POLA, POLB, MODE, PBS	0.7V_{CC}		V_{CC}	V
Output "Low" voltage	V_{OL}	I_{OL} = 0.3 mA	SPIO	GND		GND + 0.4	V
Output "High" voltage	V_{OH}	I_{OH} = –0.3 mA	SPOI	V_{CC} – 0.4		V_{CC}	V
Current consumption (In operation mode)	I_{CC1}	*1	V_{CC} – GND			12	mA
Current consumption (Instandby mode)	I_{CC2}	*2	V_{CC} – GND			4.0	mA
Current consumption (In operation mode)	I_{LS1}	*1	V_{LS} – GND			8.0	mA
Current consumption (In standby mode)	I_{LS2}	*2	V_{LS} – GND			7.0	mA
Output voltage range	V_{OUT}		XO_1 – ZO_{108}	GND + 0.2		V_{LS} – 0.2	V
Deviations between output voltage pins	V_{OD}			–20		+20	mV
Output current	I_{O1}-I_{O4}	*3			200		µA
Resistance between reference power supplies	R_{GMAH}		Between VH_0 and VH_{64}		20		kΩ
	R_{GMAL}		Between VL_0 and VL_{64}		20		kΩ

[Measuring condition]

*1 f_{CK} = 55 MHz, f_{LS} = 50 kHz (Data sampling state)

*2 f_{CK} = 55 MHz, f_{LS} = 50 kHz, SPI = GND is fixed. (Standby state)

*3 ○I_{O1}
- Applied voltage = 8.0 V for output pins XO_1-ZO_{108}
- Output voltage = 7.5 V for output pins XO_1-ZO_{108}
- V_{LS} = 10V

○I_{O2}
- Applied voltage = 7.0 V for output pins XO_1-ZO_{108}
- Output voltage = 7.5 V for output pins XO_1-ZO_{108}
- V_{LS} = 10V

○I_{O3}
- Applied voltage = 3.0 V for output pins XO_1-ZO_{108}
- Output voltage = 2.5 V for output pins XO_1-ZO_{108}
- V_{LS} = 10V

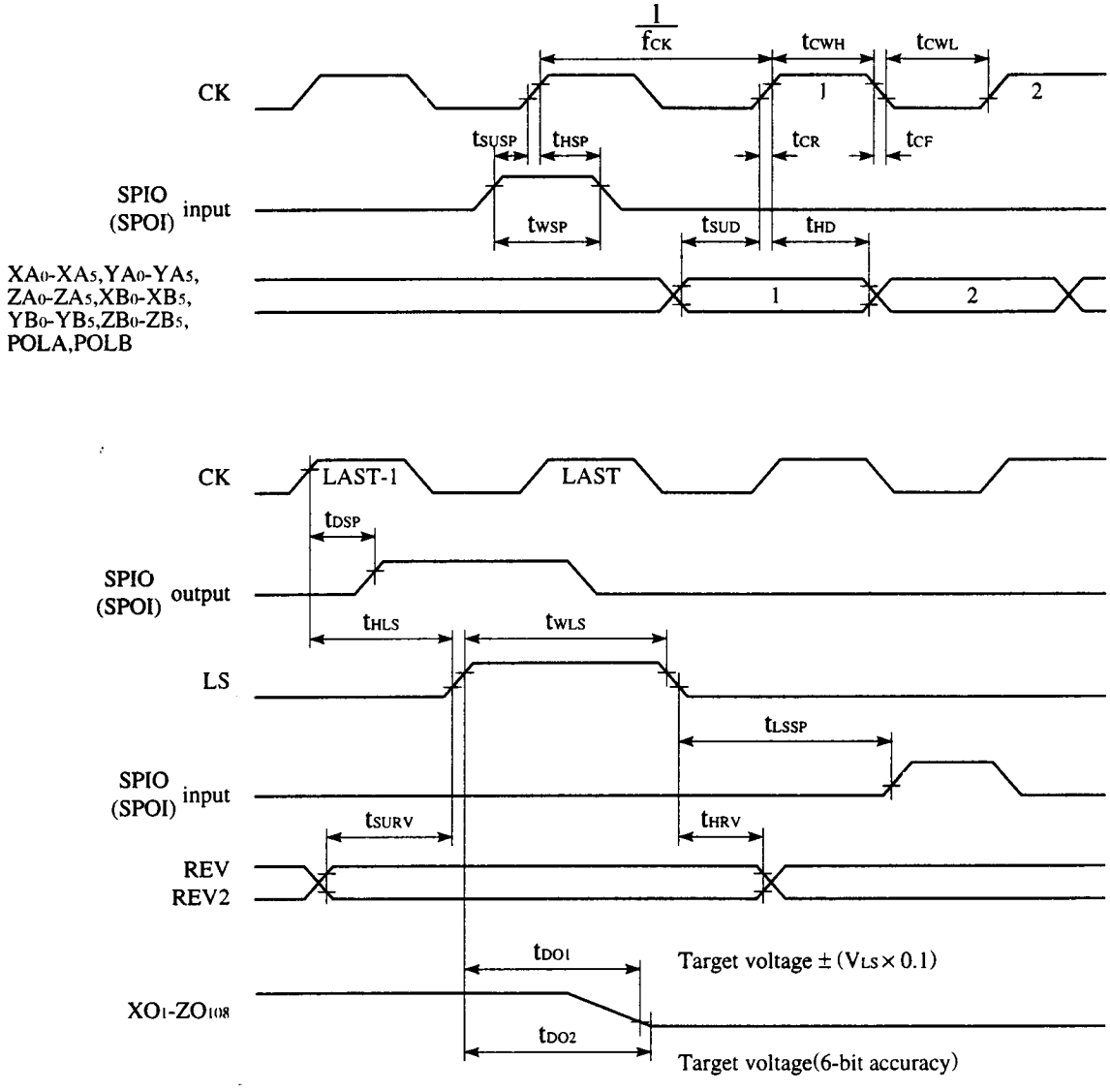
○I_{O4}
- Applied voltage = 2.0 V for output pins XO_1-ZO_{108}
- Output voltage = 2.5 V for output pins XO_1-ZO_{108}
- V_{LS} = 10 V

■ AC Electrical Characteristics

(V_{CC} = 2.7 to 3.6 V, V_{LS} = 8.0 to 13 V, Ta = –20 to +75 °C)

Parameter	Symbol	Measuring condition	Applicable pin	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{CK}		CK			55	MHz
"High" level pulse width	t_{CWH}			4.0			ns
"Low" level pulse width	t_{CWL}			4.0			ns
Input rise time	t_{CR}					10	ns
Input fall time	t_{CF}					10	ns
Data setup time	t_{SUD}		XA_0-XA_5, XB_0-XB_5, YA_0-YA_5, YB_0-YB_5, ZA_0-ZA_5, ZB_0-ZB_5, POLA, POLB	4.0			ns
Data hold time	t_{HD}			0			ns
Start pulse setup time	t_{SUSP}		SPIO, SPOI	4.0			ns
Start pulse hold time	t_{HSP}		SPIO, SPOI	0			ns
Start pulse width	t_{WSP}		SPIO, SPOI			$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t_{DSP}	C_L = 15 pF	SPIO, SPOI			12	ns
LCD drive output delay time	t_{DO1}	C_L = 150 pF	XO_1-XO_{108}			3	µs
	t_{DO2}	C_L = 150 pF				10	µs
LS signal, SPI signal setup time	t_{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal, CK signal hold time	t_{HLS}		LS	7			ns
LS signal "High" level width	t_{WLS}		LS	$\frac{1}{f_{CK}}$			ns
REV signal, LS signal setup time	t_{SURV}		REV, REV_2	14			ns
REV signal, LS signal hold time	t_{HRV}		REV, REV_2	10			ns

■ Timing Diagram



■ Example of Typical Characteristics

(Ta = 25 °C, GND = 0 V, Vcc = 3.3 V)

Parameter	MIN.	TYP.	MAX.	Unit
Basic gate propagation delay time		10		ns

■ Sharp's Product Line-up (TFT LCD Driver)

★ Under development

Model No.	Display panel	Drive function	Gray scale	Output	Display (V) MAX.	Clock frequency (Hz) MAX.	Supply voltage (V)	Description	Package
LH1689F	for OA (VGA)	Source	64-scale (6-bit)	240	5.5	55M	3.0 to 5.5	Built-in reference voltage generation circuit, R-DAC system	SST
LH1685F	for OA (SVGA/XGA)	Source	64-scale (6-bit)	309/300	5.5	55M	3.0 to 5.5	Built-in reference voltage generation circuit, R-DAC system	SST
LH168BF LH168GF	for OA (XGA)	Source	64-scale (6-bit)	324/312	13	55M	2.7 to 3.6	Dot inversion drive, Built-in reference voltage generation circuit	SST
LH168DF LH168JF	for OA (XGA/SXGA)	Source	64-scale (6-bit)	384	13	65M	2.7 to 3.6	Dot inversion drive, Built-in reference voltage generation circuit	SST
★ LH168EF	for OA (XGA/SXGA)	Source	256-scale (8-bit)	384	13	65M	2.7 to 3.6	Dot inversion drive, Built-in reference voltage generation circuit	SST
★ LH168AF	for OA (SVGA/XGA)	Source	64-scale (6-bit)	384	5.5	55M	2.7 to 3.6	2-port data input, Built-in reference voltage generation circuit, R-DAC system	SST
LH1684F	for AV	Source	Analog	240	5.5	10M	4.5 to 5.5	Three-point simultaneous or sequential sampling selectable. Sampling frequency : 20 MHz	SST
★ LH1687F	for AV	Source	Analog	240	5.5	12.5M	3.0 to 5.5	Three-point simultaneous or sequential sampling selectable. Sampling frequency : 25 MHz, Power save function	SST
LH1691F	for OA/AV (VGA)	Gate	—	240	33	100k	3.0 to 5.5	1-pulse (normal) or 2-pulse (normal/precharge) scanning selectable Both positive/negative power supply capability	SST
LH1692F	for OA (SVGA)	Gate	—	300	42	100k	3.0 to 5.5	1-pulse (normal) or 2-pulse (normal/precharge) scanning selectable Both positive/negative power supply capability	SST
LH1694F	for OA (XGA/SXGA)	Gate	—	256	42	100k	2.7 to 3.6	1-pulse (normal) or 2-pulse (normal/precharge) scanning selectable Both positive/negative power supply capability, Enable chain cascade connection	SST

SHARP

SHARP CORPORATION Japan

HEAD OFFICE
SALES & MARKETING GROUP
-ELECTRONIC COMPONENTS & DEVICES
22-22, NAGAIKE-CHO, ABENO-KU, OSAKA 545, JAPAN
PHONE: (81) 6-621-1221
FAX: (81) 6117-725300, 6117-725301, 6117-725302
http : //www.sharp.co.jp/e-device/index.html

IC SALES DEPARTMENT
INTERNATIONAL IC SALES DEPARTMENT II
2613-1 ICHINOMOTO-CHO TENRI-CITY NARA 632, JAPAN
PHONE: (81) 743-65-1321
FAX: (81) 743-65-1532

U.S.A.

SHARP ELECTRONICS CORPORATION
Microelectronics Group

North American Head Office
5700 Northwest Pacific Rim Blvd. #20,
Camas, WA 98607, U.S.A.
PHONE: (1)360-834-2500
FAX : (1)360-834-8903
http : //www.sharpmeg.com

West
1980 Zanker Road, San Jose, CA 95112
PHONE: (1)408-436-4900
FAX : (1)408-436-0924

5901 Bolsa Ave.,
Huntington Beach, CA 92647
PHONE: (1)714-250-0225
FAX : (1)714-250-0438

1025 Royal Lane (PO box 619035),
DFW Airport, TX 75261-9035
PHONE: (1)972-574-5205
FAX : (1)972-574-9870

10222 Scull Creek, Austin, TX 78730
PHONE: (1)512-349-7262
FAX : (1)512-349-7002

9950 Cypresswood, Suite 350,
Houston, TX 77070
PHONE: (1)281-955-9909
FAX : (1)281-955-9910

East
1300 Naperville Road, Romeoville, IL 60446
PHONE: (1)630-226-2400
FAX : (1)630-759-8572

691 N. Squirrel Road, Suite 110,
Auburn Hills, MI 48326
PHONE: (1)810-377-9220
FAX : (1)810-377-9222

200 Wheeler Rd., Burlington, MA 01803
PHONE: (1)617-270-7979
FAX : (1)617-229-9117

Canterbury Hall, 4815 Emperor Blvd.,
Suite 140, Durham, NC 27703
PHONE: (1)919-941-0065
FAX : (1)919-941-0066

EUROPE

SHARP ELECTRONICS (EUROPE) GmbH

Head Office
Microelectronics Division, (MED)
Sonninstrasse 3, 20097, Hamburg, Germany
PHONE: (49)40-23 76 22 86
FAX : (49)40-23 76 22 32

Germany MED Muenchen Office
Fuerstenr lederstrasse 5,
80687 Muenchen, Germany
PHONE: (49)89-54-6842-0
FAX : (49)89-54-6842-50

Germany MED Nürnberg Office
Donaustrasse 69, 90451 Nürnberg, Germany
PHONE: (49)911-642 70 51
FAX : (49)911-642 66 69

France MED Paris Office
Immeuble Rosny 2, Avénue du
Général de Gaulle 93110
Rosny Sous Bois Cédex, France
PHONE: (33)1-48 12 19 00
FAX : (33)1-48 55 46 78

Italy MED Milano Office
Centro Direzionale Colleoni
Palazzo Taurus Ingresso 2
20041 Agrate Brianza, Milano, Italy
PHONE: (39)39-68 99 946
FAX : (39)39-68 99 948

U.K. MED London Office
Centennial Court, Easthampstead Road,
Bracknell, Berkshire RG12 1YQ,
United Kingdom
PHONE: (44)1344-86 99 22
FAX : (44)1344-36 09 03

U.K. MED Scotland Office
Unit 48 Grovewood Business Centre,
Strathclyde Business Park,
Bellshill ML43NQ,
Scotland, United Kingdom
PHONE: (44)1698-84 34 42
FAX : (44)1698-84 28 99

Ireland MED Dublin Office
First Floor, Block 1, St. Johns Court,
Santry, Dublin 9, Ireland
PHONE: (353)1-842 87 05
FAX : (353)1-842 84 55

ASIA

SHARP-ROXY (HONG KONG) LTD.
3rd Business Division,
17/F, Admiralty Centre,
Tower 1, 18 Harcourt Road, Hong Kong
PHONE: (852)28229311
FAX : (852)28660779

SHARP ELECTRONICS (SINGAPORE) PTE., LTD.
Electronic Components Division
438A Alexandra Road #05-01/02
Alexandra Technopark
Singapore 119967
PHONE: (65)271-3566
FAX : (65)271-3855

SHARP ELECTRONIC COMPONENTS (TAIWAN) CORPORATION
8F-A, No. 16, Sec. 4, Nanking E. Rd.,
Taipei, Taiwan, Republic of China
PHONE: (886)2-577-7341
FAX : (886)2-577-7326, (886)2-577-7328

SHARP ELECTRONIC COMPONENTS (KOREA) CORPORATION
RM 501 Geosung B/D, 541,
Dohwa-dong, Mapo-ku, Seoul, Korea
PHONE: (82)2-711-5813 to 5818
FAX : (82)2-711-5819

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