

SHARP

NEW PRODUCT
INFORMATION
PRELIMINARY

LH101504 High-Speed BiCMOS 256K (64K×4) ECL Static RAM
LH101510 High-Speed BiCMOS 1M (1M×1) ECL Static RAM

■ Description

The LH101504/LH101510 is a 256K/1M-bit high speed BiCMOS ECL static RAM organized as 64K×4 and 1M×1 respectively, fully compatible with ECL 101K I/O levels. It is fabricated using 0.8 μ m design rule and features advanced circuit technology that result in high speed access times.

Designed for high speed applications, it is applicable to the main memory of super computers and the cache memory of high performance work stations.

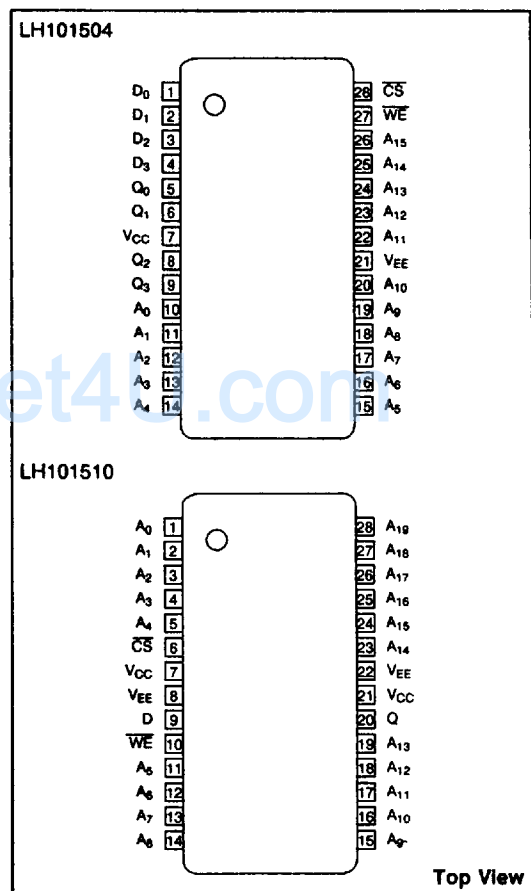
■ Features

- 0.8 μ m BiCMOS process
- Memory organization
65,536 × 4 bits (LH101504)
1,048,576 × 1 bit (LH101510)
- Access times:
7/8/10ns MAX. (LH101504)
8/10/12ns MAX. (LH101510)
- Balanced read and write cycle times
- Power consumption:
1.6W MAX. $f_0 = 100$ MHz (LH101504)
1.4W MAX. $f_0 = 100$ MHz (LH101510)
- Fully 101K compatible ECL I/O
- Power supply: $-5.2V \pm 10\%$
- Package: 28-pin ceramic flat package

■ Pin Description

Signal		Pin name
LH101504	LH101510	
A ₀ -A ₁₅	A ₀ -A ₁₉	Address inputs
Q ₀ -Q ₃	Q	Data output
D ₀ -D ₃	D	Data input
CS		Chip select
WE		Write enable
V _{EE}		Power supply
V _{CC}		Ground

■ Pin Connections



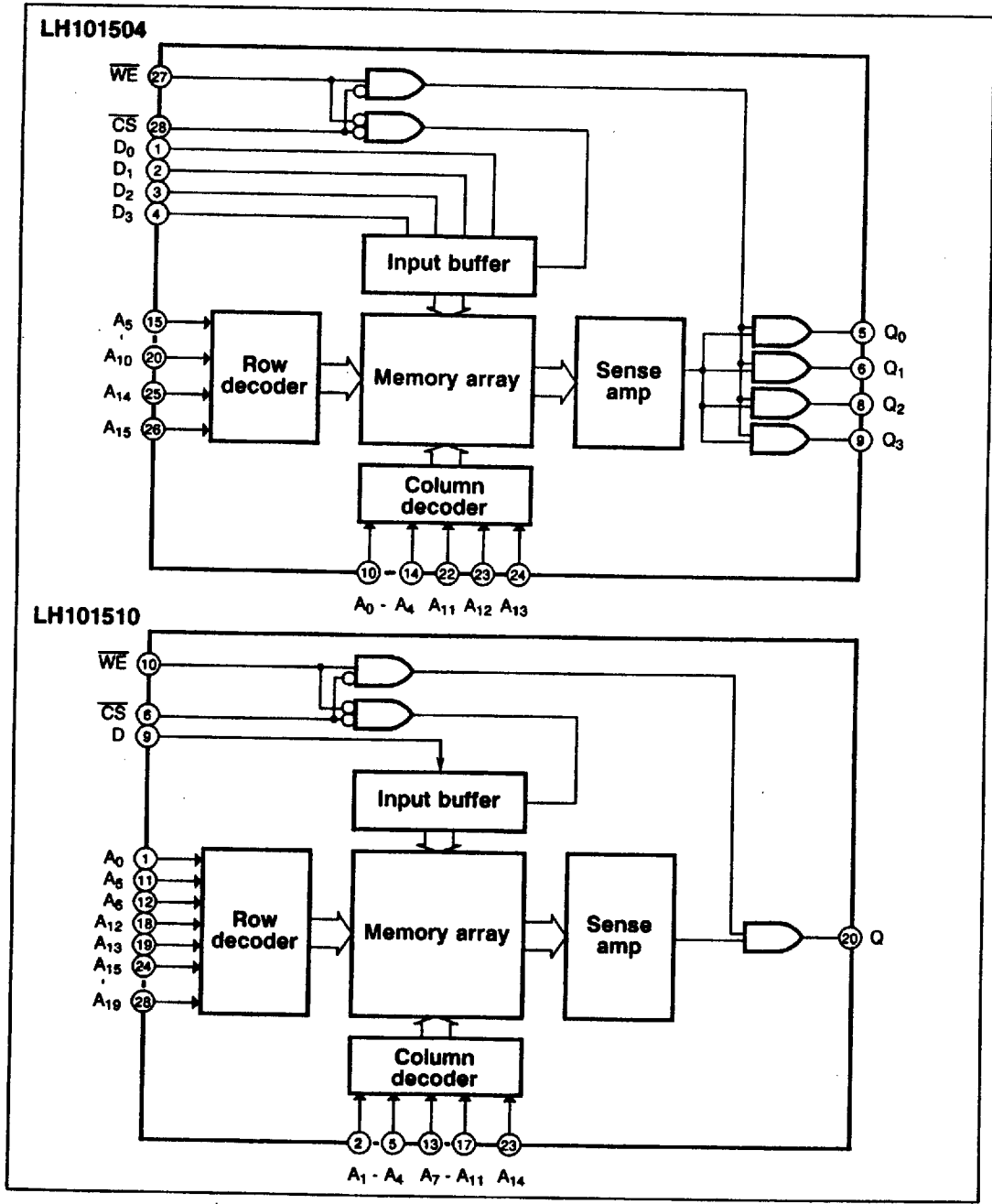
■ Truth Table

CS	WE	D	Q	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	Q	Read

LH101504
LH101510

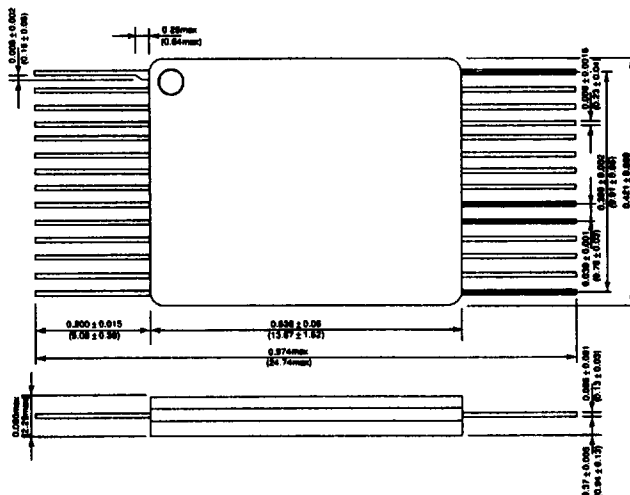
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High-Speed BiCMOS 1M (1M×1) ECL Static RAM

■ Block Diagrams

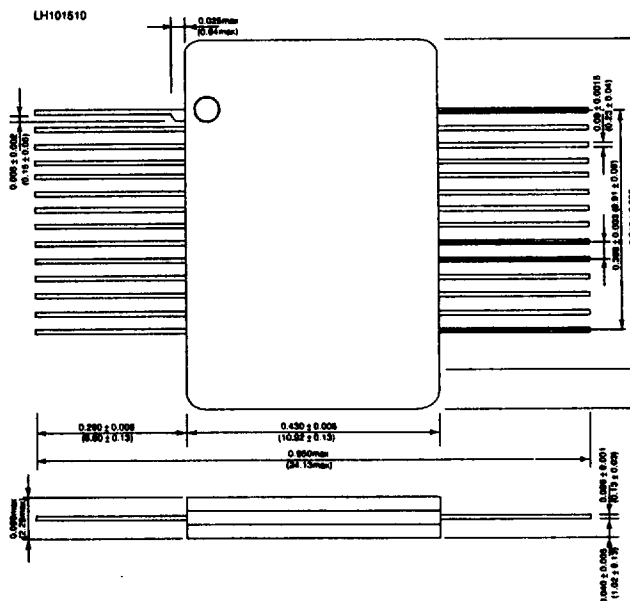


■ Package Dimensions (28-pin ceramic flat package)

LH101504



LH101510



Dimensions in inches (mm)

LH101504 High-Speed BICMOS 256K (64K×4) ECL Static RAM
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■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
VEE pin potential to ground	VEE	- 7.0 to + 0.0	V
Input voltage (DC)	V _{IN}	VEE to + 0.0	V
Output current (DC output HIGH)	I _{OH}	- 50	mA
Operating temperature	T _{opr}	0 to + 85	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Maximum junction temperature	T _j	+ 150	°C

■ DC Characteristics

(T_c = 0 to + 85°C, V_{CC} = Ground, V_{EE} = - 5.2V ± 10%)

Parameter	Symbol	Test Condition	MIN.	MAX.	Unit
Output HIGH voltage	V _{OH}	V _{IN} = V _{IH} (MAX.) or V _{IL} (MIN.)	- 1025	- 880	mV
Output LOW voltage	V _{OL}	Loading with 50 ohms to - 2.0V	- 1810	- 1620	mV
Input HIGH voltage	V _{IH}		- 1165	- 880	mV
Input LOW voltage	V _{IL}		- 1810	- 1475	mV
Output HIGH voltage	V _{OHC}	V _{IN} = V _{IH} (MIN.) or V _{IL} (MAX.)	- 1025		mV
Output LOW voltage	V _{OLC}	Loading with 50 ohms to - 2.0V		- 1620	mV
Input HIGH current	I _{IH}	V _{IN} = V _{IH} (MAX.)		220	μA
Input LOW current	I _{IL}	V _{IN} = V _{IL} (MAX.)	- 50	170	μA
Power supply current	I _{EE}	f _O = 100MHz	LH101504	- 270	mA
			LH101510	- 240	

Note: T_c = Case Temperature

■ Capacitance (Note 1)

Parameter	Symbol	LH101504		LH101510		Unit
		MIN.	MAX.	MIN.	MAX.	
Input capacitance	C _{IN}		5.0		7.0	pF
Output capacitance	C _{OUT}		8.0		8.0	pF

Note 1: Sample tested only

■ Switching Characteristics Read Cycle

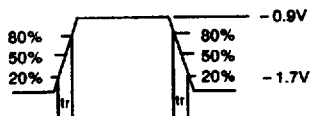
$V_{EE} = -5.2V \pm 10\%$, $V_{CC} = \text{Ground}$, $T_c = 0^\circ\text{C}$ to $+85^\circ\text{C}$

Parameter	Symbol	LH101504N-07		LH101510N-08		LH101510N-10		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Address valid to address invalid	TAVAX	7		8		10		ns
Address valid to output valid	TAVQV		7		8		10	ns
Address invalid to output invalid	TAXQX	4	7	5	7	5	8	ns
Chip select LOW to chip select HIGH	TELEH	4		5		6		ns
Chip select LOW to output valid	TELOV		4		4		4	ns
Chip select HIGH to output LOW	TEHQL		4		4		4	ns
Write cycle 1								
Address valid to address invalid	TAVAX	7		8		10		ns
Write enable LOW to chip select HIGH	TWLEH	4		5		6		ns
Write HIGH to address don't care	TWHAX	0		0		0		ns
Write LOW to write HIGH (Setup & holds)	TWLWH	4		5		6		ns
Address valid to write LOW	TAVWL	0		0		0		ns
Data valid to write HIGH	TDVWH	4		5		6		ns
Write HIGH to data don't care	TWHDX	0		0		0		ns
Write LOW to output LOW	TWLQL		4		4		4	ns
Write HIGH to output valid	TWHQV		7		8		10	ns
Write cycle 2								
Address valid to chip select LOW	TAVEL	0		0		0		ns
Chip select LOW to chip select HIGH	TELEH	4		5		6		ns
Chip select HIGH to address don't care	TEHAX	0		0		0		ns
Chip select LOW to write enable HIGH	TELWH	4		5		6		ns
Data valid to chip select HIGH	TDVEH	4		5		6		ns
Chip select HIGH to data don't care	TEHDX	0		0		0		ns
Consecutive write cycle								
Write enable HIGH to write enable LOW	TWHWL	4		4		4		ns
Chip select HIGH to chip select LOW	TEHEL	4		4		4		ns

Note: T_c = Case Temperature

■ AC Test Conditions

Input rise and fall times	1.5ns
Output reference levels	-1.33V
Input reference levels	-1.33V
AC test circuit	Figure 2



tr = Rise Time
tr = Fall Time
50% = Timing Reference

Figure 1

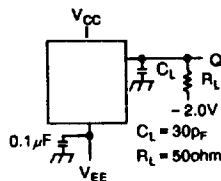


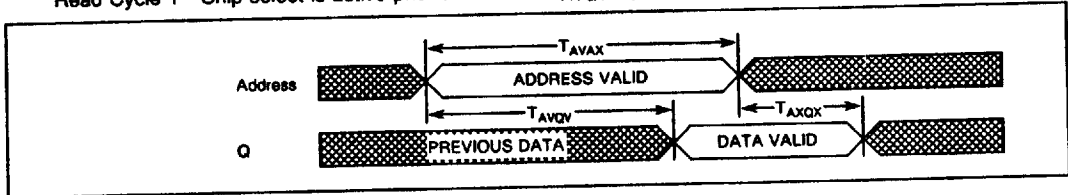
Figure 2 AC Test Circuit

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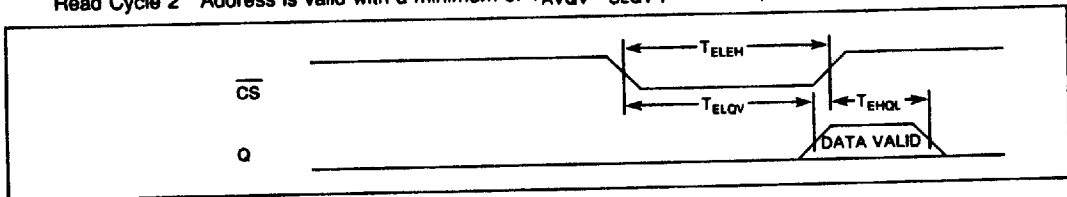
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■ **Timing Diagram**

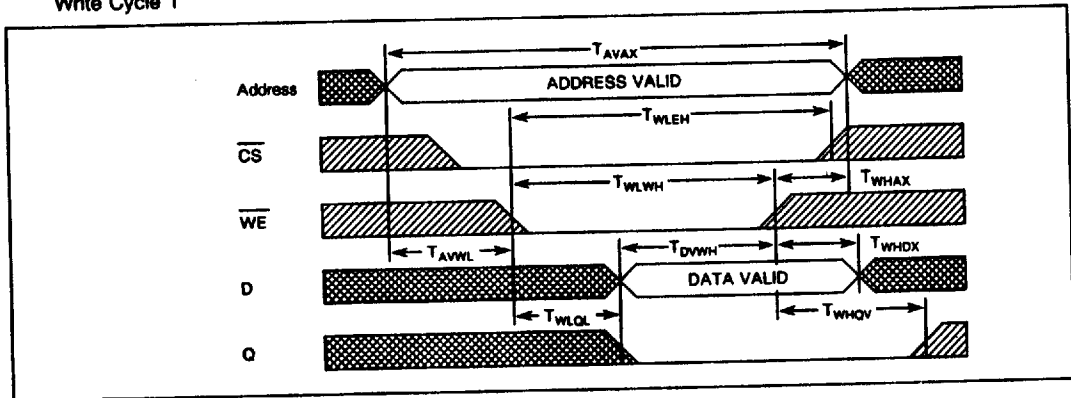
Read Cycle 1 Chip select is active prior to or within T_{AVQV} - T_{SLOW} after address valid.



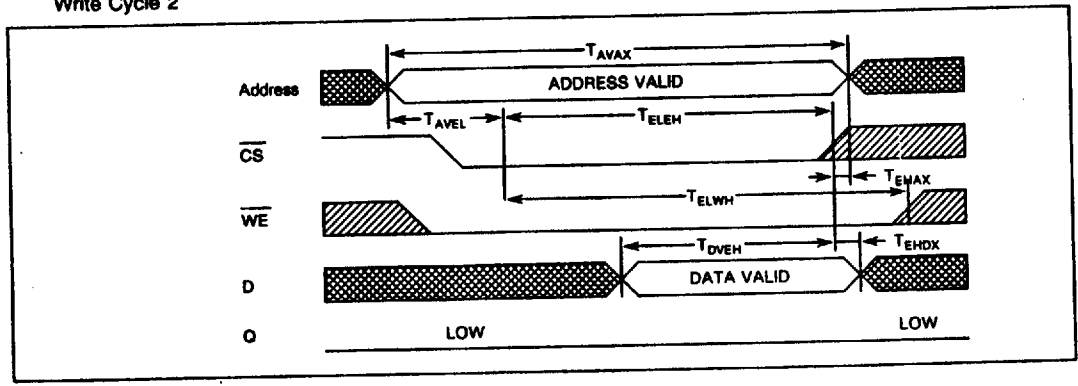
Read Cycle 2 Address is valid with a minimum of T_{AVQV} - T_{SLOW} prior to chip select becoming active.



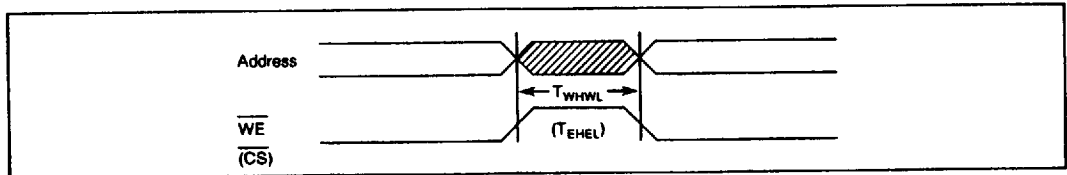
Write Cycle 1



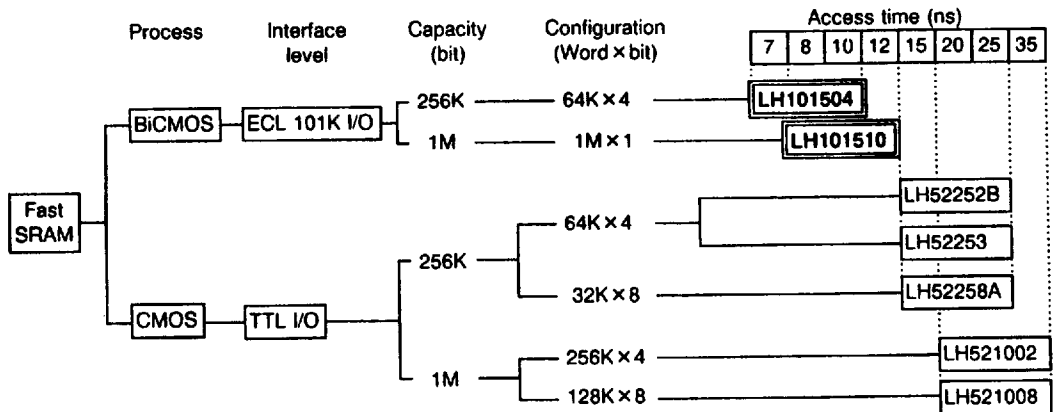
Write Cycle 2



Consecutive Write Cycle (Minimum write (select) pulse disable)



■ Sharp's Product Lineup (Fast SRAM)



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■ Ordering Information

LH101504 X - XX

- Access times
 - 08: 8ns
 - 10: 10ns
 - 12: 12ns
- Package
 - N: 28-pin ceramic flat package
- Model No.
 - 256K (64K×4) bit ECL I/O static RAM

LH101510 X - XX

- Access times
 - 07: 7ns
 - 08: 8ns
 - 10: 10ns
- Package
 - N: 28-pin ceramic flat package
- Model No.
 - 1M (1M×1) bit ECL I/O static RAM

■ Development Schedule	(LH101504)	(LH101510)
Sample	May, '92	July, '92
Mass Production Start	August, '92	October, '92

The information described herein is intended to introduce descriptions for products that are in development, and specifications and circuitry are subject to change upon final characterization.

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