

SHARP

LH168D/LH168J

384 Outputs 64 Gradations
TFT-LCD Source Driver

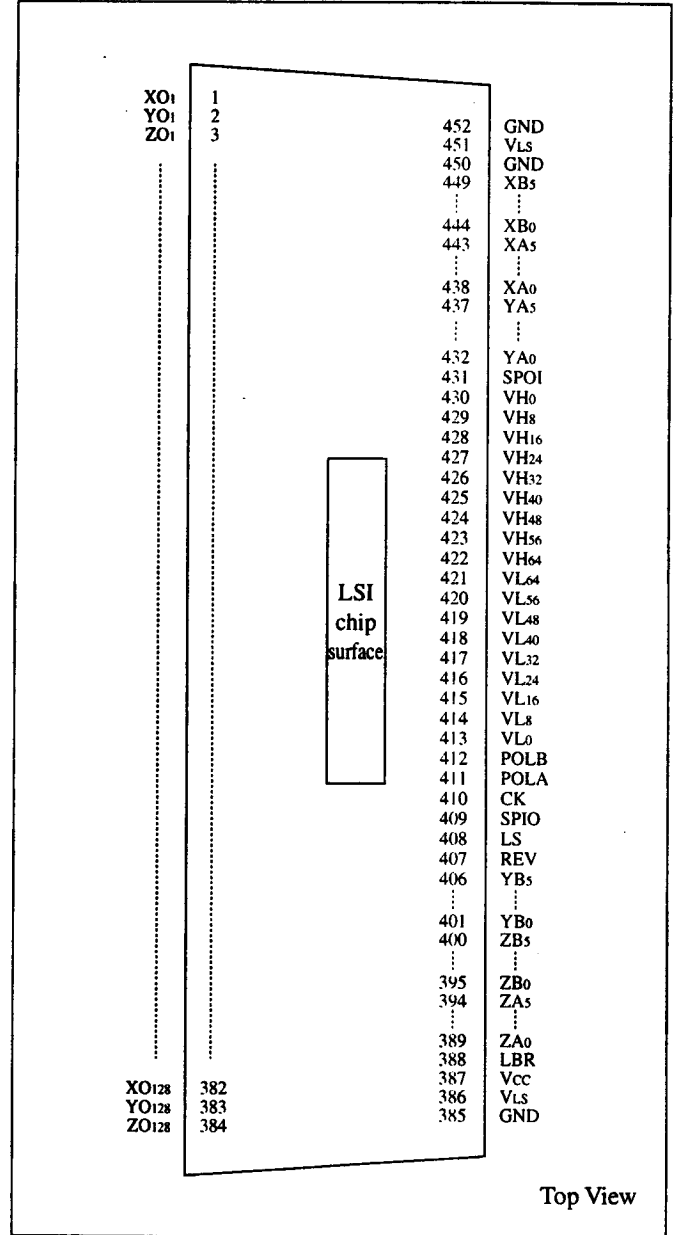
■ Description

The LH168D/LH168J are a source driver with 384 LCD drive outputs, and are used for the TFT LCD unit which can simultaneously display 262 144 colors in 64 gradations.

■ Features

1. The LH168D/LH168J are a driver which incorporates a 6-bit digital input DAC.
2. The LH168D/LH168J are a Dot-Inversion driver that the LCD drive pin inverted gradational voltage at the next LCD drive pins.
3. The number of LCD drive outputs is 384 outputs.
4. Each circuits of data input R, G and B have two port inputs. They can sample & hold display data of two pixels at the sametime.
5. The basic voltage input of 18 gradations can display 262 144 colors in 64 gradations. This basic voltage input corresponds to γ correction and the intermediate basic voltage input can be abbreviated.
6. Shift clock frequency is 65 MHz (MAX.).
7. The LH168D/LH168J have the function of cascade connection.
8. It is possible to switch the output directivity of LCD drive output.
($XO_1, YO_1, ZO_1 \rightarrow XO_{128}, YO_{128}, ZO_{128}$ and $ZO_{128}, YO_{128}, XO_{128} \rightarrow ZO_1, YO_1, XO_1$)
9. Supply voltage V_{CC} for the digital system : 2.7 to 3.6 V
10. Supply voltage V_{LS} for the analog system : 8.0 to 13.0 V
11. Package SST

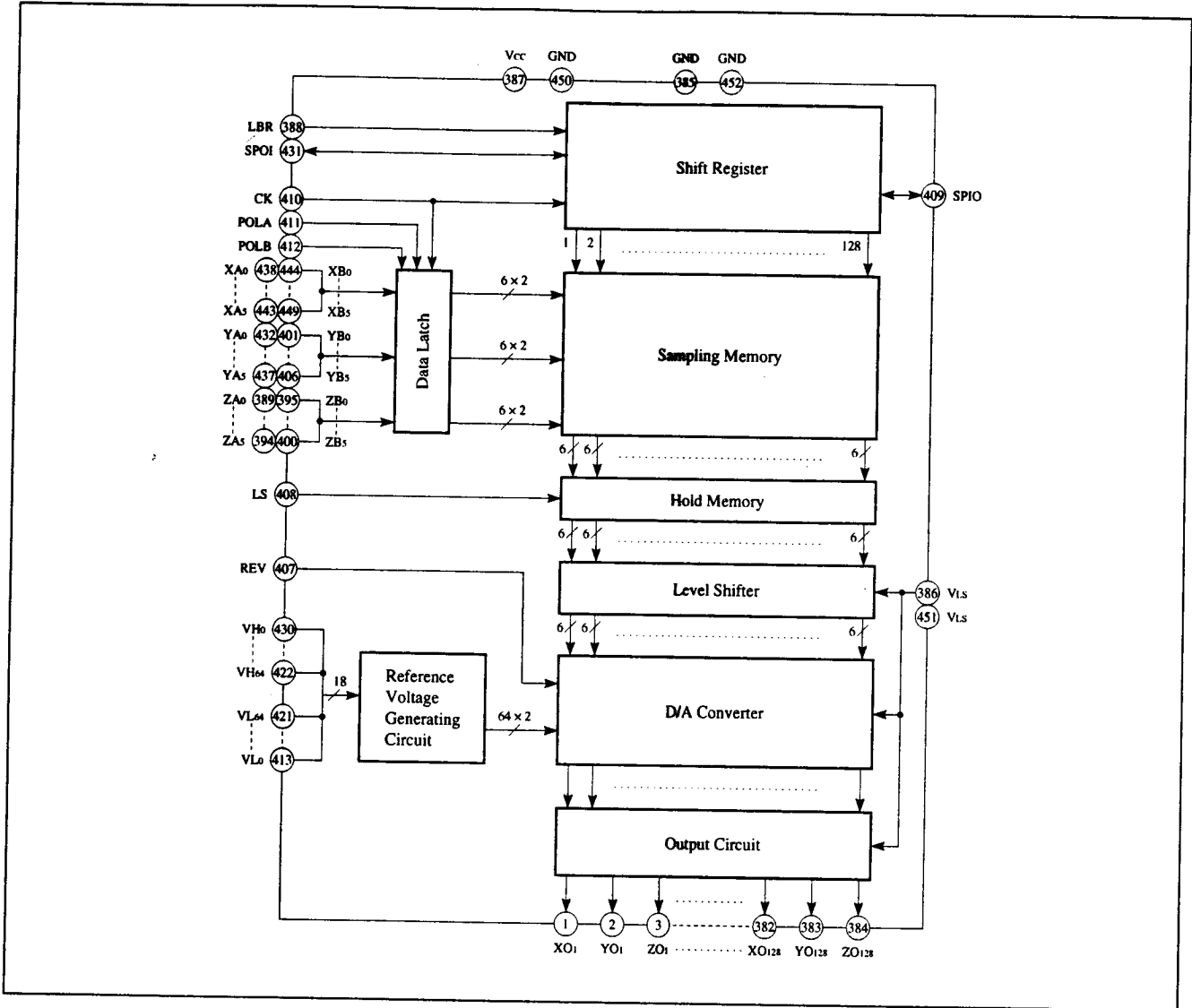
■ Pin Connections



■ Pin Description

No.	Symbol	I/O	Pin name
1-384	XO ₁ -ZO ₁₂₈	O	LCD drive output pins
385	GND	—	GND
386	V _{LS}	—	Power supply pin for analog circuit
387	V _{CC}	—	Power supply pin for digital circuit
388	LBR	I	Shift direction switching input pin
389-394	ZA ₀ -ZA ₅	I	Data input pin
395-400	ZB ₀ -ZB ₅	I	Data input pin
401-406	YB ₀ -YB ₅	I	Data input pin
407	REV	I	LCD drive output polarity exchange input pin
408	LS	I	Latch input pin
409	SPIO	I/O	Start pulse input/cascade output pin
410	CK	I	Shift clock input pin
411	POLA	I	Input data polarity exchange input pin
412	POLB	I	Input data polarity exchange input pin
413-421	VL ₀ -VL ₆₄	I	Reference voltage input pin
422-430	VH ₆₄ -VH ₀	I	Reference voltage input pin
431	SPOI	I/O	Start pulse input/cascade output pin
432-437	YA ₀ -YA ₅	I	Data input pin
438-443	XA ₀ -XA ₅	I	Data input pin
444-449	XB ₀ -XB ₅	I	Data input pin
450	GND	—	GND
451	V _{LS}	—	Power supply pin for analog circuit
452	GND	—	GND

■ Block Diagram



■ Block Function

Block name	Block function
Shift resister	Used as a bi-directional shift register, which performs the shifting operation by CK and selects bits for data sampling.
Data latch	Used to temporarily latch the input data, which is sent to the sampling memory.
Sampling memory	Used to sample the data to be entered by time sharing.
Hold memory	Used for temporary latch processing of data in the sampling memory by LS input.
Level shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and send the shifted data to D/A converter.
Reference voltage generating circuit	Used to generate a 64 × 2-level voltage corrected of gamma by the resistance split circuit.
D/A converter	Used to generate analog signal according to the displayed data and send the signal to the output circuit.
Output circuit	Used as a voltage follower configured with an operational amplifier and an output buffer, which outputs analog signals of 64 × 2 gradations to LCD drive output pin.

■ Description of Functions and Operations

(1) Pin function

Symbol	I/O	Function
V _{CC}	—	Used as power supply pin for digital circuit (Use in the range of 2.7 to 3.6 V.)
V _{LS}	—	Used as power supply pin for analog circuit (Use in the range of 8 to 13 V.)
GND	—	Used as GND pin, which must be connected to 0 V.
SPIO SPOI	I/O	Used as input pin of start pulse and is also used as output pin for cascade connection. When "High" is input into start pulse input pin, data sampling is started. On completion of sampling, "High" pulse is output to output pin for cascade connection. Pin functions are switched by LBR. For relations of switching, refer to "(2) Operation of function".
LBR	I	Used as input pin for switch shift register directivity. For relations of switching, refer to "(2) Operation of function".
LS	I	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at rising edge and output from LCD drive output pin.
CK	I	Used as shift clock input pin. Data is latched into sampling memory from data input pin at rising edge.
VH ₀ -VH ₆₄ VL ₀ -VL ₆₄	I	Used as basic voltage input pin. Hold the basic potential before outputting gradation voltage. For relation between displayed data and output voltage value, refer to "(4) Output voltage value". For internal gamma correction, refer to "(5) Gamma correction value". Observe the following relation for input potential. V _{LS} > VH ₀ > VH ₈ > ... > VH ₆₄ > VL ₆₄ > VL ₅₆ > ... > VL ₀ > GND.
XA ₀ -XA ₅ YA ₀ -YA ₅ ZA ₀ -ZA ₅ XB ₀ -XB ₅ YB ₀ -YB ₅ ZB ₀ -ZB ₅	I	Used as data input pin of R, G, and B colors. Takes in 6-bits × 2 pixels data from data pin at rising edge of CK. For relation between input data and output, refer to "(4) Output voltage value". Correlate data to be entered into X, Y, and Z according to picture element arrays of the panel used.
XO ₁ -XO ₁₂₈ YO ₁ -YO ₁₂₈ ZO ₁ -ZO ₁₂₈	O	Used as LCD drive output pin, which outputs the voltage corresponding to the input of data input pin (XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅). Data of XO ₁ -XO ₁₂₈ correspond to XA ₀ -XA ₅ , XB ₀ -XB ₅ . Data of YO ₁ -YO ₁₂₈ correspond to YA ₀ -YA ₅ , YB ₀ -YB ₅ , ZO ₁ -ZO ₁₂₈ correspond to ZA ₀ -ZA ₅ , ZB ₀ -ZB ₅ . For relation of switching and input data, refer to "(2) Operation of function" and "(4) Output voltage value".
POLA POLB	I	Used as input pin for input data polarity exchange, POLA corresponds to XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , POLB corresponds to XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ . When "Low" is entered, displayed data is normal mode becomes enable. When "High" is entered, input data is polarity exchange mode becomes enable. For relation between input data and output, refer to "(4) Output voltage value". Usually, these pins are pull-down at the inside.
REV	I	Used as polarity exchange pin of LCD drive output. Takes in data at the term that LS is "High", decides output polarity of LCD drive output pin. For switching relation refer to "(3) Output characteristics".

(2) Operation of Function

The following describes the relation between data input pin and output direction.

Data input Pin	XA0-XA5	YA0-YA5	ZA0-ZA5	XB0-XB5	YB0-YB5	ZB0-ZB5	XB0-XB5	YB0-YB5	ZB0-ZB5
Output Direction	XO1	YO1	ZO1	XO2	YO2	ZO2	XO128	YO128	ZO128

The following describes the relation between LBR pin, SP pin and output direction.

Pin	RIGHT SHIFT (Shift register directivity)	LEFT SHIFT (Shift register directivity)
LBR	"High"	"Low"
SPOI	Input	Output
SPIO	Output	Input
Output direction	XO1, YO1, ZO1 (first clock) → XO128, YO128, ZO128 (last clock)	ZO128, YO128, XO128 (first clock) → ZO1, YO1, XO1 (last clock)

Note. Color data corresponding to X, Y and Z vary depending on RIGHT SHIFT/LEFT SHIFT.

(3) Output characteristics

The following describes the relation between REV pin and output polarity of LCD drive pin.

REV	"High"	"Low"
XO1	+	-
YO1	-	+
ZO1	+	-
XO2	-	+
YO2	+	-
ZO2	-	+
XO3	+	-
YO3	-	+
ZO3	+	-
XO4	-	+
YO4	+	-
ZO4	-	+
⋮	⋮	⋮
XO125	+	-
YO125	-	+
ZO125	+	-
XO126	-	+
YO126	+	-
ZO126	-	+
XO127	+	-
YO127	-	+
ZO127	+	-
XO128	-	+
YO128	+	-
ZO128	-	+

Note. + : The gradation voltages corresponding to basic voltage VH0-VH64 are outputs.
- : The gradation voltages corresponding to basic voltage VL0-VL64 are outputs.

(4) Output voltage value

Of the 6-bit data (D₅, D₄, D₃, D₂, D₁, and D₀) taken in by time sharing, reference power supply V₀ - V₆₄ is selected by upper 3 bits (D₅, D₄, and D₃) and interpolation value of output voltage is determined by lower 3 bits (D₂, D₁ and D₀). The basic voltage V_i is reference voltage (V_{Hi} or V_{Li}) that determined by polarity exchange input (REV).

Relation between input data and output voltage values is shown below.

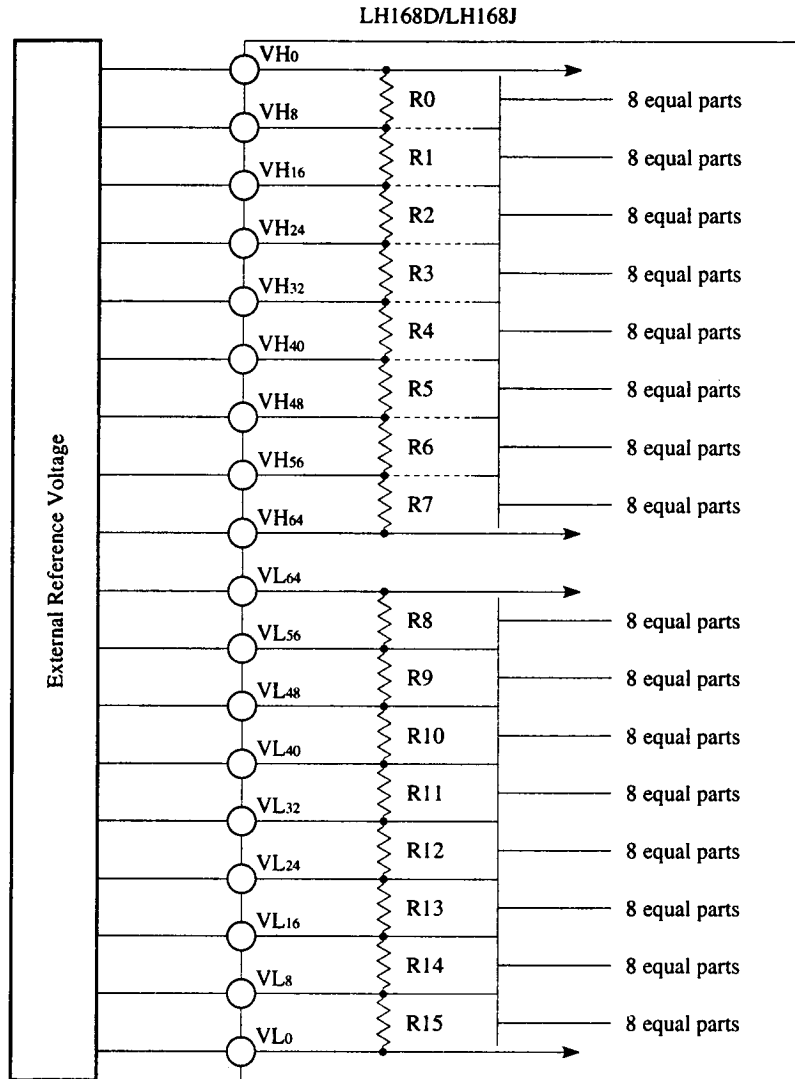
Input data	Output voltage		Input data	Output voltage	
	POLA(POLB)="Low"	POLA(POLB)="High"		POLA(POLB)="Low"	POLA(POLB)="High"
0	V ₀	V ₆₄ + (V ₅₆ - V ₆₄) × 1/8	20	V ₃₂	V ₃₂ + (V ₂₄ - V ₃₂) × 1/8
1	V ₈ + (V ₀ - V ₈) × 7/8	V ₆₄ + (V ₅₆ - V ₆₄) × 2/8	21	V ₄₀ + (V ₃₂ - V ₄₀) × 7/8	V ₃₂ + (V ₂₄ - V ₃₂) × 2/8
2	V ₈ + (V ₀ - V ₈) × 6/8	V ₆₄ + (V ₅₆ - V ₆₄) × 3/8	22	V ₄₀ + (V ₃₂ - V ₄₀) × 6/8	V ₃₂ + (V ₂₄ - V ₃₂) × 3/8
3	V ₈ + (V ₀ - V ₈) × 5/8	V ₆₄ + (V ₅₆ - V ₆₄) × 4/8	23	V ₄₀ + (V ₃₂ - V ₄₀) × 5/8	V ₃₂ + (V ₂₄ - V ₃₂) × 4/8
4	V ₈ + (V ₀ - V ₈) × 4/8	V ₆₄ + (V ₅₆ - V ₆₄) × 5/8	24	V ₄₀ + (V ₃₂ - V ₄₀) × 4/8	V ₃₂ + (V ₂₄ - V ₃₂) × 5/8
5	V ₈ + (V ₀ - V ₈) × 3/8	V ₆₄ + (V ₅₆ - V ₆₄) × 6/8	25	V ₄₀ + (V ₃₂ - V ₄₀) × 3/8	V ₃₂ + (V ₂₄ - V ₃₂) × 6/8
6	V ₈ + (V ₀ - V ₈) × 2/8	V ₆₄ + (V ₅₆ - V ₆₄) × 7/8	26	V ₄₀ + (V ₃₂ - V ₄₀) × 2/8	V ₃₂ + (V ₂₄ - V ₃₂) × 7/8
7	V ₈ + (V ₀ - V ₈) × 1/8	V ₅₆	27	V ₄₀ + (V ₃₂ - V ₄₀) × 1/8	V ₂₄
8	V ₈	V ₅₆ + (V ₄₈ - V ₅₆) × 1/8	28	V ₄₀	V ₂₄ + (V ₁₆ - V ₂₄) × 1/8
9	V ₁₆ + (V ₈ - V ₁₆) × 7/8	V ₅₆ + (V ₄₈ - V ₅₆) × 2/8	29	V ₄₈ + (V ₄₀ - V ₄₈) × 7/8	V ₂₄ + (V ₁₆ - V ₂₄) × 2/8
A	V ₁₆ + (V ₈ - V ₁₆) × 6/8	V ₅₆ + (V ₄₈ - V ₅₆) × 3/8	2A	V ₄₈ + (V ₄₀ - V ₄₈) × 6/8	V ₂₄ + (V ₁₆ - V ₂₄) × 3/8
B	V ₁₆ + (V ₈ - V ₁₆) × 5/8	V ₅₆ + (V ₄₈ - V ₅₆) × 4/8	2B	V ₄₈ + (V ₄₀ - V ₄₈) × 5/8	V ₂₄ + (V ₁₆ - V ₂₄) × 4/8
C	V ₁₆ + (V ₈ - V ₁₆) × 4/8	V ₅₆ + (V ₄₈ - V ₅₆) × 5/8	2C	V ₄₈ + (V ₄₀ - V ₄₈) × 4/8	V ₂₄ + (V ₁₆ - V ₂₄) × 5/8
D	V ₁₆ + (V ₈ - V ₁₆) × 3/8	V ₅₆ + (V ₄₈ - V ₅₆) × 6/8	2D	V ₄₈ + (V ₄₀ - V ₄₈) × 3/8	V ₂₄ + (V ₁₆ - V ₂₄) × 6/8
E	V ₁₆ + (V ₈ - V ₁₆) × 2/8	V ₅₆ + (V ₄₈ - V ₅₆) × 7/8	2E	V ₄₈ + (V ₄₀ - V ₄₈) × 2/8	V ₂₄ + (V ₁₆ - V ₂₄) × 7/8
F	V ₁₆ + (V ₈ - V ₁₆) × 1/8	V ₄₈	2F	V ₄₈ + (V ₄₀ - V ₄₈) × 1/8	V ₁₆
10	V ₁₆	V ₄₈ + (V ₄₀ - V ₄₈) × 1/8	30	V ₄₈	V ₁₆ + (V ₈ - V ₁₆) × 1/8
11	V ₂₄ + (V ₁₆ - V ₂₄) × 7/8	V ₄₈ + (V ₄₀ - V ₄₈) × 2/8	31	V ₅₆ + (V ₄₈ - V ₅₆) × 7/8	V ₁₆ + (V ₈ - V ₁₆) × 2/8
12	V ₂₄ + (V ₁₆ - V ₂₄) × 6/8	V ₄₈ + (V ₄₀ - V ₄₈) × 3/8	32	V ₅₆ + (V ₄₈ - V ₅₆) × 6/8	V ₁₆ + (V ₈ - V ₁₆) × 3/8
13	V ₂₄ + (V ₁₆ - V ₂₄) × 5/8	V ₄₈ + (V ₄₀ - V ₄₈) × 4/8	33	V ₅₆ + (V ₄₈ - V ₅₆) × 5/8	V ₁₆ + (V ₈ - V ₁₆) × 4/8
14	V ₂₄ + (V ₁₆ - V ₂₄) × 4/8	V ₄₈ + (V ₄₀ - V ₄₈) × 5/8	34	V ₅₆ + (V ₄₈ - V ₅₆) × 4/8	V ₁₆ + (V ₈ - V ₁₆) × 5/8
15	V ₂₄ + (V ₁₆ - V ₂₄) × 3/8	V ₄₈ + (V ₄₀ - V ₄₈) × 6/8	35	V ₅₆ + (V ₄₈ - V ₅₆) × 3/8	V ₁₆ + (V ₈ - V ₁₆) × 6/8
16	V ₂₄ + (V ₁₆ - V ₂₄) × 2/8	V ₄₈ + (V ₄₀ - V ₄₈) × 7/8	36	V ₅₆ + (V ₄₈ - V ₅₆) × 2/8	V ₁₆ + (V ₈ - V ₁₆) × 7/8
17	V ₂₄ + (V ₁₆ - V ₂₄) × 1/8	V ₄₀	37	V ₅₆ + (V ₄₈ - V ₅₆) × 1/8	V ₈
18	V ₂₄	V ₄₀ + (V ₃₂ - V ₄₀) × 1/8	38	V ₅₆	V ₈ + (V ₀ - V ₈) × 1/8
19	V ₃₂ + (V ₂₄ - V ₃₂) × 7/8	V ₄₀ + (V ₃₂ - V ₄₀) × 2/8	39	V ₆₄ + (V ₅₆ - V ₆₄) × 7/8	V ₈ + (V ₀ - V ₈) × 2/8
1A	V ₃₂ + (V ₂₄ - V ₃₂) × 6/8	V ₄₀ + (V ₃₂ - V ₄₀) × 3/8	3A	V ₆₄ + (V ₅₆ - V ₆₄) × 6/8	V ₈ + (V ₀ - V ₈) × 3/8
1B	V ₃₂ + (V ₂₄ - V ₃₂) × 5/8	V ₄₀ + (V ₃₂ - V ₄₀) × 4/8	3B	V ₆₄ + (V ₅₆ - V ₆₄) × 5/8	V ₈ + (V ₀ - V ₈) × 4/8
1C	V ₃₂ + (V ₂₄ - V ₃₂) × 4/8	V ₄₀ + (V ₃₂ - V ₄₀) × 5/8	3C	V ₆₄ + (V ₅₆ - V ₆₄) × 4/8	V ₈ + (V ₀ - V ₈) × 5/8
1D	V ₃₂ + (V ₂₄ - V ₃₂) × 3/8	V ₄₀ + (V ₃₂ - V ₄₀) × 6/8	3D	V ₆₄ + (V ₅₆ - V ₆₄) × 3/8	V ₈ + (V ₀ - V ₈) × 6/8
1E	V ₃₂ + (V ₂₄ - V ₃₂) × 2/8	V ₄₀ + (V ₃₂ - V ₄₀) × 7/8	3E	V ₆₄ + (V ₅₆ - V ₆₄) × 2/8	V ₈ + (V ₀ - V ₈) × 7/8
1F	V ₃₂ + (V ₂₄ - V ₃₂) × 1/8	V ₃₂	3F	V ₆₄ + (V ₅₆ - V ₆₄) × 1/8	V ₀

(5) γ (gamma) correction value

Between reference voltage input pin VH_0 and VH_{64} , 64 resistors are connected in series. And between reference voltage input pin VL_0 and VL_{64} , 64 resistors are connected in series. And between reference voltage input pin VH_{64} and VL_{64} , a resistor isn't connected.

The γ correction curve is broken line connected between intermediate voltage input ($VH_8, VH_{16}, VH_{24}, VH_{32}, VH_{40}, VH_{48}, VH_{56}, VL_8, VL_{16}, VL_{24}, VL_{32}, VL_{40}, VL_{48}$ and VL_{56}).

Between the intermediate voltage input, it is divided into 8 parts by the same resistor.



The following shows the ratio of 2 correction resistance, when R_0 equals 1.

R0	1.00
R1	0.50
R2	0.50
R3	0.50
R4	0.50
R5	0.50
R6	0.50
R7	1.00

R8	1.00
R9	0.50
R10	0.50
R11	0.50
R12	0.50
R13	0.50
R14	0.50
R15	1.00

■ Absolute Maximum Ratings

Parameter		Symbol	Condition	Rating	Unit
Supply voltage	V _{CC}	V _{CC}	T _a =25°C	-0.3 to +7.0	V
	V _{LS}	V _{LS}	T _a =25°C	-0.3 to +15.0	V
Input voltage	V _{H0} -V _{L0}	V _i	T _a =25°C	-0.3 to V _{LS} +0.3	V
	Other	V _i	T _a =25°C	-0.3 to V _{CC} +0.3	V
Output voltage	SPIO, SPOI	V _o	T _a =25°C	-0.3 to V _{CC} +0.3	V
	XO ₁ -ZO ₁₂₈	V _o	T _a =25°C	-0.3 to V _{LS} +0.3	V
Storage temperature		T _{stg}		-45 to +125	°C

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V _{CC}	2.7		3.6	V	
	V _{LS}	8.0		13.0	V	
Reference voltage input	V _{H0} -V _{H64}	0.5V _{LS}		V _{LS} - 0.1	V	1
	V _{L0} -V _{L64}	+0.1		0.5V _{LS}	V	
Clock frequency	f _{CK}			65	MHz	
LCD drive output load capacity	CL			150	pF	
Operating temperature	T _{opr}	-20		75	°C	

Note 1. Observe the following relation for the potential of the reference voltage input.

$$V_{LS} > V_{H0} > V_{H8} > V_{H16} > V_{H24} > V_{H32} > V_{H40} > V_{H48} > V_{H56} > V_{H64} \geq 0.5 V_{LS} \\ \geq V_{L64} > V_{L56} > V_{L48} > V_{L40} > V_{L32} > V_{L24} > V_{L16} > V_{L8} > V_{L0} > GND$$

Note 2. Observe the following sequence of switching power supply on the device.

$$V_{CC} \rightarrow \text{Logic input} \rightarrow V_{LS}, V_{H0}-V_{H64}, V_{L64}-V_{L0}$$

Observe the contrary sequence of switching power supply off the device.

DC Electrical Characteristics

($V_{CC}=2.7$ to 3.6 V, $V_{LS}=8.0$ to 13 V, $T_a=-20$ to $+75$ °C)

Parameter	Symbol	Measuring condition	Applicable pin	MIN.	TYP.	MAX.	Unit
Input "Low" current	I_{ILL1}		XA0-XA5, YA0-YA5, ZA0-ZA5, XB0-XB5, YB0-YB5, ZB0-ZB5, SPIO, SPOI, CK, LS, LBR, REV, POLA, POLB			10	μ A
Input "High" current	I_{ILH1}		XA0-XA5, YA0-YA5, ZA0-ZA5, XB0-XB5, YB0-YB5, ZB0-ZB5, SPIO, SPOI, CK, LS, LBR, REV			10	μ A
	I_{ILH2}		POLA, POLB			400	μ A
Input "Low" voltage	V_{IL}		XA0-XA5, YA0-YA5, ZA0-ZA5, XB0-XB5, YB0-YB5, ZB0-ZB5, SPIO, SPOI, CK, LS, LBR, REV, POLA, POLB	GND		$0.3V_{CC}$	V
Input "High" voltage	V_{IH}		XA0-XA5, YA0-YA5, ZA0-ZA5, XB0-XB5, YB0-YB5, ZB0-ZB5, SPIO, SPOI, CK, LS, LBR, REV, POLA, POLB	$0.7V_{CC}$		V_{CC}	V
Output "Low" voltage	V_{OL}	$I_{OL}=0.3$ mA	SPIO	GND		$GND + 0.4$	V
Output "High" voltage	V_{OH}	$I_{OH}=-0.3$ mA	SPOI	$V_{CC} - 0.4$		V_{CC}	V
Current consumption (In operation mode)	I_{CC1}	*1	$V_{CC} - GND$			14	mA
Current consumption (In standby mode)	I_{CC2}	*2	$V_{CC} - GND$			4.0	mA
Current consumption (In operation mode)	I_{LS1}	*1	$V_{LS} - GND$			10	mA
Current consumption (In standby mode)	I_{LS2}	*2	$V_{LS} - GND$			8.0	mA
Output voltage range	V_{OUT}			$GND + 0.2$		$V_{LS} - 0.2$	V
Deviations between output voltage pins	V_{OD}		XO1-ZO128	-20		20	mV
Output current	I_{O1-I04}	*3			200		μ A
Resistance between reference power supplies	R_{GMAH}		Between V_{H0} and V_{H64}		20		k Ω
	R_{GMAL}		Between V_{L0} and V_{L64}		20		k Ω

[Measuring condition]

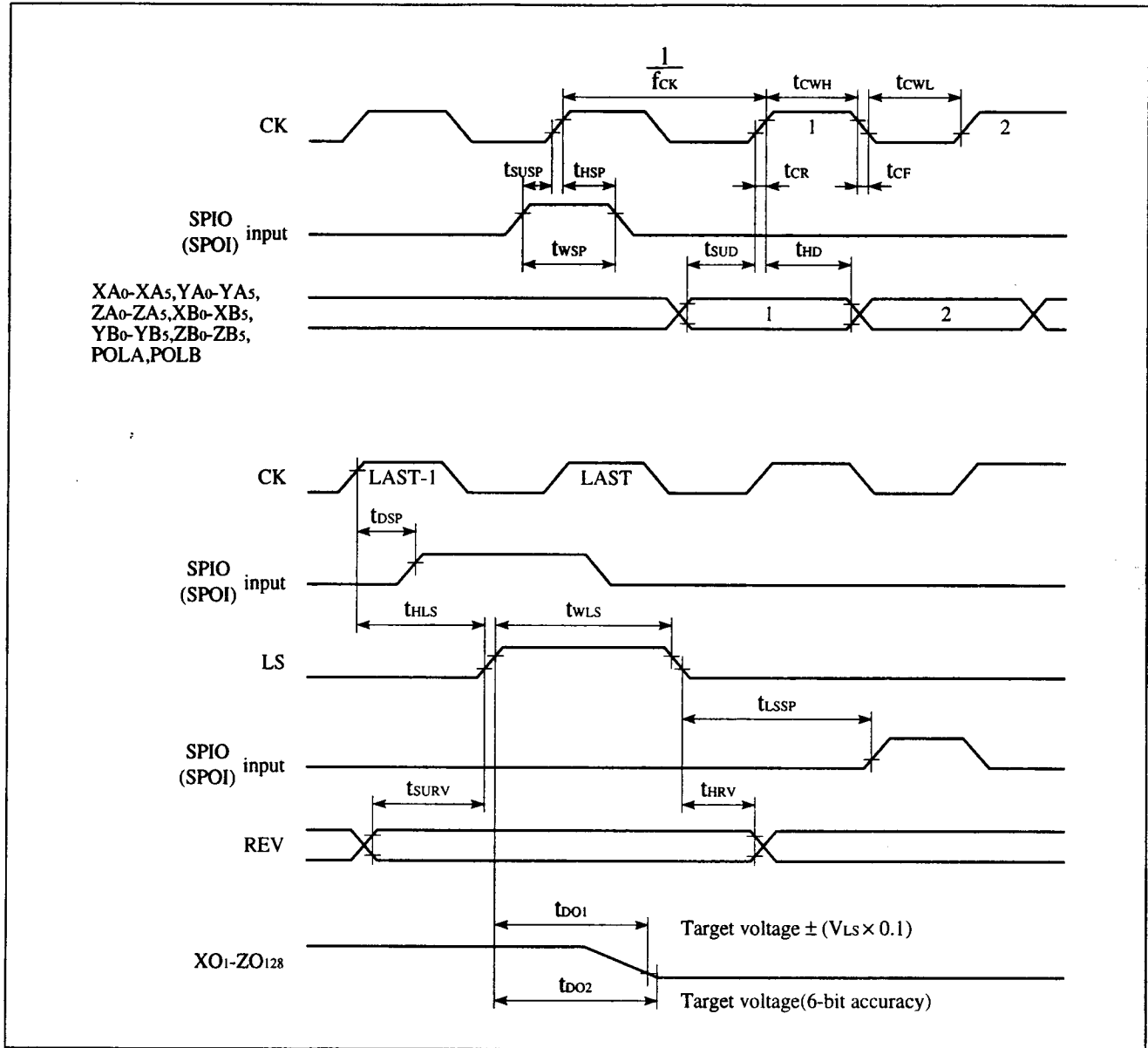
- *1 $f_{CK}=65$ MHz, $f_{LS}=50$ kHz (Data sampling state)
- *2 $f_{CK}=65$ MHz, $f_{LS}=50$ kHz, SPT=GND is fixed. (Standby state)
- *3
 - IO1 • Applied voltage = 8.0 V(XO1-ZO128)
 - Output voltage = 7.5 V(XO1-ZO128)
 - $V_{LS}=10$ V
 - IO2 • Applied voltage = 7.0 V(XO1-ZO128)
 - Output voltage = 7.5 V(XO1-ZO128)
 - $V_{LS}=10$ V
 - IO3 • Applied voltage = 3.0 V(XO1-ZO128)
 - Output voltage = 2.5 V(XO1-ZO128)
 - $V_{LS}=10$ V
 - IO4 • Applied voltage = 2.0 V(XO1-ZO128)
 - Output voltage = 2.5 V(XO1-ZO128)
 - $V_{LS}=10$ V

■ AC Electrical Characteristics

(V_{CC}=2.7 to 3.6 V, V_{LS}=8.0 to 13 V, T_a=-20 to +75 °C)

Parameter	Symbol	Measuring condition	Applicable pin	MIN.	TYP.	MAX.	Unit
Clock frequency	f _{CK}		CK			65	MHz
"High" level pulse width	t _{CWH}			4.0			ns
"Low" level pulse width	t _{CWL}			4.0			ns
Input rise time	t _{CR}					10	ns
Input fall time	t _{CF}					10	ns
Data set up time	t _{SUD}		XA ₀ -XA ₅ , XB ₀ -XB ₅ YA ₀ -YA ₅ , YB ₀ -YB ₅	4.0			ns
Data hold time	t _{HD}		ZA ₀ -ZA ₅ , ZB ₀ -ZB ₅ POLA, POLB	4.0			ns
Start pulse setup time	t _{SUSP}		SPIO, SPOI	4.0			ns
Start pulse hold time	t _{HSP}		SPIO, SPOI	4.0			ns
Start pulse width	t _{WSP}		SPIO, SPOI			$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t _{DSP}	C _L = 15 pF	SPIO, SPOI			11	ns
LCD drive output delay time	t _{DO1}	C _L = 150 pF	XO ₁ -ZO ₁₂₈			3	μs
	t _{DO2}	C _L = 150 pF				10	μs
LS signal, SPI signal setup time	t _{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal, CK signal hold time	t _{HLS}		LS	7			ns
LS signal "High" level width	t _{WLS}		LS	$\frac{1}{f_{CK}}$			ns
REV signal, LS signal setup time	t _{SURV}		REV	14			ns
REV signal, LS signal hold time	t _{HRV}		REV	10			ns

■ Timing Diagram



■ Example of Typical Characteristics

($T_a=25\text{ }^\circ\text{C}$, $GND=0\text{ V}$, $V_{CC}=3.3\text{ V}$)

Parameter	MIN.	TYP.	MAX.	Unit
Basic gate propagation delay time		10		ns

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