

LH168K

324-output TFT-LCD Source Driver IC

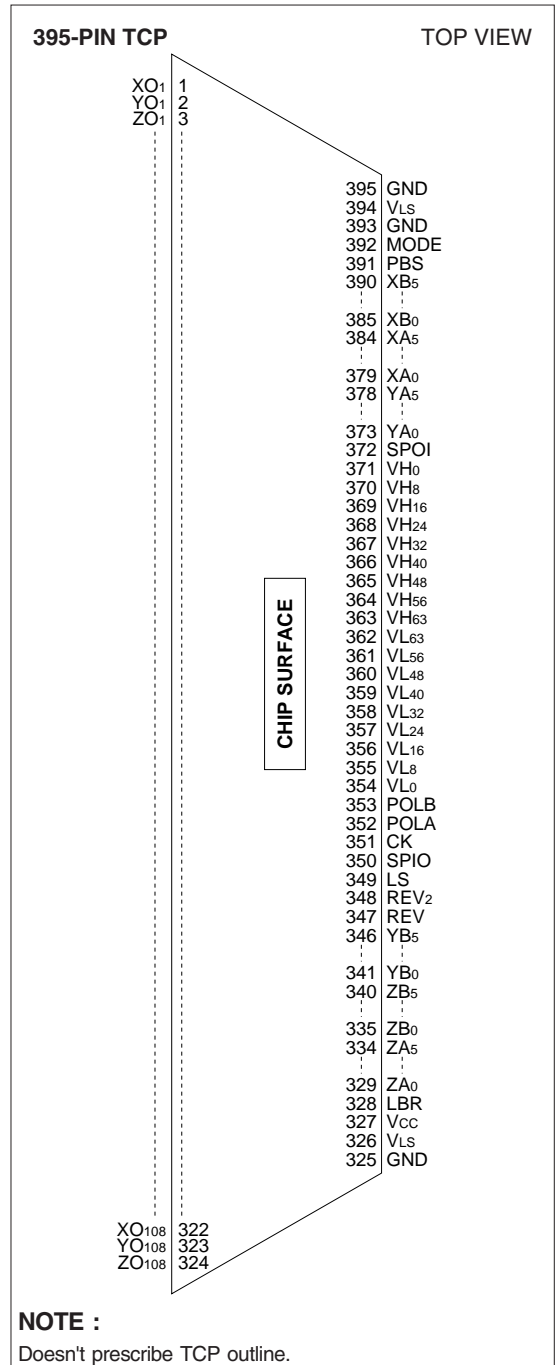
DESCRIPTION

The LH168K is a 324-output TFT-LCD source driver IC which can simultaneously display 262 144 colors in 64 gray scales.

FEATURES

- Selectable number of LCD drive outputs : 324/321/312/309
- Built-in 6-bit digital input DAC
- Dot-inversion drive : Outputs the inverted gray scale voltages between LCD drive pins next to each other
- 2-port input for each circuit of data inputs R, G and B, and it is possible to sample and hold display data of two pixels at the same time at 324-output and 312-output modes. 1-port input for each circuit of data inputs R, G and B at 321-output and 309-output modes.
- Possible to display 262 144 colors in 64 gray scales with reference voltage input of 18 gray scales : This reference voltage input corresponds to γ correction and intermediate reference voltage input can be abbreviated
- Cascade connection
- Sampling sequence :
Output shift direction can be selected
XO₁, YO₁, ZO₁→XO₁₀₈, YO₁₀₈, ZO₁₀₈ or
ZO₁₀₈, YO₁₀₈, XO₁₀₈→ZO₁, YO₁, XO₁
- Shift clock frequency : 55 MHz (MAX.)
- Supply voltages
 - V_{CC} (for logic system) : +2.7 to +3.6 V
 - V_{LS} (for LCD drive system) : +12 V (MAX.)
- Package : 395-pin TCP (Tape Carrier Package)

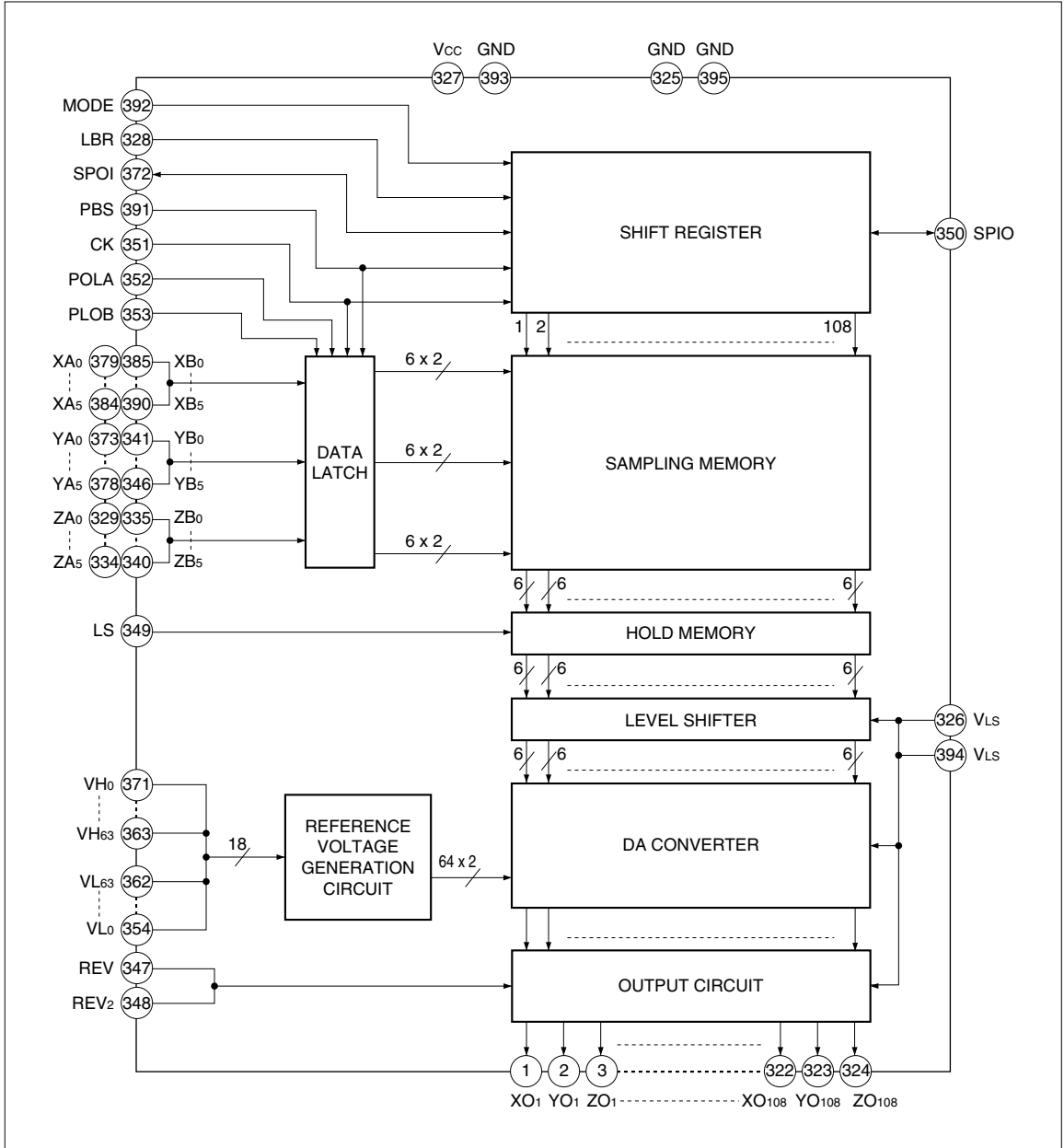
PIN CONNECTIONS



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 324	XO1-ZO108	O	LCD drive output pins
325, 393, 395	GND	–	Ground pins
326, 394	VLS	–	Power supply pins for analog circuit
327	VCC	–	Power supply pin for digital circuit
328	LBR	I	Shift direction selection input pin
329 to 334	ZA0-ZA5	I	Data input pins
335 to 340	ZB0-ZB5	I	Data input pins
341 to 346	YB0-YB5	I	Data input pins
347, 348	REV, REV2	I	LCD drive output polarity exchange input pins
349	LS	I	Latch input pin
350	SPIO	I/O	Start pulse input/cascade output pin
351	CK	I	Shift clock input pin
352, 353	POLA, POLB	I	Input data polarity exchange input pins
354 to 362	VL0-VL63	I	Reference voltage input pins
363 to 371	VH63-VH0	I	Reference voltage input pins
372	SPOI	I/O	Start pulse input/cascade output pin
373 to 378	YA0-YA5	I	Data input pins
379 to 384	XA0-XA5	I	Data input pins
385 to 390	XB0-XB5	I	Data input pins
391	PBS	I	2-port/1-port selection input pin
392	MODE	I	Input pin for selecting the number of LCD drive outputs

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Shift Register	Used as a bi-directional shift register which performs the shifting operation by CK and selects bits for data sampling.
Data Latch	Used to temporary latch the input data which is sent to the sampling memory.
Sampling Memory	Used to sample the data to be entered by time sharing.
Hold memory	Used for latch processing of data in the sampling memory by LS input.
Level Shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and sends the shifted data to DA converter.
Reference Voltage Generation Circuit	Used to generate a gamma-corrected 64 x 2-level voltage by the resistor dividing circuit.
DA Converter	Used to generate an analog signal according to the display data and sends the signal to the output circuit.
Output Circuit	Used as a voltage follower, configured with an operational amplifier and an output buffer, which outputs analog signals of 64 x 2 gray scales to LCD drive output pin.

INPUT/OUTPUT CIRCUITS

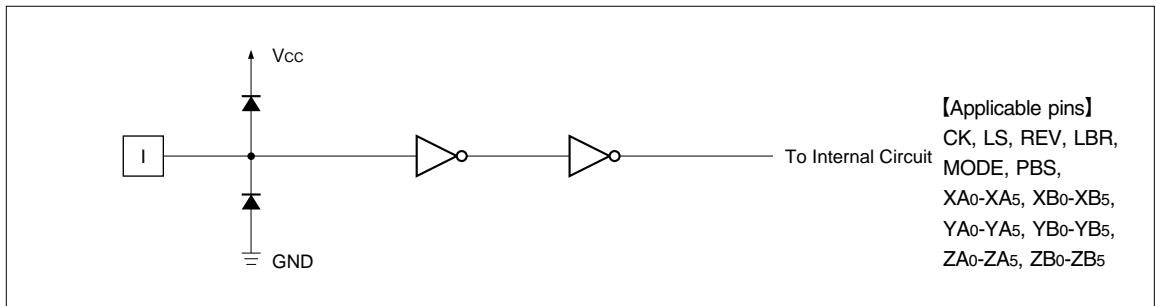


Fig. 1 Input Circuit (1)

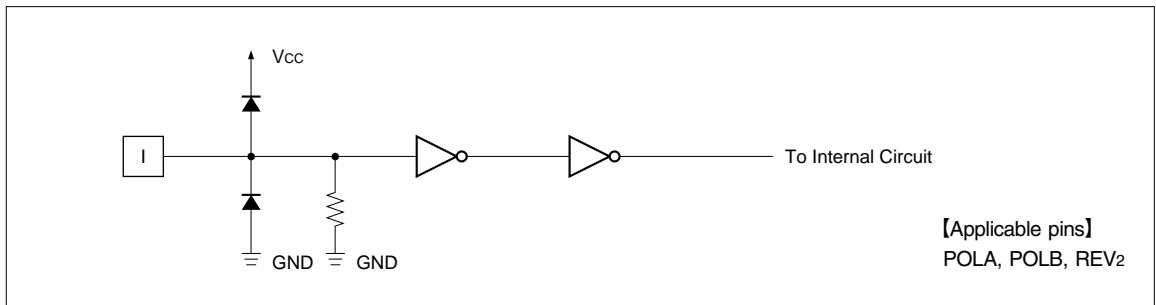


Fig. 2 Input Circuit (2)

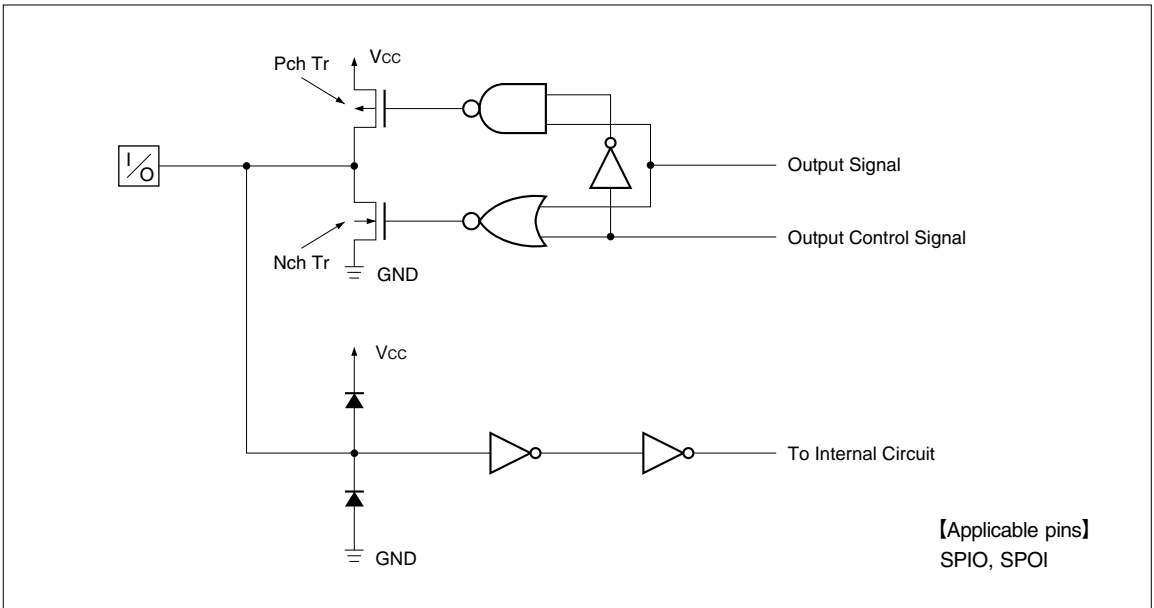


Fig. 3 Input/Output Circuit

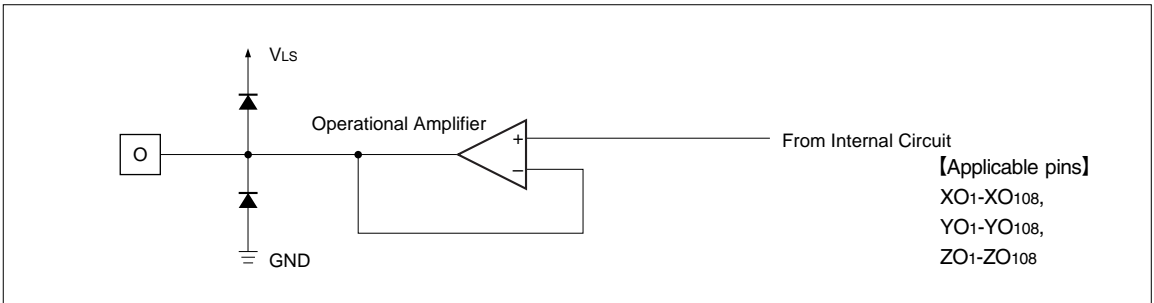


Fig. 4 Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTION
VCC	Used as power supply pin for digital circuit, connected to +2.7 to +3.6 V.
VLS	Used as power supply pin for analog circuit, connected to +8.0 to +12.0 V.
GND	Used as ground pin, connected to 0 V.
SPIO SPOI	Used as input pins of start pulse and also used as output pins for cascade connection. When "H" is input into start pulse input pin, data sampling is started. On completion of sampling, "H" pulse is output to output pin for cascade connection. Pin functions are selected by LBR. For selecting, refer to " Functional Operations ".
LBR	Used as input pin for selecting the shift register direction. For selecting, refer to " Functional Operations ".
LS	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at the rising edge and output from LCD drive output pin.
CK	Used as shift clock input pin. Data is latched into sampling memory from data input pin at the rising edge.
VH0-VH63 VL0-VL63	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. For relation between input data and output voltage values, refer to " Output Voltage Value ". For internal gamma correction, refer to " Gamma Correction Value ". Observe the following relation for input voltage. $VLS > VH0 \geq VH8 \geq \dots \geq VH63 \geq VL63 \geq VL56 \geq \dots \geq VL0 > GND$.
XA0-XA5 YA0-YA5 ZA0-ZA5 XB0-XB5 YB0-YB5 ZB0-ZB5	Used as data input pins of R, G, and B colors. 6-bit data are input from data pins at the rising edge of CK. When PBS is "L", 2-pixel data are input from XA0 to XA5, YA0 to YA5, ZA0 to ZA5 and XB0 to XB5, YB0 to YB5, ZB0 to ZB5 at the same time. When PBS is "H", 1-pixel data is input from XA0 to XA5, YA0 to YA5 and ZA0 to ZA5, and fixed XB0 to XB5, YB0 to YB5 and ZB0 to ZB5 to "L" or "H". For relation between input data and output voltage values, refer to " Functional Operations " and " Output Voltage Value ". Select the data to be entered into X, Y, and Z according to picture element arrays of the panel.
MODE	Used as input pin for selecting the number of LCD drive outputs, which sets up operation mode with PBS pin. When "L" is entered, it becomes 324-output/2-port input mode at PBS pin "L" or 321-output/1-port input mode at PBS pin "H". When "H" is entered, it becomes 312-output/2-port input mode at PBS pin "L" or 309-output/1-port mode at PBS pin "H". For selecting the number of LCD drive outputs, refer to " Output Characteristics ".
PBS	Used as 2-port/1-port exchange input pin to take in data. When "L" is entered, it becomes 2-port input mode and 2-pixel data are input at the same time. When "H" is entered, it becomes 1-port input mode.

SYMBOL	FUNCTIONS
XO1-XO108 YO1-YO108 ZO1-ZO108	<p>Used as LCD drive output pins which output the voltage corresponding to the input of data input pins. When 321-output mode, 3 outputs (XO54 to ZO54) are invalid. When 312-output mode, 12 outputs (XO55 to XO58, YO55 to YO58, ZO55 to ZO58) are invalid. When 309-outputs mode, 15 outputs (XO54 to XO58, YO54 to YO58, ZO54 to ZO58) are invalid. Invalid output pins must be opened. Data of XO1 to XO108 correspond to XA0 to XA5 and XB0 to XB5. Data of YO1 to YO108 correspond to YA0 to YA5 and YB0 to YB5, and data of ZO0 to ZO108 correspond to ZA0 to ZA5 and ZB0 to ZB5. For relation between input data and output voltage values, refer to "Functional Operations" and "Output Voltage Value".</p>
POLA POLB	<p>Used as input pins for input data polarity exchange, POLA corresponds to XA0 to XA5, YA0 to YA5 and ZA0 to ZA5, and POLB corresponds to XB0 to XB5, YB0 to YB5 and ZB0 to ZB5. When "L" is entered, display data becomes normal mode. When "H" is entered, input data becomes polarity exchange mode. For relation between input data and output voltage values, refer to "Output Voltage Value". These pins are pulled down at the inside.</p>
REV REV2	<p>Used as polarity exchange pins of LCD drive output. Data is taken at the term when LS is "H" and the output polarity of the LCD drive output pin is determined. Function of REV is the same as function of REV2. Input polarity exchange signal to REV, and REV2 is fixed to "L" or opened in general.</p> <p>When 321-output/309-output mode, it is possible to exchange output polarity between LCD driver next to each other by fixing REV2 to "L" or "H" according to position on panel. For exchanging, refer to "Output Characteristics". REV2 pin is pulled down at the inside.</p>

Functional Operations

The following describes the relation between data input pin and output direction.

(1) PBS = "L"

Data input pin	XA0-XA5	YA0-YA5	ZA0-ZA5	XB0-XB5	YB0-YB5	ZB0-ZB5	XB0-XB5	YB0-YB5	ZB0-ZB5
Output direction	XO1	YO1	ZO1	XO2	YO2	ZO2	XO108	YO108	ZO108

(2) PBS = "H"

Data input pin	XA0-XA5	YA0-YA5	ZA0-ZA5	XA0-XA5	YA0-YA5	ZA0-ZA5	XA0-XA5	YA0-YA5	ZA0-ZA5
Output direction	XO1	YO1	ZO1	XO2	YO2	ZO2	XO108	YO108	ZO108

The following describes the relation between LBR pin, SPOI pin, SPIO pin and output direction.

PIN	OUTPUT DIRECTION	
	RIGHT SHIFT (XO1, YO1, ZO1→XO108, YO108, ZO108)	LEFT SHIFT (ZO108, YO108, XO108→ZO1, YO1, XO1)
LBR	H	L
SPOI	Input	Output
SPIO	Output	Input

NOTE :

Color data corresponding to X, Y, and Z vary depending on the output direction.

Output Characteristics

The following describes the relation between operation mode, REV pin, REV₂ pin and output polarity of LCD drive pin.

MODE	WHEN REV = "L", REV ₂ = "L" or REV = "H", REV ₂ = "H"				WHEN REV = "H", REV ₂ = "L" or REV = "L", REV ₂ = "H"			
	L	L	H	H	L	L	H	H
PBS	L	H	L	H	L	H	L	H
Operation	324-output mode	321-output mode	312-output mode	309-output mode	324-output mode	321-output mode	312-output mode	309-output mode
XO ₁	-	-	-	-	+	+	+	+
YO ₁	+	+	+	+	-	-	-	-
ZO ₁	-	-	-	-	+	+	+	+
XO ₂	+	+	+	+	-	-	-	-
YO ₂	-	-	-	-	+	+	+	+
ZO ₂	+	+	+	+	-	-	-	-

XO ₅₃	-	-	-	-	+	+	+	+
YO ₅₃	+	+	+	+	-	-	-	-
ZO ₅₃	-	-	-	-	+	+	+	+
XO ₅₄	+	NA	+	NA	-	NA	-	NA
YO ₅₄	-	NA	-	NA	+	NA	+	NA
ZO ₅₄	+	NA	+	NA	-	NA	-	NA
XO ₅₅	-	+	NA	NA	+	-	NA	NA
YO ₅₅	+	-	NA	NA	-	+	NA	NA
ZO ₅₅	-	+	NA	NA	+	-	NA	NA
XO ₅₆	+	-	NA	NA	-	+	NA	NA
YO ₅₆	-	+	NA	NA	+	-	NA	NA
ZO ₅₆	+	-	NA	NA	-	+	NA	NA
XO ₅₇	-	+	NA	NA	+	-	NA	NA
YO ₅₇	+	-	NA	NA	-	+	NA	NA
ZO ₅₇	-	+	NA	NA	+	-	NA	NA
XO ₅₈	+	-	NA	NA	-	+	NA	NA
YO ₅₈	-	+	NA	NA	+	-	NA	NA
ZO ₅₈	+	-	NA	NA	-	+	NA	NA
XO ₅₉	-	+	-	+	+	-	+	-
YO ₅₉	+	-	+	-	-	+	-	+
ZO ₅₉	-	+	-	+	+	-	+	-

XO ₁₀₇	-	+	-	+	+	-	+	-
YO ₁₀₇	+	-	+	-	-	+	-	+
ZO ₁₀₇	-	+	-	+	+	-	+	-
XO ₁₀₈	+	-	+	-	-	+	-	+
YO ₁₀₈	-	+	-	+	+	-	+	-
ZO ₁₀₈	+	-	+	-	-	+	-	+

NOTES :

+ : The gray scale voltages corresponding to reference voltage VH₀ to VH₆₃ are output.

- : The gray scale voltages corresponding to reference voltage VL₀ to VL₆₃ are output.

NA : Non active. Must be opened.

Output Voltage Value

Two voltages are selected from all of the reference voltages (V_0 - V_{63}) by the upper 3-bit data (D_5 , D_4 and D_3) of the 6-bit input data (D_5 , D_4 , D_3 , D_2 , D_1 and D_0) taken by time sharing, and intermediate value is determined by the lower 3-bit data (D_2 , D_1 and D_0).

The V_i is a reference voltage (V_{Hi} or V_{Li}) that is determined by the polarity exchange input (REV and REV_2).

Relation between input data and output voltage values is shown below.

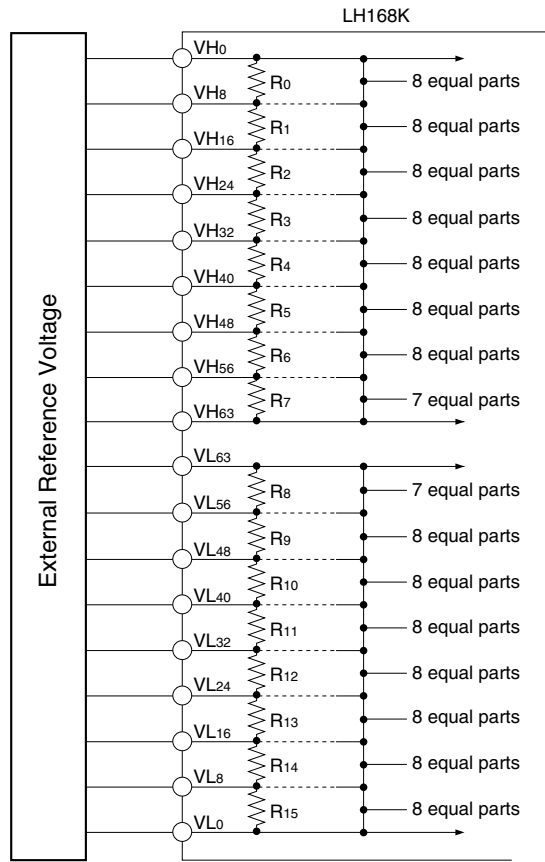
$$(i = 0, 8, 16, 24, 32, 40, 48, 56, 63)$$

INPUT DATA	OUTPUT VOLTAGE		INPUT DATA	OUTPUT VOLTAGE	
	POLA (POLB) = "L"	POLA (POLB) = "H"		POLA (POLB) = "L"	POLA (POLB) = "H"
0	V_0	V_{63}	20	V_{32}	$V_{32} + (V_{24} - V_{32}) \times 1/8$
1	$V_8 + (V_0 - V_8) \times 7/8$	$V_{63} + (V_{56} - V_{63}) \times 1/7$	21	$V_{40} + (V_{32} - V_{40}) \times 7/8$	$V_{32} + (V_{24} - V_{32}) \times 2/8$
2	$V_8 + (V_0 - V_8) \times 6/8$	$V_{63} + (V_{56} - V_{63}) \times 2/7$	22	$V_{40} + (V_{32} - V_{40}) \times 6/8$	$V_{32} + (V_{24} - V_{32}) \times 3/8$
3	$V_8 + (V_0 - V_8) \times 5/8$	$V_{63} + (V_{56} - V_{63}) \times 3/7$	23	$V_{40} + (V_{32} - V_{40}) \times 5/8$	$V_{32} + (V_{24} - V_{32}) \times 4/8$
4	$V_8 + (V_0 - V_8) \times 4/8$	$V_{63} + (V_{56} - V_{63}) \times 4/7$	24	$V_{40} + (V_{32} - V_{40}) \times 4/8$	$V_{32} + (V_{24} - V_{32}) \times 5/8$
5	$V_8 + (V_0 - V_8) \times 3/8$	$V_{63} + (V_{56} - V_{63}) \times 5/7$	25	$V_{40} + (V_{32} - V_{40}) \times 3/8$	$V_{32} + (V_{24} - V_{32}) \times 6/8$
6	$V_8 + (V_0 - V_8) \times 2/8$	$V_{63} + (V_{56} - V_{63}) \times 6/7$	26	$V_{40} + (V_{32} - V_{40}) \times 2/8$	$V_{32} + (V_{24} - V_{32}) \times 7/8$
7	$V_8 + (V_0 - V_8) \times 1/8$	V_{56}	27	$V_{40} + (V_{32} - V_{40}) \times 1/8$	V_{24}
8	V_8	$V_{56} + (V_{48} - V_{56}) \times 1/8$	28	V_{40}	$V_{24} + (V_{16} - V_{24}) \times 1/8$
9	$V_{16} + (V_8 - V_{16}) \times 7/8$	$V_{56} + (V_{48} - V_{56}) \times 2/8$	29	$V_{48} + (V_{40} - V_{48}) \times 7/8$	$V_{24} + (V_{16} - V_{24}) \times 2/8$
A	$V_{16} + (V_8 - V_{16}) \times 6/8$	$V_{56} + (V_{48} - V_{56}) \times 3/8$	2A	$V_{48} + (V_{40} - V_{48}) \times 6/8$	$V_{24} + (V_{16} - V_{24}) \times 3/8$
B	$V_{16} + (V_8 - V_{16}) \times 5/8$	$V_{56} + (V_{48} - V_{56}) \times 4/8$	2B	$V_{48} + (V_{40} - V_{48}) \times 5/8$	$V_{24} + (V_{16} - V_{24}) \times 4/8$
C	$V_{16} + (V_8 - V_{16}) \times 4/8$	$V_{56} + (V_{48} - V_{56}) \times 5/8$	2C	$V_{48} + (V_{40} - V_{48}) \times 4/8$	$V_{24} + (V_{16} - V_{24}) \times 5/8$
D	$V_{16} + (V_8 - V_{16}) \times 3/8$	$V_{56} + (V_{48} - V_{56}) \times 6/8$	2D	$V_{48} + (V_{40} - V_{48}) \times 3/8$	$V_{24} + (V_{16} - V_{24}) \times 6/8$
E	$V_{16} + (V_8 - V_{16}) \times 2/8$	$V_{56} + (V_{48} - V_{56}) \times 7/8$	2E	$V_{48} + (V_{40} - V_{48}) \times 2/8$	$V_{24} + (V_{16} - V_{24}) \times 7/8$
F	$V_{16} + (V_8 - V_{16}) \times 1/8$	V_{48}	2F	$V_{48} + (V_{40} - V_{48}) \times 1/8$	V_{16}
10	V_{16}	$V_{48} + (V_{40} - V_{48}) \times 1/8$	30	V_{48}	$V_{16} + (V_8 - V_{16}) \times 1/8$
11	$V_{24} + (V_{16} - V_{24}) \times 7/8$	$V_{48} + (V_{40} - V_{48}) \times 2/8$	31	$V_{56} + (V_{48} - V_{56}) \times 7/8$	$V_{16} + (V_8 - V_{16}) \times 2/8$
12	$V_{24} + (V_{16} - V_{24}) \times 6/8$	$V_{48} + (V_{40} - V_{48}) \times 3/8$	32	$V_{56} + (V_{48} - V_{56}) \times 6/8$	$V_{16} + (V_8 - V_{16}) \times 3/8$
13	$V_{24} + (V_{16} - V_{24}) \times 5/8$	$V_{48} + (V_{40} - V_{48}) \times 4/8$	33	$V_{56} + (V_{48} - V_{56}) \times 5/8$	$V_{16} + (V_8 - V_{16}) \times 4/8$
14	$V_{24} + (V_{16} - V_{24}) \times 4/8$	$V_{48} + (V_{40} - V_{48}) \times 5/8$	34	$V_{56} + (V_{48} - V_{56}) \times 4/8$	$V_{16} + (V_8 - V_{16}) \times 5/8$
15	$V_{24} + (V_{16} - V_{24}) \times 3/8$	$V_{48} + (V_{40} - V_{48}) \times 6/8$	35	$V_{56} + (V_{48} - V_{56}) \times 3/8$	$V_{16} + (V_8 - V_{16}) \times 6/8$
16	$V_{24} + (V_{16} - V_{24}) \times 2/8$	$V_{48} + (V_{40} - V_{48}) \times 7/8$	36	$V_{56} + (V_{48} - V_{56}) \times 2/8$	$V_{16} + (V_8 - V_{16}) \times 7/8$
17	$V_{24} + (V_{16} - V_{24}) \times 1/8$	V_{40}	37	$V_{56} + (V_{48} - V_{56}) \times 1/8$	V_8
18	V_{24}	$V_{40} + (V_{32} - V_{40}) \times 1/8$	38	V_{56}	$V_8 + (V_0 - V_8) \times 1/8$
19	$V_{32} + (V_{24} - V_{32}) \times 7/8$	$V_{40} + (V_{32} - V_{40}) \times 2/8$	39	$V_{63} + (V_{56} - V_{63}) \times 6/7$	$V_8 + (V_0 - V_8) \times 2/8$
1A	$V_{32} + (V_{24} - V_{32}) \times 6/8$	$V_{40} + (V_{32} - V_{40}) \times 3/8$	3A	$V_{63} + (V_{56} - V_{63}) \times 5/7$	$V_8 + (V_0 - V_8) \times 3/8$
1B	$V_{32} + (V_{24} - V_{32}) \times 5/8$	$V_{40} + (V_{32} - V_{40}) \times 4/8$	3B	$V_{63} + (V_{56} - V_{63}) \times 4/7$	$V_8 + (V_0 - V_8) \times 4/8$
1C	$V_{32} + (V_{24} - V_{32}) \times 4/8$	$V_{40} + (V_{32} - V_{40}) \times 5/8$	3C	$V_{63} + (V_{56} - V_{63}) \times 3/7$	$V_8 + (V_0 - V_8) \times 5/8$
1D	$V_{32} + (V_{24} - V_{32}) \times 3/8$	$V_{40} + (V_{32} - V_{40}) \times 6/8$	3D	$V_{63} + (V_{56} - V_{63}) \times 2/7$	$V_8 + (V_0 - V_8) \times 6/8$
1E	$V_{32} + (V_{24} - V_{32}) \times 2/8$	$V_{40} + (V_{32} - V_{40}) \times 7/8$	3E	$V_{63} + (V_{56} - V_{63}) \times 1/7$	$V_8 + (V_0 - V_8) \times 7/8$
1F	$V_{32} + (V_{24} - V_{32}) \times 1/8$	V_{32}	3F	V_{63}	V_0

γ (Gamma) Correction Value

Between reference voltage input pins VH0 and VH63, 63 resistors are connected in series. And between reference voltage input pins VL0 and VL63, 63 resistors are connected in series. No resistor is connected between reference voltage input pins VH63 and VL63.

The γ correction curve is a broken line connected between intermediate voltage inputs (VH8, VH16, VH24, VH32, VH40, VH48, VH56, VL8, VL16, VL24, VL32, VL40, VL48 and VL56). Each γ correction value between the intermediate voltage inputs is divided into 7 or 8 parts by the same resistor.



The following shows the ratio of γ correction resistance, when R0 equals 1.

R0	1.00
R1	0.20
R2	0.10
R3	0.10
R4	0.10
R5	0.10
R6	0.10
R7	0.20

R8	0.20
R9	0.10
R10	0.10
R11	0.10
R12	0.10
R13	0.10
R14	0.20
R15	1.00

PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

$V_{CC} \rightarrow$ logic input $\rightarrow V_{LS}, V_{H0}\text{-}V_{H63}, V_{L0}\text{-}V_{L63}$

When disconnecting the power supply, follow the reverse sequence.

Reference voltage input

The relation of the reference voltage input is shown here.

$V_{LS} > V_{H0} \geq V_{H8} \geq \dots \geq V_{H56} \geq V_{H63} \geq 0.5V_{LS} \geq V_{L63} \geq V_{L56} \geq \dots \geq V_{L8} \geq V_{L0} > GND$

Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

Target output load

This IC is designed for a 150 pF output load capacity. When using this IC for other than 150 pF panels, confirm the device is having no problem before using it.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V_{CC}	V_{CC}	-0.3 to +6.0	V	1, 2
	V_{LS}	V_{LS}	-0.3 to +13.0	V	
Input voltage	V_I	$V_{H0}\text{-}V_{L0}$	-0.3 to $V_{LS} + 0.3$	V	
	V_I	SPIO, SPOI, CK, LS, REV, REV ₂ , LBR, POLA, POLB, MODE, PBS, XA ₀ -XA ₅ , XB ₀ -XB ₅ , YA ₀ -YA ₅ , YB ₀ -YB ₅ , ZA ₀ -ZA ₅ , ZB ₀ -ZB ₅	-0.3 to $V_{CC} + 0.3$	V	
Output voltage	V_O	SPIO, SPOI	-0.3 to $V_{CC} + 0.3$	V	
	V_O	XO ₁ -ZO ₁₀₈	-0.3 to $V_{LS} + 0.3$	V	
Storage temperature	T _{STG}		-45 to +125	°C	

NOTES :

1. $T_A = +25\text{ }^\circ\text{C}$
2. The maximum applicable voltage on any pin with respect to GND (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	+2.7		+3.6	V	1
	V_{LS}	+8.0		+12.0	V	
Reference voltage input	$V_{H0}\text{-}V_{H63}$	$0.5V_{LS}$		$V_{LS} - 0.1$	V	
	$V_{L0}\text{-}V_{L63}$	+0.1		$0.5V_{LS}$	V	
Clock frequency	f _{CK}			55	MHz	
LCD drive output load capacity	CL			150	pF	
Operating temperature	T _{OPR}	-20		+75	°C	

NOTE :

1. The applicable voltage on any pin with respect to GND (0 V).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = +2.7 to +3.6 V, V_{LS} = +8.0 to +12.0 V, T_{OPR} = -20 to +75 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ , SPIO, SPOI, CK, LS, LBR, REV, REV ₂ , POLA, POLB, MODE, PBS	GND		0.3V _{CC}	V	
Input "High" voltage	V _{IH}			0.7V _{CC}		V _{CC}	V	
Output "Low" voltage	V _{OL}	I _{OL} = 0.3 mA	SPIO, SPOI	GND		GND + 0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -0.3 mA		V _{CC} - 0.4		V _{CC}	V	
Input "Low" current	I _{ILL1}		XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ , SPIO, SPOI, CK, LS, LBR, REV, REV ₂ , POLA, POLB, MODE, PBS			10	μA	
Input "High" current	I _{ILH1}		XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ , SPIO, SPOI, CK, LS, LBR, REV, MODE, PBS			10	μA	
	I _{ILH2}		POLA, POLB, REV ₂			400	μA	
Supply current (In operation mode)	I _{CC1}	f _{CK} = 55 MHz f _{LS} = 50 kHz (Data sampling state)	V _{CC} -GND			12	mA	
Supply current (In standby mode)	I _{CC2}	f _{CK} = 55 MHz f _{LS} = 50 kHz SPI = GND is fixed. (Standby state)				1.5	mA	
Supply current (In operation mode)	I _{LS1}	f _{CK} = 55 MHz f _{LS} = 50 kHz (Data sampling state)	V _{LS} -GND			4.5	mA	
Supply current (In standby mode)	I _{LS2}	f _{CK} = 55 MHz f _{LS} = 50 kHz SPI = GND is fixed. (Standby state)				3.5	mA	
Output voltage range	V _{OUT}		XO ₁ -ZO ₁₀₈	GND + 0.2		V _{LS} - 0.2	V	1
Deviations between output voltage pins	V _{OD}			-20		+20	mV	
Output current	IO ₁ -IO ₄				200		μA	2
Resistance between reference voltage input pins	RGMAH		VH ₀ -VH ₆₃		20		kΩ	
	RGMAL		VL ₀ -VL ₆₃		20		kΩ	

NOTES :

1. Criterion of evaluating voltage deviations.
 - (a) Between output voltage pins
Measuring values : Output voltage value at the time after
10 μ s at the rising edge of LS.
(Average of several times)
(Conditions) Output load capacity is 150 pF.
In a state when the reference voltage is fixed.
Expecting values : Calculated following these specifications.
(Conditions) In a state when the reference voltage is fixed.
 - (b) Between LCD drivers
Measuring values : Applicable to (a).
(Conditions) Applicable to (a).
Expecting values : Applicable to (a).
(Conditions) Applicable to (a).
Each input voltage between the LCD drivers must be made perfectly equal by connecting corresponding reference voltage input pins.
2. I_{O1} : Applied voltage = 8.0 V for output pins XO₁ to ZO₁₀₈.
Output voltage = 7.5 V for output pins XO₁ to ZO₁₀₈.
V_{LS} = 10.0 V
- I_{O2} : Applied voltage = 7.0 V for output pins XO₁ to ZO₁₀₈.
Output voltage = 7.5 V for output pins XO₁ to ZO₁₀₈.
V_{LS} = 10.0 V
- I_{O3} : Applied voltage = 3.0 V for output pins XO₁ to ZO₁₀₈.
Output voltage = 2.5 V for output pins XO₁ to ZO₁₀₈.
V_{LS} = 10.0 V
- I_{O4} : Applied voltage = 2.0 V for output pins XO₁ to ZO₁₀₈.
Output voltage = 2.5 V for output pins XO₁ to ZO₁₀₈.
V_{LS} = 10.0 V

AC Characteristics ($V_{CC} = +2.7$ to $+3.6$ V, $V_{LS} = +8.0$ to $+12.0$ V, $T_{OPR} = -20$ to $+75$ °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f _{CK}		CK			55	MHz
"H" level pulse width	t _{CWH}			4			ns
"L" level pulse width	t _{CWL}			4			ns
Input rise time	t _{CR}					10	ns
Input fall time	t _{CF}					10	ns
Data setup time	t _{SUD}		XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ , POLA, POLB	4			ns
Data hold time	t _{HD}			0			ns
Start pulse setup time	t _{SUSP}		SPIO, SPOI	4			ns
Start pulse hold time	t _{HSP}			0			ns
Start pulse width	t _{WSP}					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t _{DSP}	CL = 15 pF				12	ns
LCD drive output delay time 1	t _{DO1}	CL = 150 pF	XO ₁ -ZO ₁₀₈			3	μs
LCD drive output delay time 2	t _{DO2}	CL = 150 pF				10	μs
LS signal-SPI signal setup time	t _{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t _{HLS}			7			ns
LS signal "H" level width	t _{WLS}			$\frac{1}{f_{CK}}$			ns
REV signal-LS signal setup time	t _{SURV}		REV, REV ₂	14			ns
REV signal-LS signal hold time	t _{HRV}			10			ns

Timing Chart

