

LH1692

300-output TFT-LCD Gate Driver IC

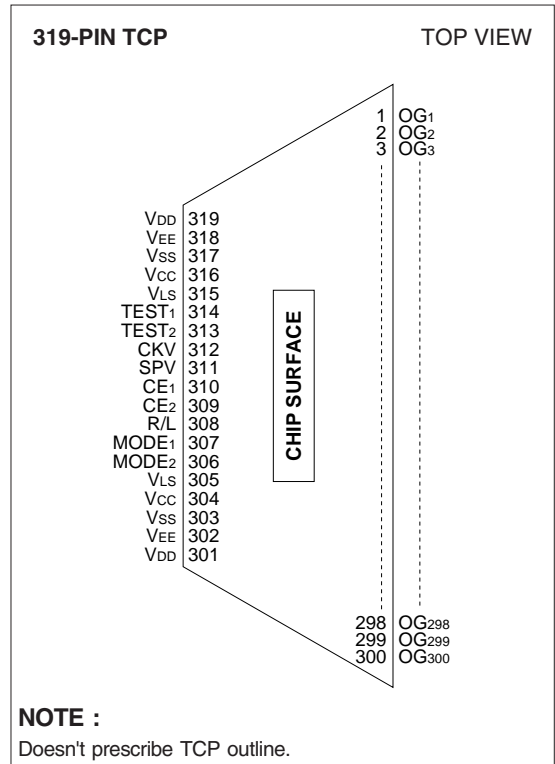
DESCRIPTION

The LH1692 is a 300-output TFT-LCD gate driver IC.

FEATURES

- Number of LCD drive outputs : 300
- LCD drive output sequence :
Output shift direction can be selected
OG₁→OG₃₀₀ or OG₃₀₀→OG₁
- Cascade connection :
Max. 4 cascades (internal counting system)
- Usable with both positive/negative power supplies
- Output mode selection
 - Normal mode (1-pulse scanning)
 - Continuous 2-pulse mode (2-pulse scanning)
 - Jumping 2-pulse mode (2-pulse scanning)
- LCD drive voltage : +16.0 to +42.0 V
- Operating temperature : -30 to + 85 °C
- Package : 319-pin TCP (Tape Carrier Package)

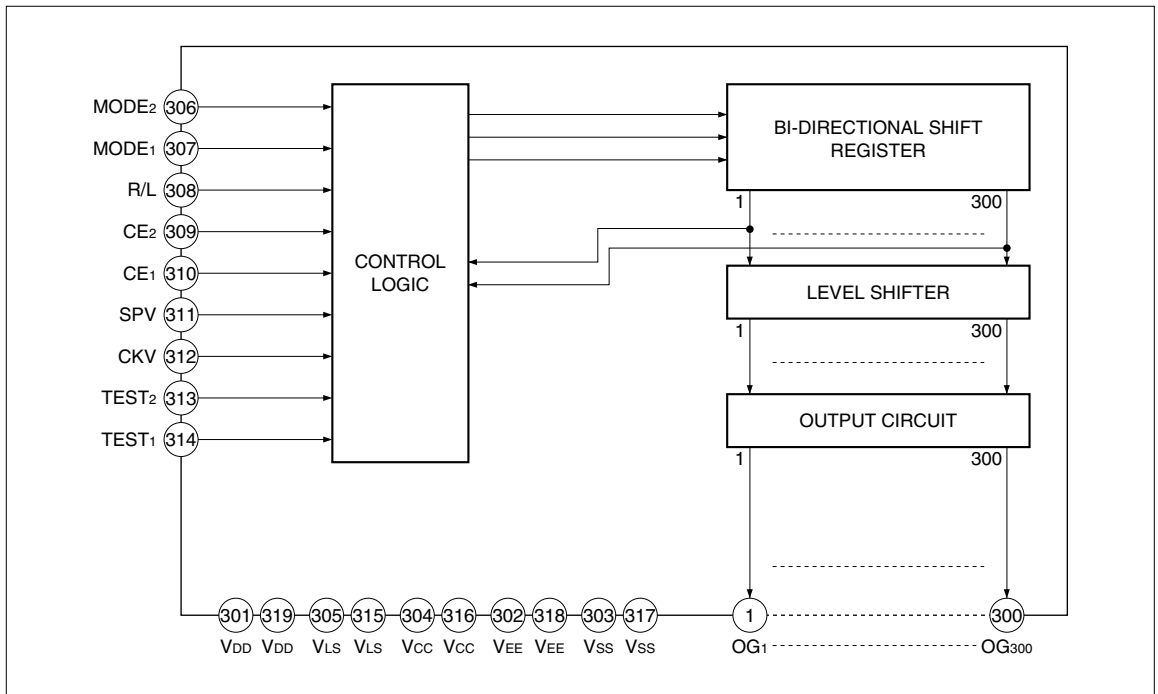
PIN CONNECTIONS



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 300	OG1-OG300	O	LCD drive output pins
301, 309	VDD	-	Power supply pins for LCD drive
302, 318	VEE	-	Power supply pins for LCD drive
303, 317	VSS	-	Power supply pins for logic system
304, 316	VCC	-	Power supply pins for logic system
305, 315	VLS	-	Power supply pins for input level shifter
306, 307	MODE2, MODE1	I	Output mode selection pins
308	R/L	I	Pin for selecting bi-directional shift register and setting cascade sequence
309, 310	CE2, CE1	I	Cascade sequence setting pins
311	SPV	I	Vertical scanning start pulse input pin
312	CKV	I	Vertical shift clock input pin
313, 314	TEST2, TEST1	I	IC test pins

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Control Logic	Used to create signals necessary for mode selecting signal, cascade sequence setting signal and for operation of bi-directional shift register.
Bi-directional Shift Register	Used as transfer circuit of LCD drive output start signal. It is possible to set LCD drive output sequence of OG ₁ →OG ₃₀₀ direction or OG ₃₀₀ →OG ₁ direction.
Level Shifter	Used as circuit which shifts LCD drive output signals transferred by bi-directional shift register to VDD-VEE level.
Output Circuit	Configured with output buffers to output VDD-VEE level.

INPUT/OUTPUT CIRCUITS

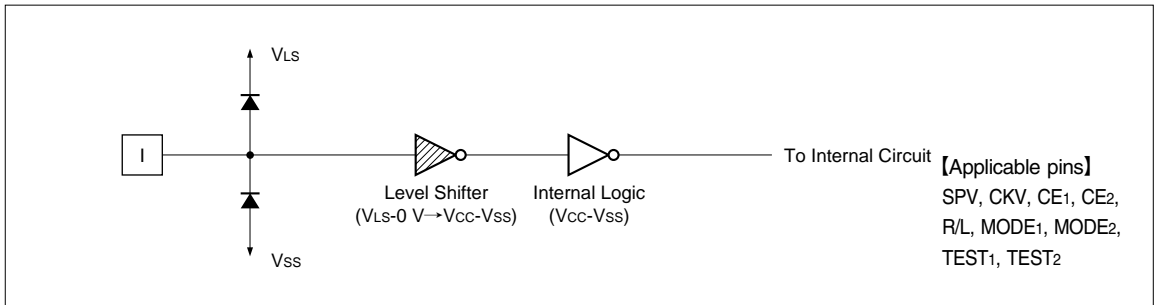


Fig. 1 Input Circuit

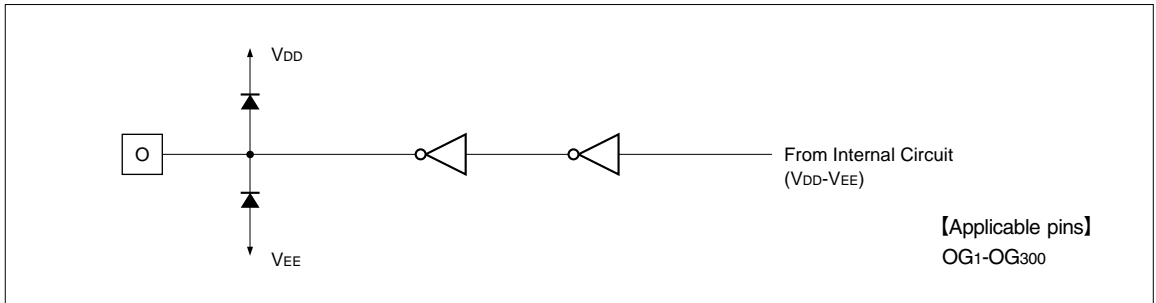


Fig. 2 Output Circuit

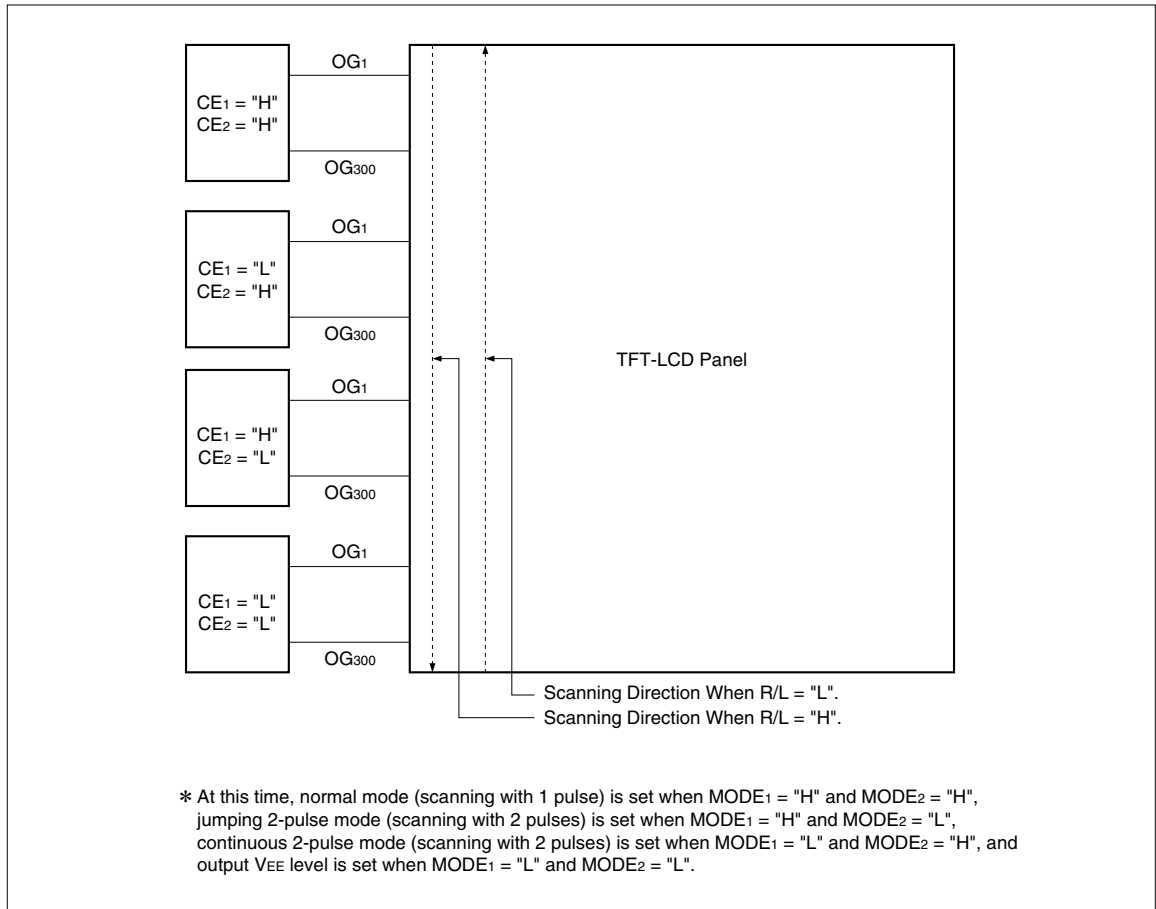
FUNCTIONAL DESCRIPTION

Pin Functions

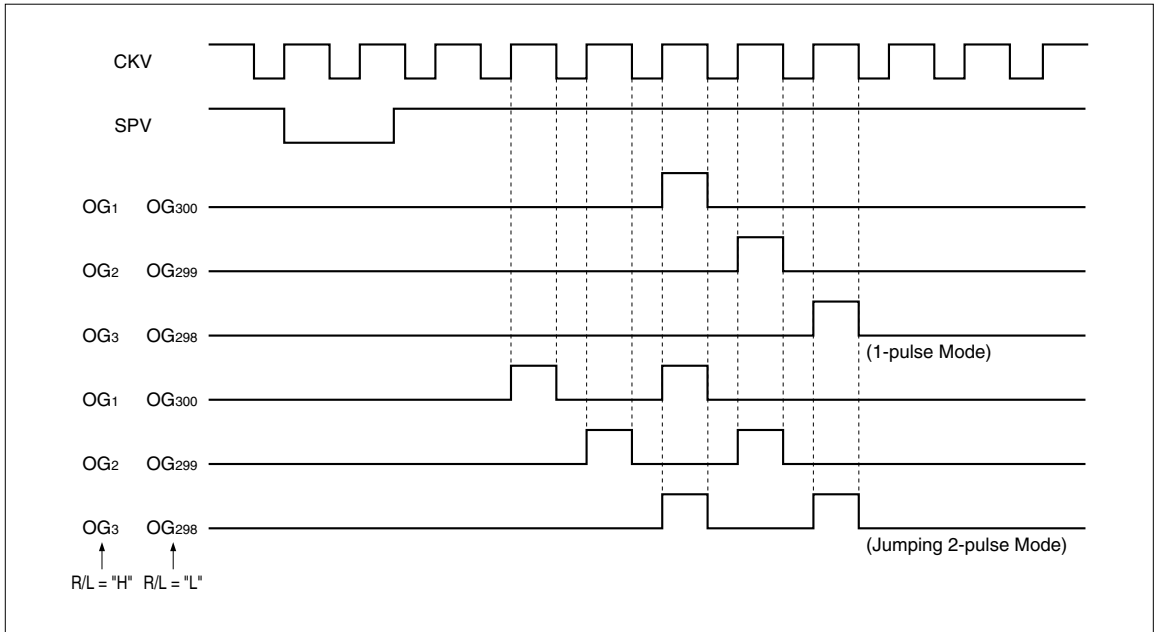
SYMBOL	FUNCTION																						
VDD	Used as power supply pin for high level LCD drive.																						
VLS	Used as power supply pin for input level shifters.																						
VCC	Used as power supply pin for logic system, normally connected to Vss + 5.0 V.																						
VEE	Used as power supply pin for low level LCD drive.																						
VSS	Used as logic system power supply pin.																						
CKV	Used as vertical shift clock pulse input pin.																						
SPV	Used as vertical scanning start pulse input pin. (At least, input one cycle of CKV during "L" period of SPV.)																						
MODE1 MODE2	<p>Used as input pins for selecting output mode. Output mode is set as shown in the table below by setting MODE1 pin and MODE2 pin.</p> <table border="1"> <thead> <tr> <th>MODE1</th> <th>MODE2</th> <th>Output mode</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>Normal mode (1-pulse scanning)</td> </tr> <tr> <td>L</td> <td>H</td> <td>Continuous 2-pulse mode</td> </tr> <tr> <td>H</td> <td>L</td> <td>Jumping 2-pulse mode</td> </tr> <tr> <td>L</td> <td>L</td> <td>Set all outputs to VEE level.</td> </tr> </tbody> </table>	MODE1	MODE2	Output mode	H	H	Normal mode (1-pulse scanning)	L	H	Continuous 2-pulse mode	H	L	Jumping 2-pulse mode	L	L	Set all outputs to VEE level.							
MODE1	MODE2	Output mode																					
H	H	Normal mode (1-pulse scanning)																					
L	H	Continuous 2-pulse mode																					
H	L	Jumping 2-pulse mode																					
L	L	Set all outputs to VEE level.																					
R/L	<p>Used as input pin for selecting the shift direction of bi-directional shift register and for setting the sequence of cascade connection. LCD drive outputs shift from OG1 to OG300 when set to "H". LCD drive outputs shift from OG300 to OG1 when set to "L". At the same time, cascade sequence is set as shown in the table below.</p>																						
CE1 CE2	<p>Used as input pins for setting of chip cascade sequence. (Max. 4 cascades)</p> <table border="1"> <thead> <tr> <th rowspan="2">CE1</th> <th rowspan="2">CE2</th> <th colspan="2">Cascade sequence</th> </tr> <tr> <th>R/L = "H"</th> <th>R/L = "L"</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>1st</td> <td>4th</td> </tr> <tr> <td>L</td> <td>H</td> <td>2nd</td> <td>3rd</td> </tr> <tr> <td>H</td> <td>L</td> <td>3rd</td> <td>2nd</td> </tr> <tr> <td>L</td> <td>L</td> <td>4th</td> <td>1st</td> </tr> </tbody> </table> <p>With above setting, sets the cascade sequence signal inside the IC.</p>	CE1	CE2	Cascade sequence		R/L = "H"	R/L = "L"	H	H	1st	4th	L	H	2nd	3rd	H	L	3rd	2nd	L	L	4th	1st
CE1	CE2			Cascade sequence																			
		R/L = "H"	R/L = "L"																				
H	H	1st	4th																				
L	H	2nd	3rd																				
H	L	3rd	2nd																				
L	L	4th	1st																				
TEST1 TEST2	<p>Used as input pins for IC testing. Must be set to "H".</p>																						
OG1-OG300	<p>Used as output pins for LCD drive output, and which output data at 2 levels.</p> <ul style="list-style-type: none"> • Selecting data is output at VDD level . • Non-selecting data is output at VEE level . 																						

Functional Operations

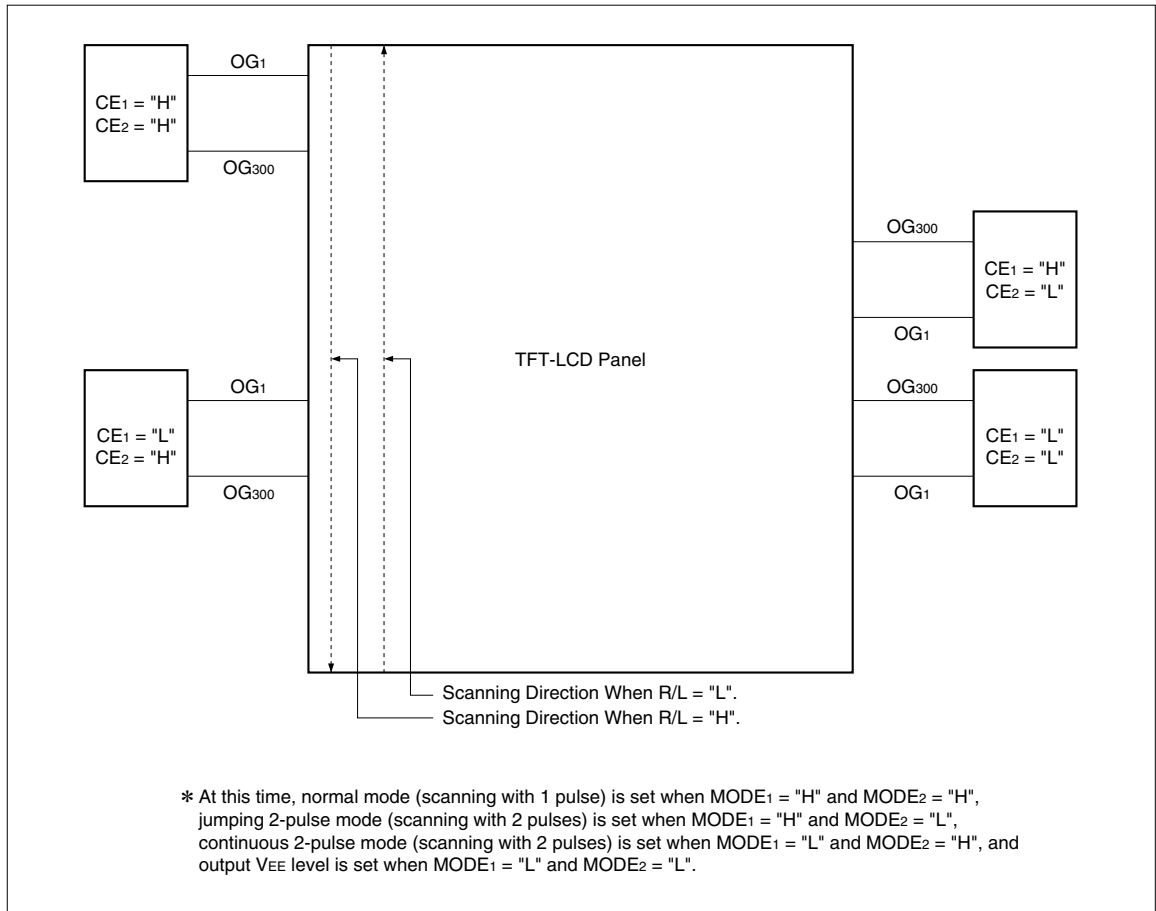
(1) Example of Cascade Sequence (One Side Assembled)



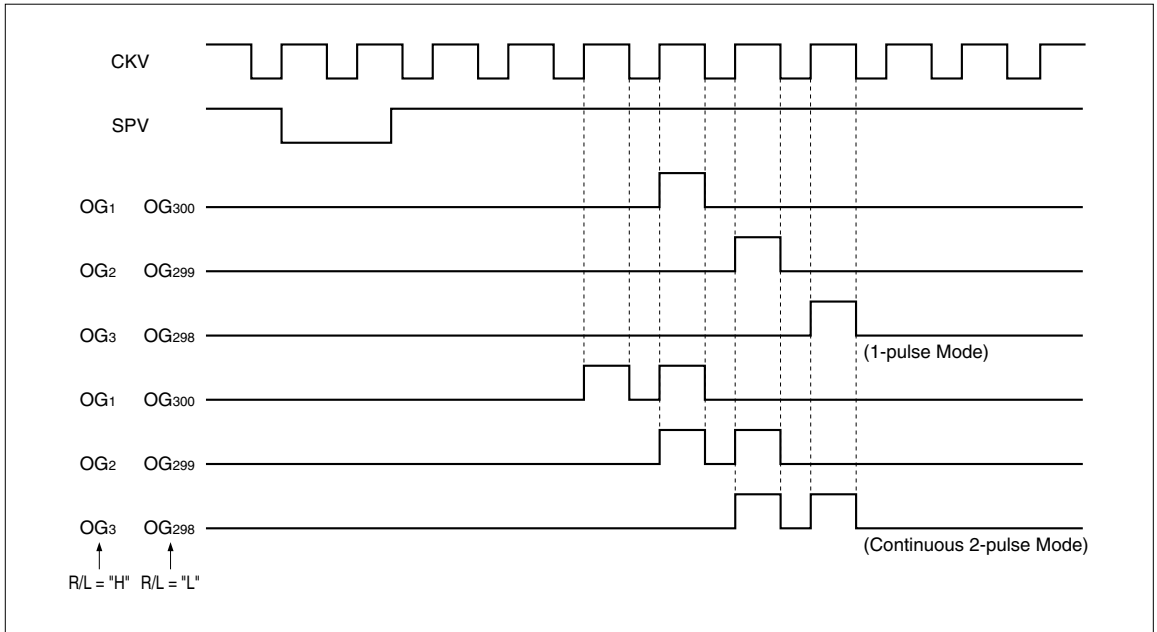
(2) Example of Input/Output Timing (For 1st Cascade Sequence)



(3) Example of Cascade Sequence (Both Side Assembled)



(4) Example of Input/Output Timing (For 1st Cascade Sequence)



PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

Logic system power supply (V_{LS}) or internal logic system power supply (V_{SS} , V_{CC} ; $V_{CC} > V_{SS}$) → logic input → LCD drive power supply (V_{EE} , V_{DD})

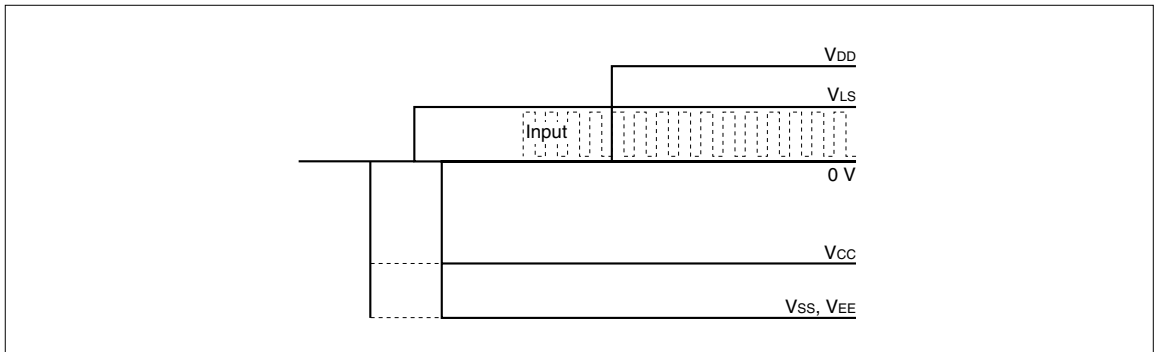
It is possible to set voltage V_{EE} to the same as V_{SS} . When connecting the power supply when $V_{EE} = V_{SS}$, observe the following sequence and the recommended sequence figure shown below.

Logic system power supply (V_{LS}), internal logic system power supply (V_{SS} , V_{CC} ; $V_{CC} > V_{SS}$) and low-level LCD drive power supply (V_{EE}) → logic input → high-level LCD drive power supply (V_{DD})

When disconnecting the power supply, follow the reverse sequence.

Since the logic state of the internal circuit is unstable immediately after the logic system power is supplied, input CKV and SPV while initializing the internal circuit (minimum input clock number is 300 CKV).

MODE1 and MODE2 should be set to "L" during the initializing period for setting the LCD drive output to V_{EE} level.



Input pin setting

Input pins other than CKV and SPV must be set to "H" or "L" level.

Maximum ratings

When connecting or disconnecting the power, this IC must be used within the range of the absolute maximum ratings.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V _{DD}	V _{DD}	-0.3 to +45.0	V	1, 2
	V _{LS}	V _{LS}	-0.3 to +7.0	V	
	V _{CC} - V _{SS}	V _{CC} , V _{SS}	-0.3 to +7.0	V	
	V _{EE} - V _{SS}	V _{EE} , V _{SS}	-0.3 to +45.0	V	
	V _{DD} - V _{EE} (V _{SS})	V _{DD} , V _{EE} , V _{SS}	-0.3 to +45.0	V	
Input voltage	V _{IN}	CKV, SPV, CE ₁ , CE ₂ , R/L, MODE1, MODE2, TEST ₁ , TEST ₂	-0.3 to V _{LS} + 0.3	V	
Storage temperature	T _{STG}		-45 to +125	°C	

NOTES :

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to 0 V.

RECOMMENDED OPERATING CONDITIONS

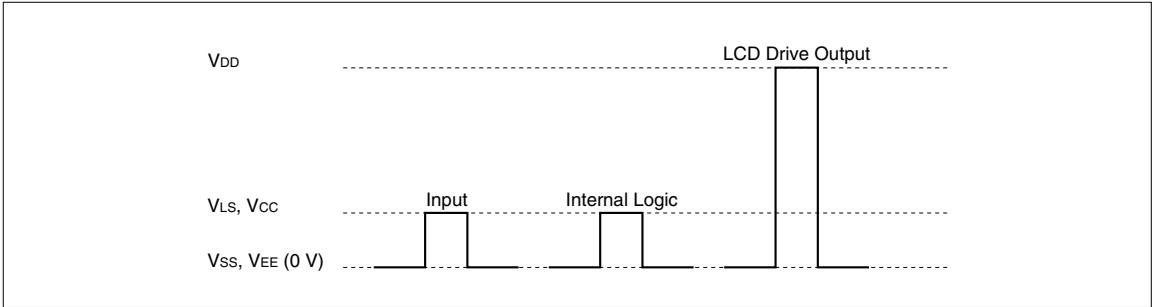
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V _{DD}	+5.5	+9.0	+42.0	V	1, 2
	V _{LS}	+3.0	+5.0	+5.5	V	
	V _{CC} - V _{SS}	+3.0	+5.0	+5.5	V	
	V _{EE} - V _{SS}	0		+11.0	V	
	V _{DD} - V _{EE} (V _{SS})	+16.0	+25.0	+42.0	V	
Input voltage	V _{IN}	0		V _{LS}	V	
Operating temperature	T _{OPR}	-30		+85	°C	

NOTES :

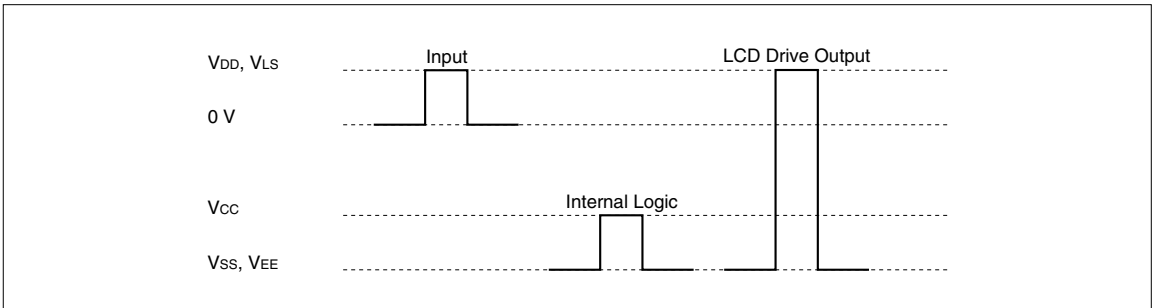
1. The applicable voltage on any pin with respect to 0 V.
2. Ensure that voltages are set as follows.
 - V_{SS}, V_{EE} ≤ 0 V
 - V_{CC} - V_{SS} = V_{LS} ± 0.1 V (For 3.3 V specifications)
 - V_{CC} - V_{SS} = V_{LS} ± 0.2 V (For 5.0 V specifications)
 - V_{CC} ≤ V_{LS}

When power supply pins are set as shown below, the LH1692 can output positive voltage and negative voltage to LCD drive output.

Example 1 : For Positive Voltage Output



Example 2 : For Negative Voltage Output



ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{LS} = +3.3±0.3 V (= V_{CC} - V_{SS}), V_{EE} = V_{SS}, T_{OPR} = -30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		CKV, SPV, MODE ₁ ,			0.2V _{LS}	V	
Input "High" voltage	V _{IH}		MODE ₂ , CE ₁ , CE ₂ , R/L	0.8V _{LS}			V	
Output "Low" voltage	V _{OL}	I _{OL} = 0.4 mA	OG ₁ -OG ₃₀₀			V _{EE} + 0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -0.4 mA		V _{DD} - 0.4			V	
Input "Low" current	I _{IL}	V _I = 0 V	CKV, SPV, MODE ₁ ,			5.0	μA	
Input "High" current	I _{IH}	V _I = V _{LS}	MODE ₂ , CE ₁ , CE ₂ , R/L			5.0	μA	1
Supply current (1)	I _{DD}	For 1-pulse mode				60	μA	2
	I _{LS}					130	μA	
	I _{CC}					80	μA	
	I _{EE}					50	μA	
Supply current (2)	I _{DD}	For jumping 2-pulse mode				130	μA	3
	I _{LS}					200	μA	
	I _{CC}					90	μA	
	I _{EE}					50	μA	
Supply current (3)	I _{DD}	For continuous 2-pulse mode				130	μA	4
	I _{LS}					200	μA	
	I _{CC}					90	μA	
	I _{EE}					90	μA	

NOTES :

- All input pins : 3.3 V
- CKV : Frequency = 31 kHz, "L" period width t_{wL} = 16.2 μs
SPV : Frequency = 60 Hz
Other input pins : 3.3 V
All output pins are opened.
- CKV : Frequency = 31 kHz, "L" period width t_{wL} = 16.2 μs
SPV : Frequency = 60 Hz
MODE₂ : 0 V
Other input pins : 3.3 V
All output pins are opened.
- CKV : Frequency = 31 kHz, "L" period width t_{wL} = 16.2 μs
SPV : Frequency = 60 Hz
MODE₁ : 0 V
Other input pins : 3.3 V
All output pins are opened.

($V_{LS} = +5.0 \pm 0.5 \text{ V} (= V_{CC} - V_{SS})$, $V_{EE} = V_{SS}$, $T_{OPR} = -30 \text{ to } +85 \text{ }^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		CKV, SPV, MODE ₁ ,			0.2 V_{LS}	V	
Input "High" voltage	V_{IH}		MODE ₂ , CE ₁ , CE ₂ , R/L	0.8 V_{LS}			V	
Output "Low" voltage	V_{OL}	$I_{OL} = 0.4 \text{ mA}$	OG1-OG ₃₀₀			$V_{EE} + 0.4$	V	
Output "High" voltage	V_{OH}	$I_{OH} = -0.4 \text{ mA}$		$V_{DD} - 0.4$			V	
Input "Low" current	I_{IL}	$V_I = 0 \text{ V}$	CKV, SPV, MODE ₁ ,			5.0	μA	
Input "High" current	I_{IH}	$V_I = V_{LS}$	MODE ₂ , CE ₁ , CE ₂ , R/L			5.0	μA	1
Supply current (1)	IDD	For 1-pulse mode				60	μA	2
	ILS					180	μA	
	ICC					100	μA	
	IEE					50	μA	
Supply current (2)	IDD	For jumping 2-pulse mode				130	μA	3
	ILS					300	μA	
	ICC					150	μA	
	IEE					50	μA	
Supply current (3)	IDD	For continuous 2-pulse mode				130	μA	4
	ILS					300	μA	
	ICC					150	μA	
	IEE					50	μA	

NOTES :

- All input pins : 5 V
- CKV : Frequency = 31 kHz, "L" period width $t_{wL} = 16.2 \mu\text{s}$
SPV : Frequency = 60 Hz
Other input pins : 5 V
All output pins are opened.
- CKV : Frequency = 31 kHz, "L" period width $t_{wL} = 16.2 \mu\text{s}$
SPV : Frequency = 60 Hz
MODE₂ : 0 V
Other input pins : 5 V
All output pins are opened.
- CKV : Frequency = 31 kHz, "L" period width $t_{wL} = 16.2 \mu\text{s}$
SPV : Frequency = 60 Hz
MODE₁ : 0 V
Other input pins : 5 V
All output pins are opened.

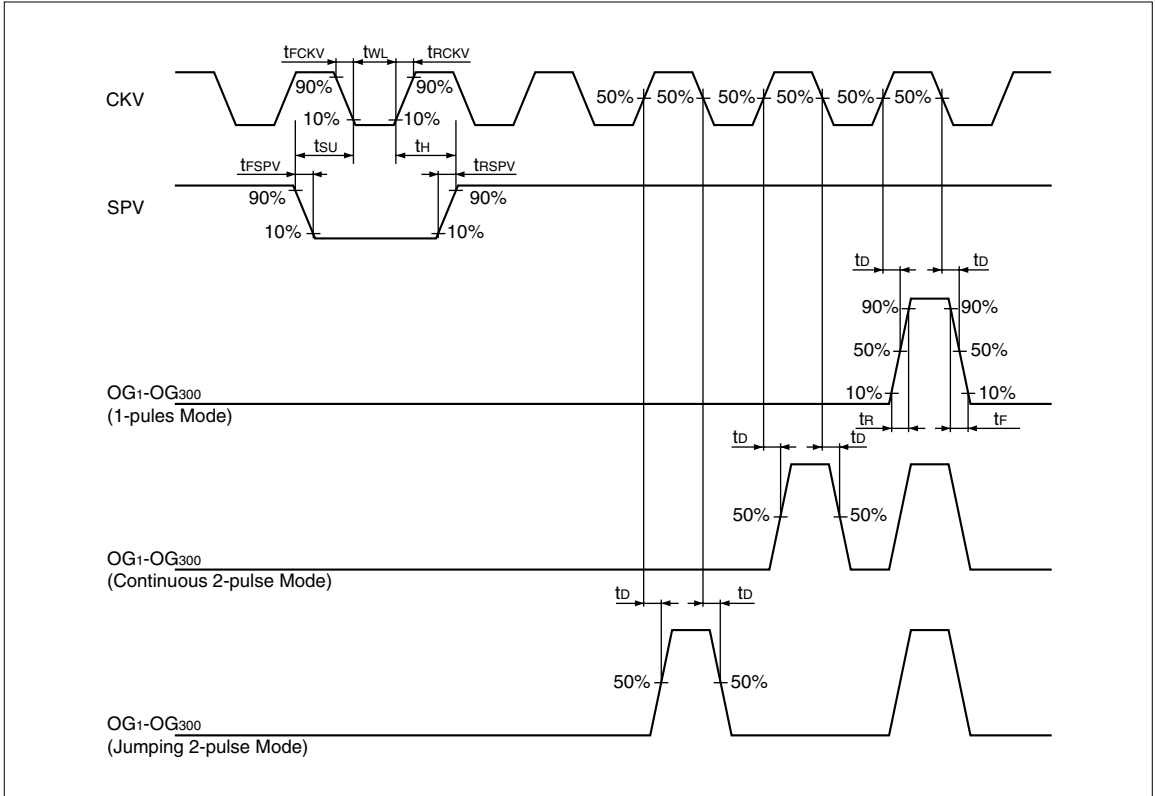
AC Characteristics ($V_{LS} = +3.3 \pm 0.3 \text{ V} (= V_{CC} - V_{SS})$, $V_{EE} = V_{SS}$, $T_{OPR} = -30 \text{ to } +85 \text{ } ^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f _{CKV}		CKV			100	kHz
"L" clock pulse width	t _{WL}			0.5			μs
Clock rise time	t _{RCKV}					100	ns
Clock fall time	t _{FCKV}					100	ns
Data setup time	t _{SU}		CKV, SPV	100			ns
Data hold time	t _H			300			ns
Pulse rise time	t _{RSPV}		SPV			100	ns
Pulse fall time	t _{FSPV}					100	ns
Output transfer delay time	t _d	C _L = 500 pF	OG1-OG300			3.0	μs
Output rise time	t _R					1.0	μs
Output fall time	t _F					1.0	μs

($V_{LS} = +5.0 \pm 0.5 \text{ V} (= V_{CC} - V_{SS})$, $V_{EE} = V_{SS}$, $T_{OPR} = -30 \text{ to } +85 \text{ } ^\circ\text{C}$)

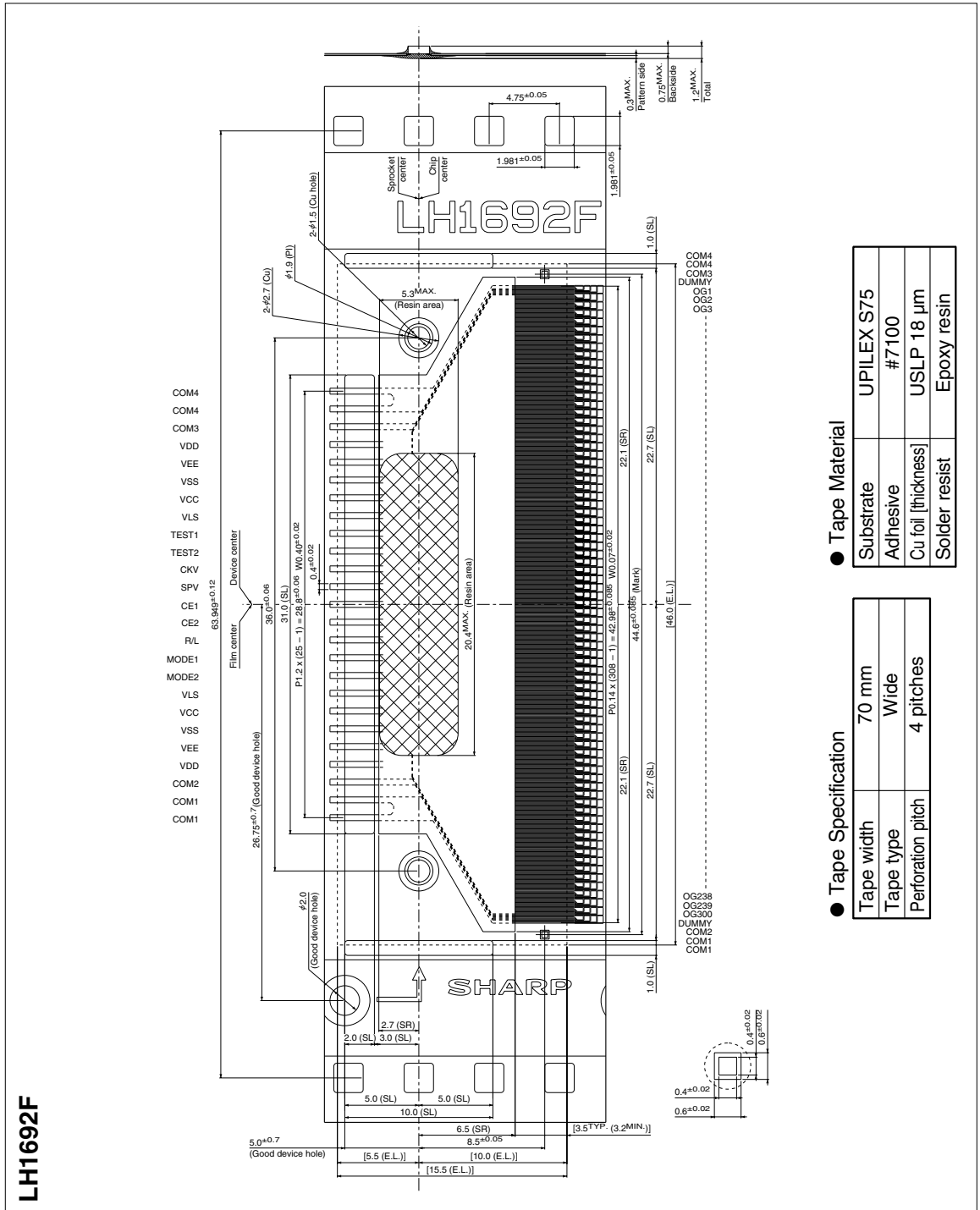
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f _{CKV}		CKV			100	kHz
"L" clock pulse width	t _{WL}			0.5			μs
Clock rise time	t _{RCKV}					100	ns
Clock fall time	t _{FCKV}					100	ns
Data setup time	t _{SU}		CKV, SPV	100			ns
Data hold time	t _H			300			ns
Pulse rise time	t _{RSPV}		SPV			100	ns
Pulse fall time	t _{FSPV}					100	ns
Output transfer delay time	t _d	C _L = 500 pF	OG1-OG300			2.0	μs
Output rise time	t _R					1.0	μs
Output fall time	t _F					1.0	μs

Timing Chart



PACKAGE

(Unit : mm)



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