National Semiconductor

LH2011/LH2011B/LH2011C Dual Operational Amplifiers

General Description

The LH2011 series of dual operational amplifiers contain a pair of LM11 op amps in a single hermetic package, combining the best features of existing bipolar and FET op amps. The LH2011 is similar to the LH2108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been improved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and the low drift makes compensation practical. Offset current is almost unmeasurable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (**– 55°C** to **125°C**) are:

- Offset voltage: 100 μV (**200 μV**)
- Bias current: 25 pA (**65 pA**)
- Offset current: 0.5 pA (**3 pA**)
- Temperature drift: **1 μV/°C**
- Long-term stability: 10 μV/year

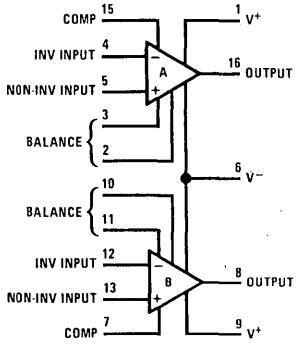
The LH2011 is internally compensated, but external compensation may be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low-resistance potentiometer.

Otherwise, the device is the electrical equivalent of the LH2108, except that the negative common-mode limit is 0.6V less, performance is specified down to ±2.5V and the guaranteed output drive has been increased to ±2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

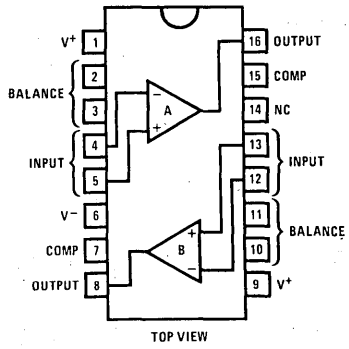
The LH2011 has applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations. The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LH2011 is manufactured with standard bipolar processing using super-gain transistors.

Connection Diagrams

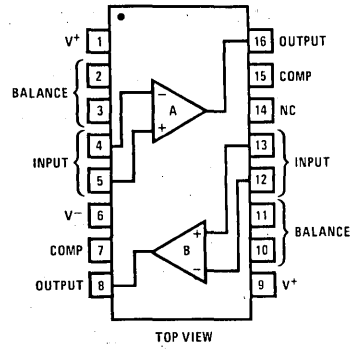


Dual-In-Line Package



Order Number LH2011D, LH2011BD, or LH2011CD
See Package D16C

Flat Package



Order Number LH2011F or LH2011BF
See Package F16B

Absolute Maximum Ratings

V_S	Total Supply Voltage	40V
I_{IN}	Input Current (Note 1)	± 10 mA
P_D	Power Dissipation at 25°C Derate Linearly above 100°C at 100°C/W	500 mW
I_{SC}	Output Short-Circuit Duration (Note 2)	Indefinite
T_J	Junction Temperature	150°C
T_{stg}	Storage Temperature Range	−65°C to +150°C
T_A	Operating Temperature Range	
	LH2011CD	−25°C to +85°C
	LH2011D, LH2011F	−55°C to +125°C
	LH2011BD, LH2011BF	−55°C to +125°C
	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_J \leq T_{MAX}$ unless noted.

Parameter		Conditions		LH2011			LH2011B			LH2011C			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	Note 3	$T_J = 25°C$		0.1	0.3		0.2	0.6		0.5	1	mV
						0.6			1.1			1.3	
I_{OS}	Input Offset Current		$T_J = 25°C$		0.5	10		1	10		4	25	pA
						30			30			50	
I_B	Input Bias Current		$T_J = 25°C$		25	50		40	100		70	180	pA
						150			300			400	
R_{IN}	Input Resistance				10^{11}			10^{11}			10^{11}		Ω
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift	Note 4			1	3		2	5		3		μV/°C
$\Delta I_B/\Delta T$	Bias Current Drift				0.5	1.5		0.8	3		1.4		pA/°C
$\Delta I_{OS}/\Delta T$	Offset Current Drift				20			20			50		fA/°C
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $I_O = \pm 2$ mA	$T_J = 25°C$, $V_O = \pm 12V$	100	300		100	300		50	300		V/mV
		$V_O = \pm 11.5V$		50			50			15			
		$V_S = \pm 15V$, $I_O = \pm 0.5$ mA	$T_J = 25°C$, $V_O = \pm 12V$	250	1200		250	1200		90	800		
		$V_O = \pm 11.5V$		100			100			30			
CMRR	Common-Mode Rejection		$T_J = 25°C$	110	130		110	130		96	110		dB
		$V_{CM} = -13V, +14V$		100			100			90			
PSRR	Power Supply Rejection Ratio		$T_J = 25°C$	100	118		100	118		84	100		dB
		$V_S = \pm 2.5V$ to $\pm 20V$		96			96			80			
I_S	Supply Current		$T_J = 25°C$		0.3	0.6		0.3	0.8		0.3	0.8	mA
						0.8			1			1	
I_{SC}	Output Short Circuit Current	$T_J = T_{MAX}$			±15			±15			±15		mA

Note 1: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch-up initiated by supply reversals.

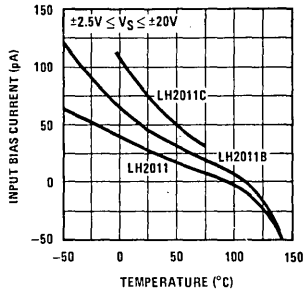
Note 2: Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

Note 3: These specifications apply for test at $V_S = \pm 15V$ and $V_{CM} = -12.5V$ (−13V at 25°C), 14V; $V_S = \pm 20V$ and $V_{CM} = 0V$; in addition, V_{OS} is also tested at $V_S = \pm 2.5V$ and $V_{CM} = 0V$.

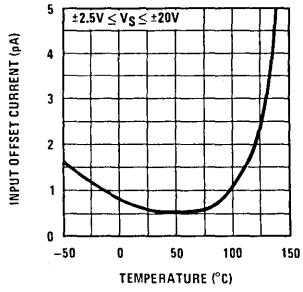
Note 4: Drift parameters are sample tested to 5% LTPD at the same conditions as Note 3. The values are average-calculated from measurements at 25°C and 125°C.

Typical Characteristics (for single device)

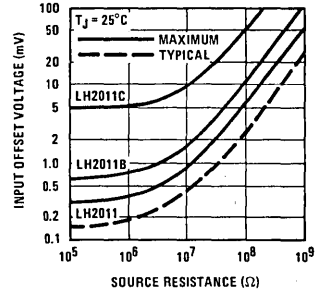
Input Bias Current



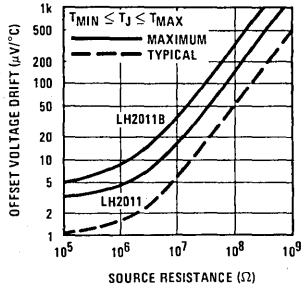
Input Offset Current



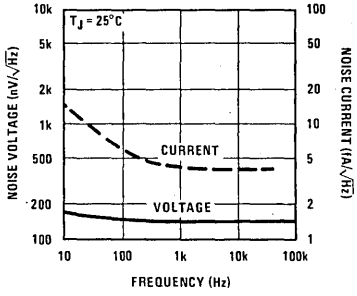
Offset: Single Source Resistor (Unbalanced)



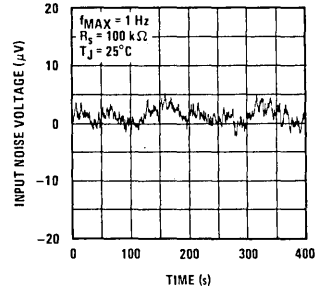
Drift: Single Source Resistor (Unbalanced)



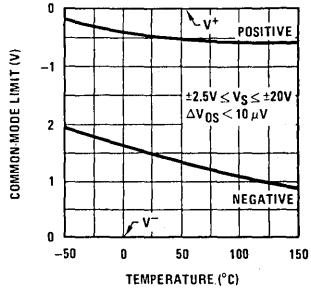
Equivalent Input Noise



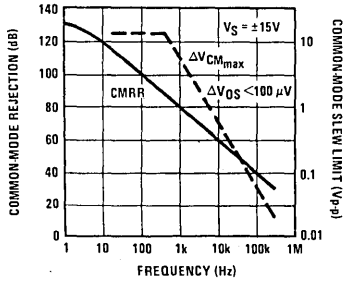
Input Noise



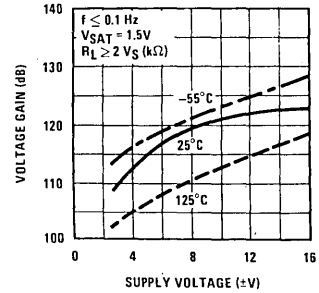
Input Common-Mode Limits



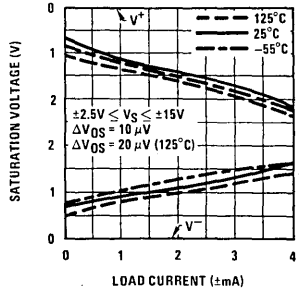
Common-Mode Rejection



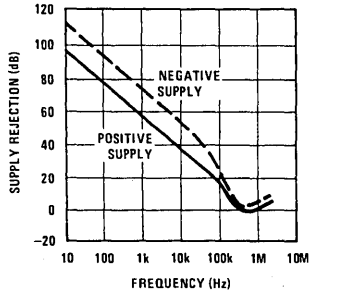
Large Signal Voltage Gain



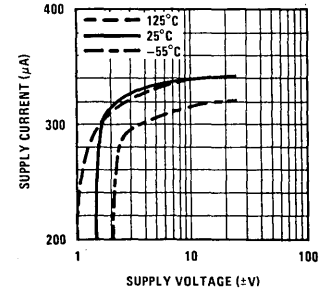
Output Saturation Threshold



Supply Rejection

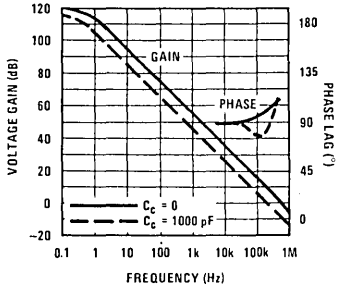


Supply Current (Each Amplifier)

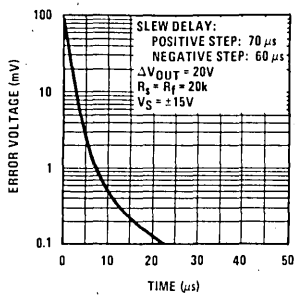


Typical Characteristics (Continued) (for single device)

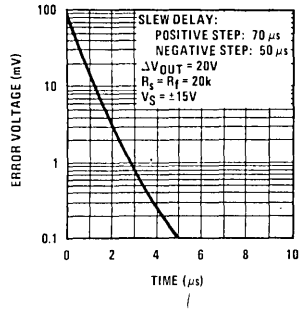
Open Loop Response



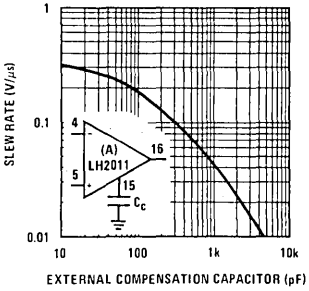
Follower Settling Time



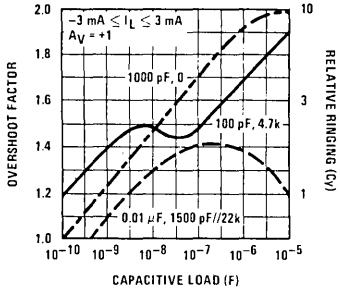
Inverter Settling Time



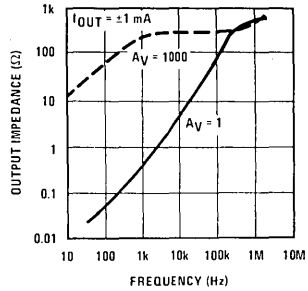
Slew Rate



Stability with Over-Compensation



Closed Loop Output Impedance



Application Hints

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, the floating metal lid is best connected to the guard. This might be accomplished with a dab of conductive paint connecting the metal lid to the "no-connection" pin 14.

Electrostatic shielding of high impedance circuitry is advisable.

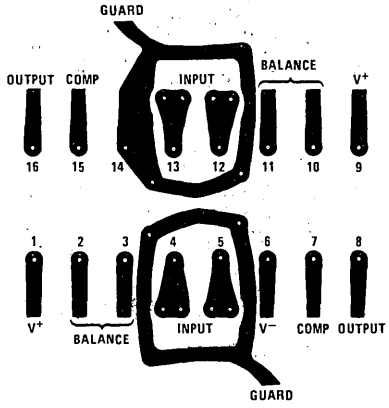
Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 µV/°C for copper-kovar) and internal resistor connections. Problems can be avoided by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together can also help.

With the LH2011 there is a temptation to remove the bias-current-compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3V. The potential problem involves the loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the input of the device is not limited to less than 100 mA or if there is much more than 1 µF bypass on the supply buss.

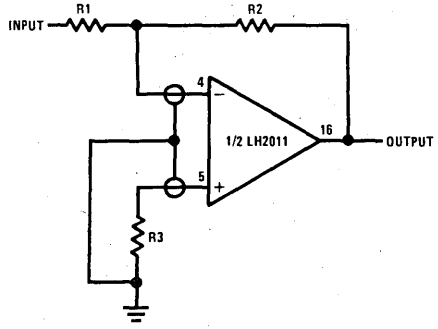
Although these difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH2011.

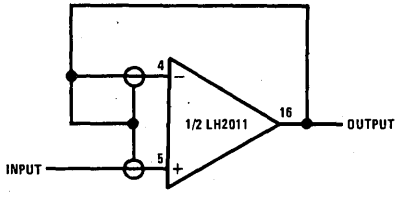
Input Guarding

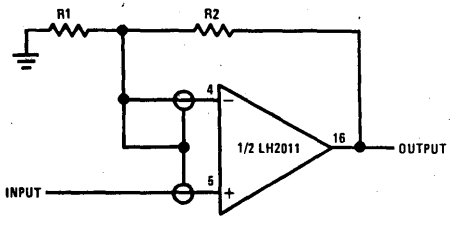
Input guarding can drastically reduce surface leakage. Layout for the LH2011 is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.



Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are shown here.

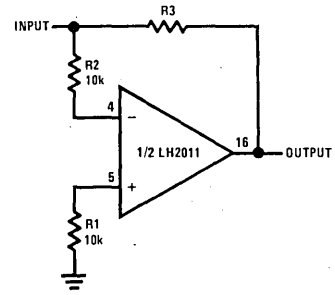




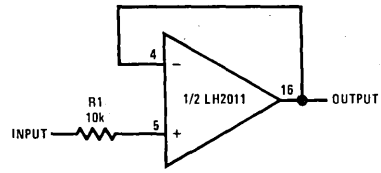


Input Protection

Current is limited by R2 even when input is connected to voltage source outside common-mode range. If one supply reverses, current is limited by R1. These resistors do not affect normal operation.

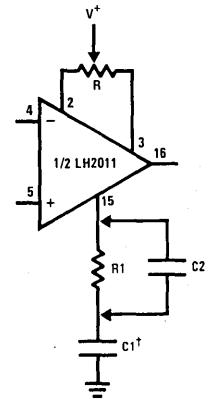


Input resistor limits current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.



Balancing and Over-Compensation

Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.

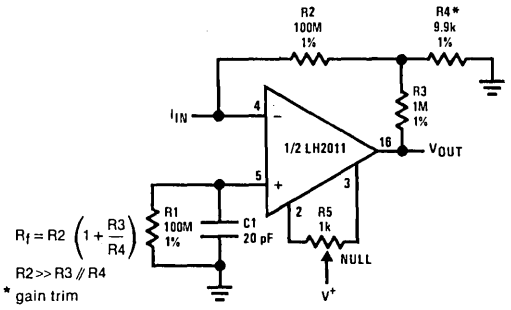


Min Adj Range	R
±5 mV	100 kΩ
±2	10k
±1	3k
±0.8	3k
±0.4	1k

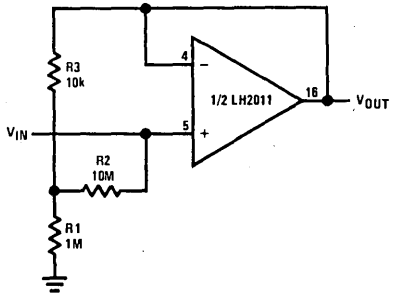
†See stability with over-compensation curve

Resistance Multiplication

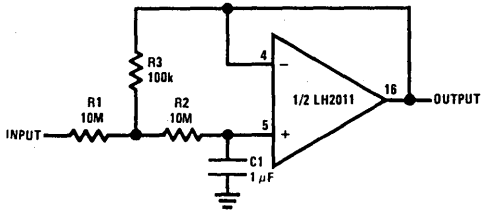
Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.



Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not significant because the op amp offset is low.



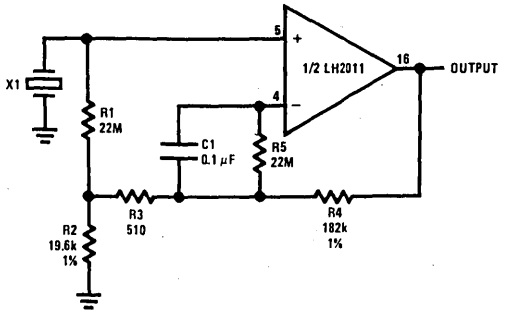
This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.



$$\tau = \frac{R1\,C}{R3}(R2+R3)$$

$$\Delta V_{OUT} = \frac{R1+R3}{R3}(I_B R2 + V_{OS})$$

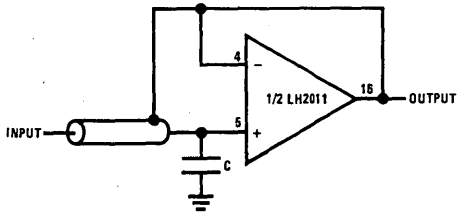
A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.



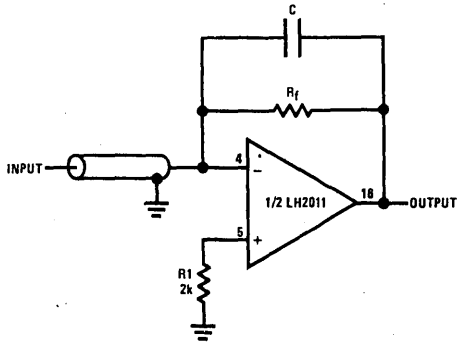
$$R_{IN} = R1\left(1+\frac{R2}{R3}\right) \quad A_V = \frac{R2+R3+R4}{R2+R3}$$

Cable Bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage, and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.



With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

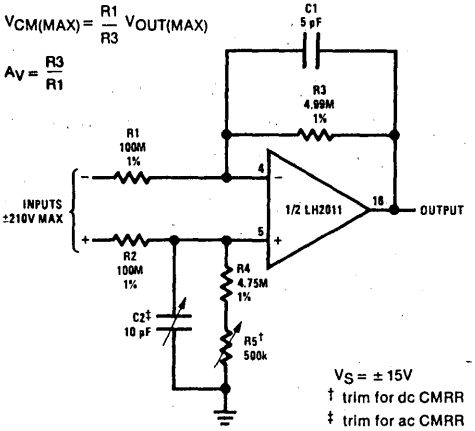


Differential Amplifiers

This differential amplifier handles high input voltages. Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.

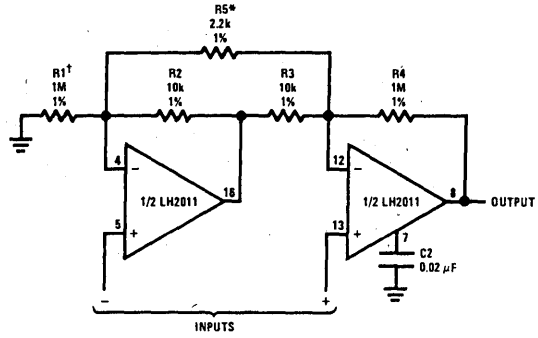
$V_{CM(MAX)} = \frac{R1}{R3} V_{OUT(MAX)}$

$A_V = \frac{R3}{R1}$



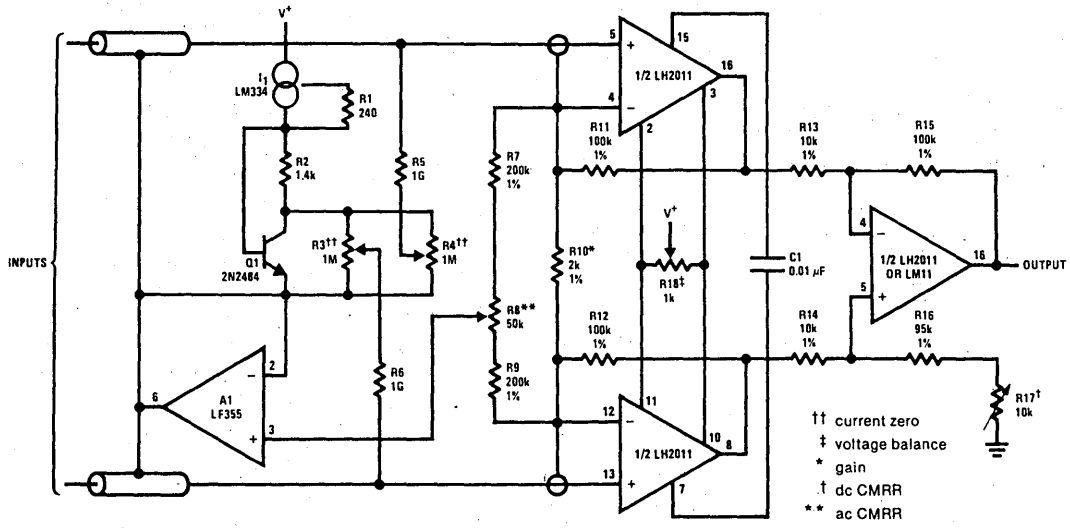
$V_S = \pm 15V$
† trim for dc CMRR
‡ trim for ac CMRR

Two op-amp instrumentation amplifier has poor ac common-mode rejection. This can be improved at the expense of differential bandwidth with C2.

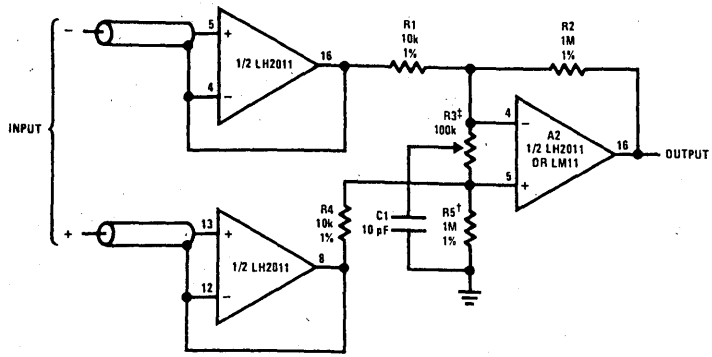


* gain set
† trim for dc CMRR
$f_O = 10$ Hz

High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.



For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A2 must also have low drift.



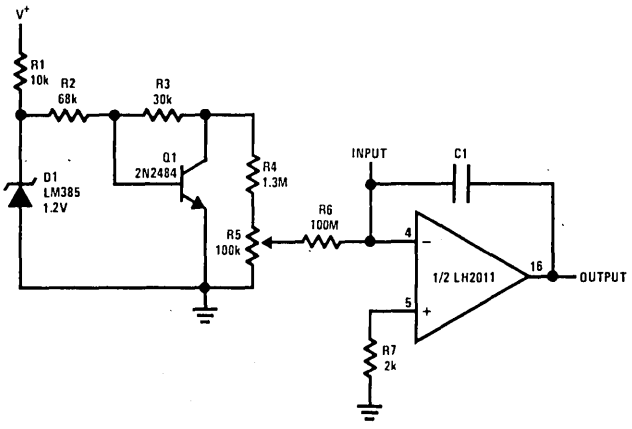
$R1 = R3;\ R2 = R4$

$A_V = \frac{R2}{R1}$

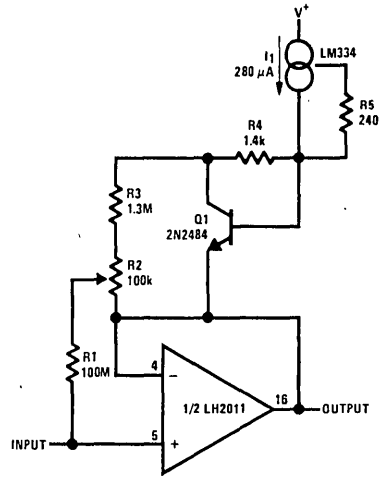
†trim for dc CMRR
‡set for ac CMRR

Bias Current Compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.

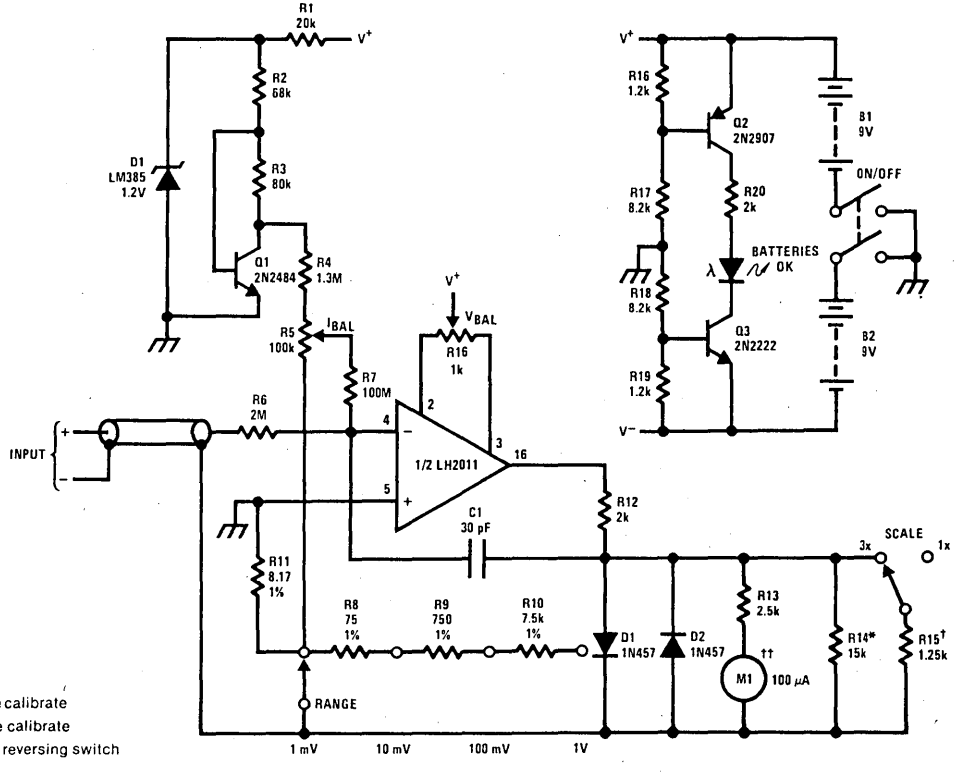


This circuit shows how bias current compensation can be used on a voltage follower.



Voltmeter

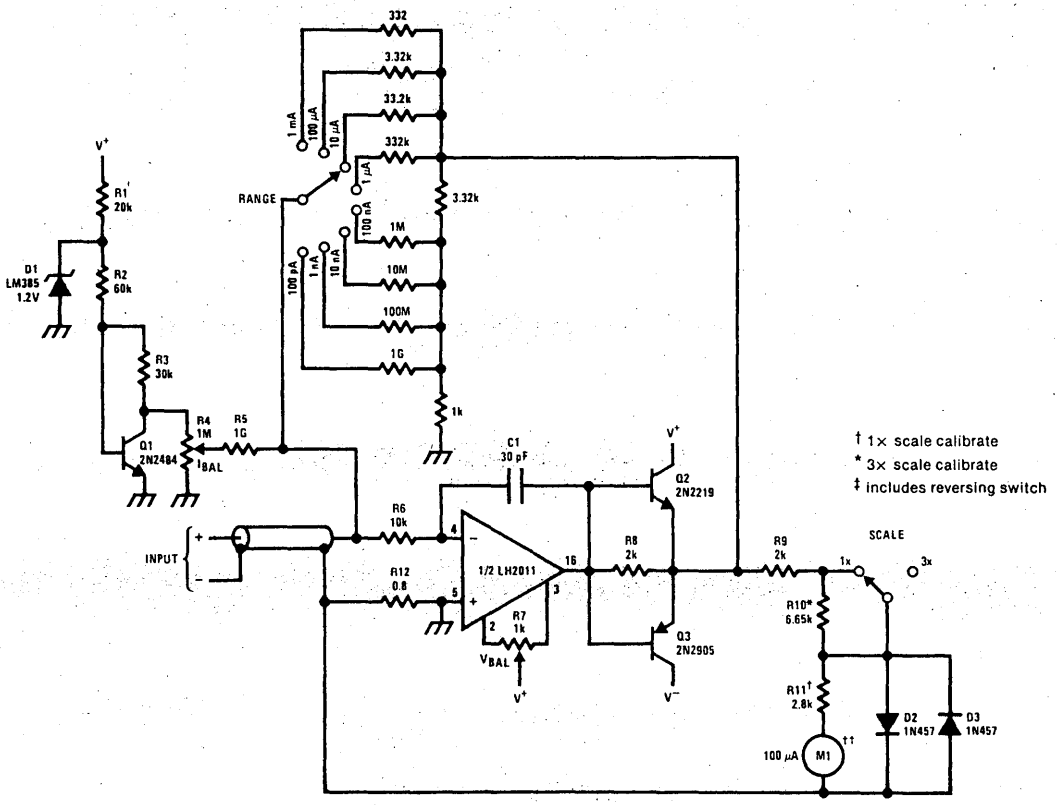
High-input-impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full-scale. Reference could be used to make direct reading linear ohmmeter.



* 1× scale calibrate
† 3× scale calibrate
‡ includes reversing switch

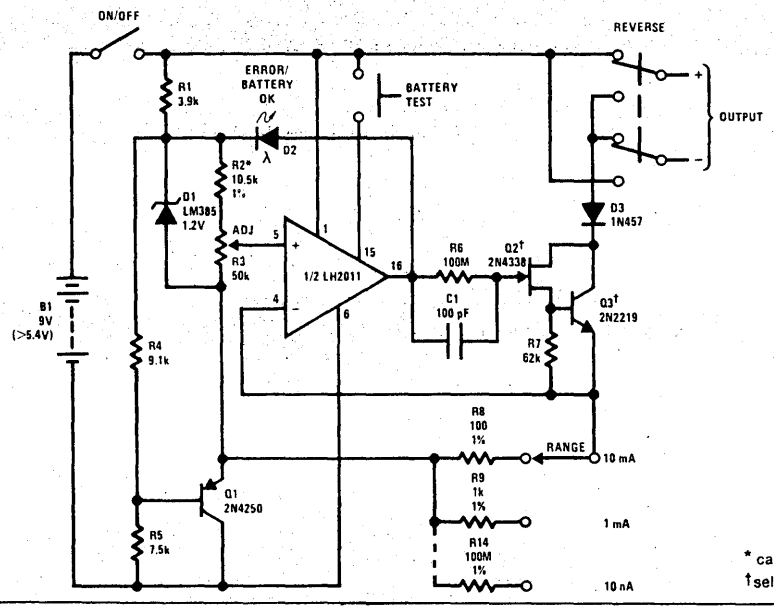
Ammeter

Current meter ranges from 100 pA to 3 mA full-scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.



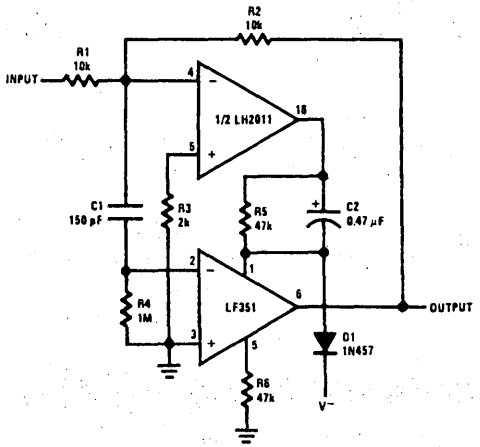
Current Source

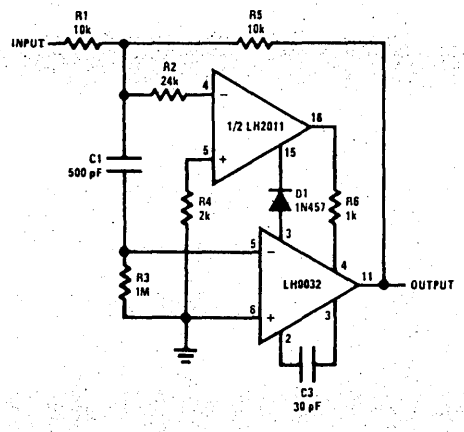
Precision current source has 10 μA to 10 mA ranges with output compliance of 30V to −5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.



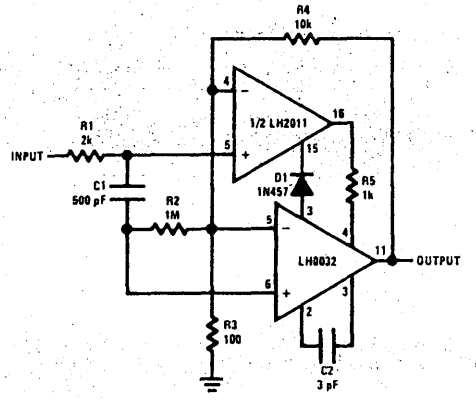
Fast Amplifiers

These inverters have bias current and offset voltage of LH2011 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 μs. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.

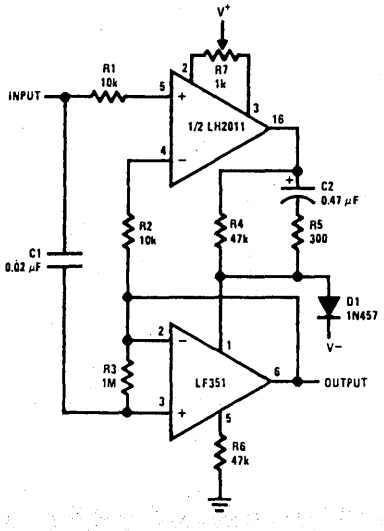




This 100× amplifier has small and large signal bandwidth of 1 MHz. The LH2011 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.

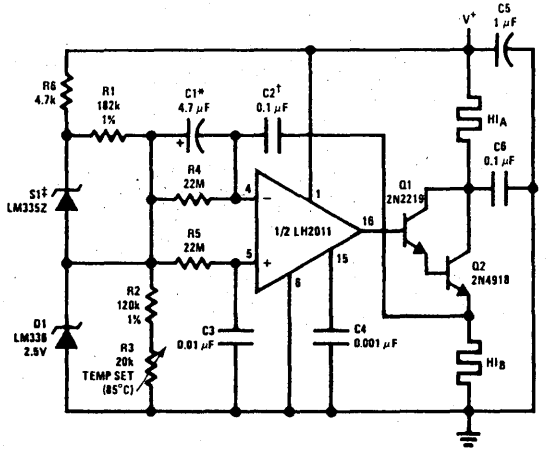


Follower has 10 μs settling to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.



Heater Control

Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.



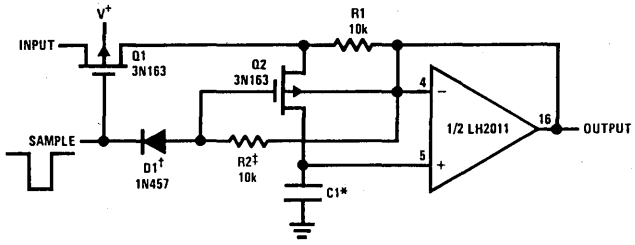
* solid tantalum

† mylar

‡ close thermal coupling between sensor and oven shell is recommended.

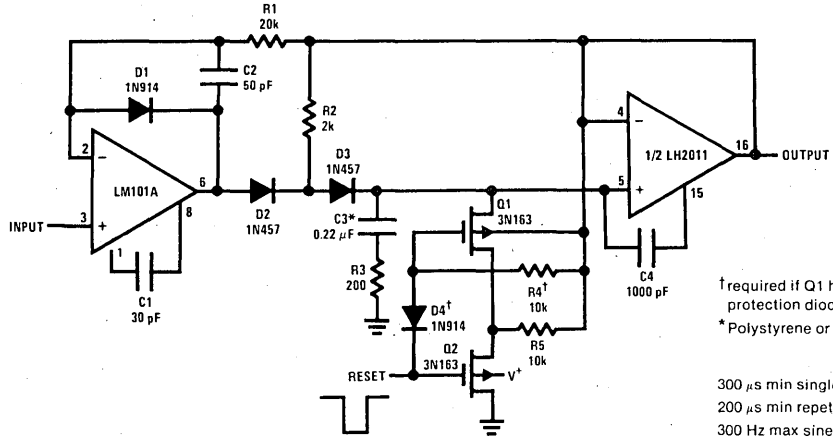
Leakage Isolation

Switch leakage in this sample and hold does not reach storage capacitor.



* Polystyrene or Teflon
† required if protected-gate switch is used

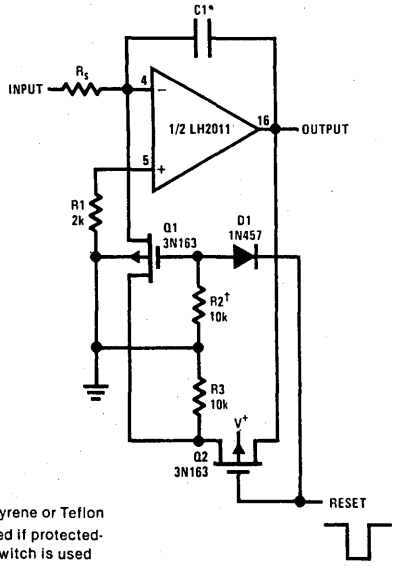
A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.



† required if Q1 has gate-protection diode
* Polystyrene or Teflon

300 μs min single pulse
200 μs min repetitive pulse
300 Hz max sine wave error < 5 mV

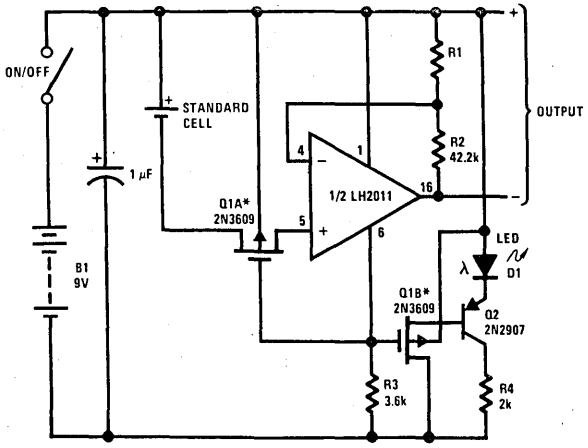
Reset is provided for this integrator and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.



* Polystyrene or Teflon
† required if protected-gate switch is used

Standard-Cell Buffer

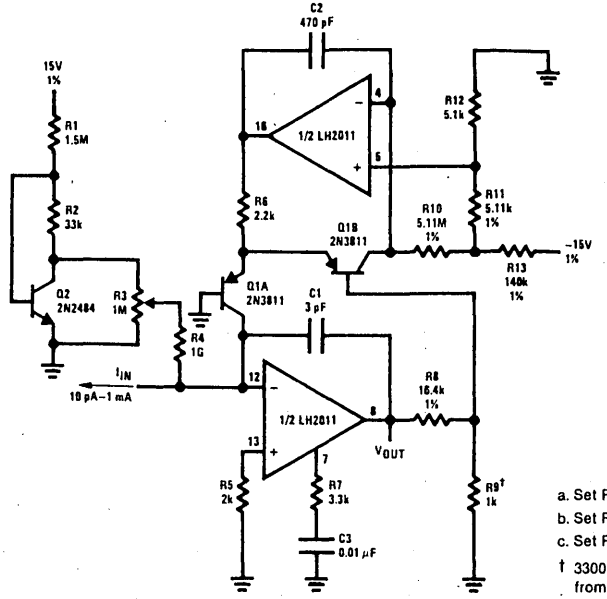
Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.



* cannot have gate-protection diode; $V_{TH} > V_{OUT}$

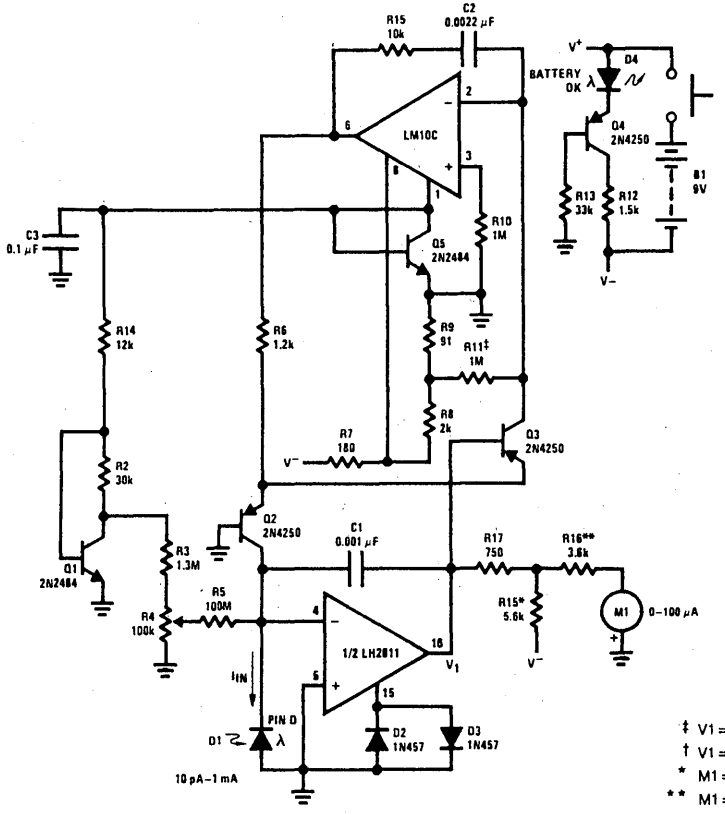
Logarithmic Amplifiers

Unusual frequency compensation gives this logarithmic converter a 100 μs time constant from 1 mA down to 100 μA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.



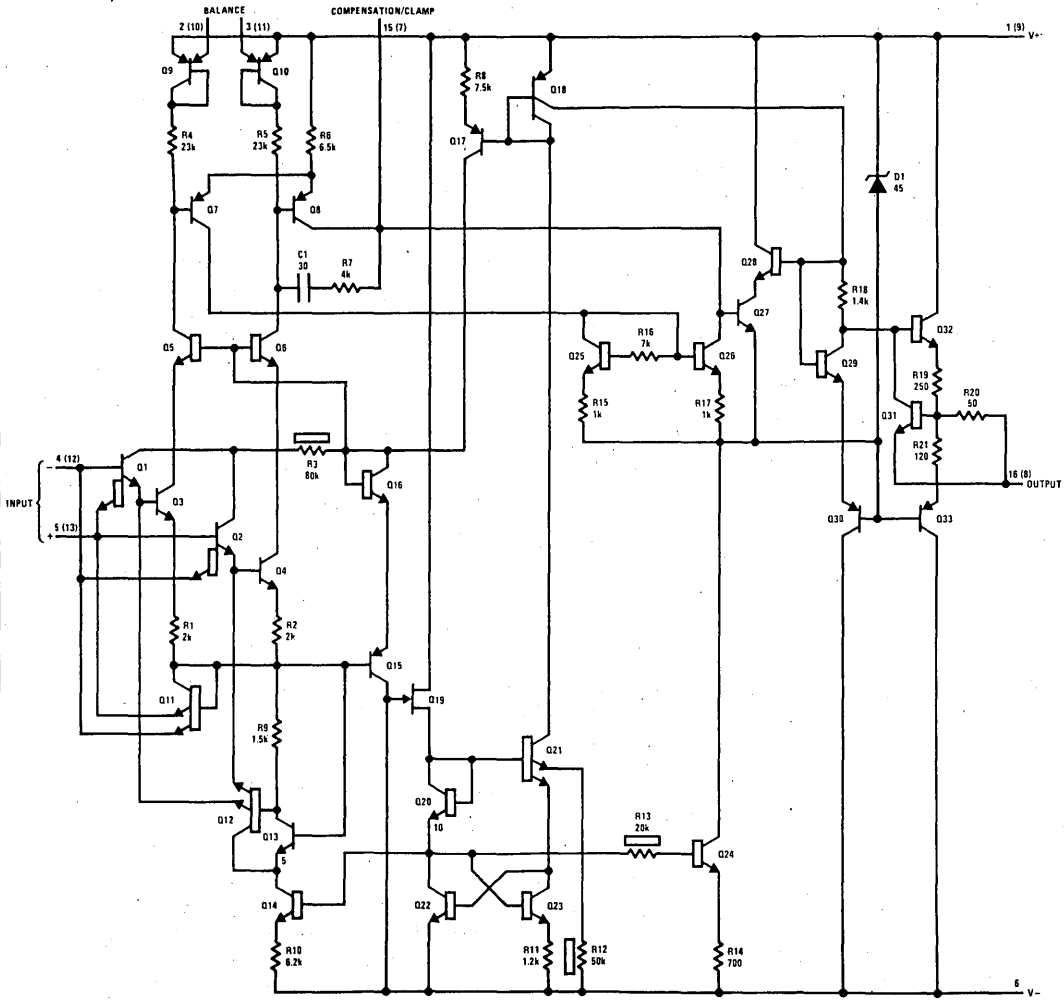
a. Set R11 for $V_{OUT} = 0$ at $I_{IN} = 100\ \mu A$
b. Set R8 for $V_{OUT} = 3V$ at $I_{IN} = 100\ \mu A$
c. Set R3 for $V_{OUT} = -4V$ at $I_{IN} = 10$ pA
† 3300 ppm/°C. Type Q209 available from Tel Labs, Inc., Manchester, N.H.

Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.



‡ $V1 = 0$ @ $I_{IN} = 100$ nA
† $V1 = -0.24V$ @ $I_{IN} = 10$ pA
* $M1 = 0$ @ $I_{IN} = 10$ pA
** $M1 = f_S$ @ $I_{IN} = 1$ mA

Schematic Diagram (for single device)



Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Temperature drift: The change of a parameter measured at 25°C and either temperature extreme divided by the temperature change.

Supply-voltage rejection: The ratio of the specified supply-voltage change (either or both supplies) to the change in offset voltage between the extremes.

Supply current: The current required from the power source to operate the amplifier with the output unloaded and operating in the linear range.