Preliminary Version

SPECIFICATION
FOR
APPROVAL

(●) Preliminary Specification
( ) Final Specification

Title	2.4"(240×320) 262K Color AMOLED Module.

BUYER	
MODEL	

SUPPLIER	LG Display Co., Ltd.
MODEL	LH240Q02
SUFFIX	ED01

SIGNATURE	DATE
/	
/	
/	

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OLED Product Development Team
LG Display Co., Ltd

CONTENTS

No.	Item	Page
0	Record of Revisions	3
1	General Description	4
2	Absolute Maximum Ratings	6
3	Electrical Characteristics	7
4	Optical Characteristics	19
5	Mechanical Characteristics	23
6	Reliability Test	24
7	Packing	25
8	Precautions	28
9	Inspection Standard	30
10	Appendix. - External Interface	32

RECORD OF REVISIONS

Revision No.	Revision Date	Page	Summary
0.0	June. 03. 2008	-	Preliminary CAS Release.
0.1	July. 15. 2008		External I/F(RGB, SPI, I2C)

1. General Description

The LH240Q02-ED01 is a Color Active Matrix Organic Light Emitting Diode Product Model. The matrix employs poly-Si Thin Film Transistor as Backplane. And This OLED Model use digital driving method. It has 2.4inch diagonally active display area with qVGA(240×RGBx320) resolution. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes.

1.1 Block Diagram

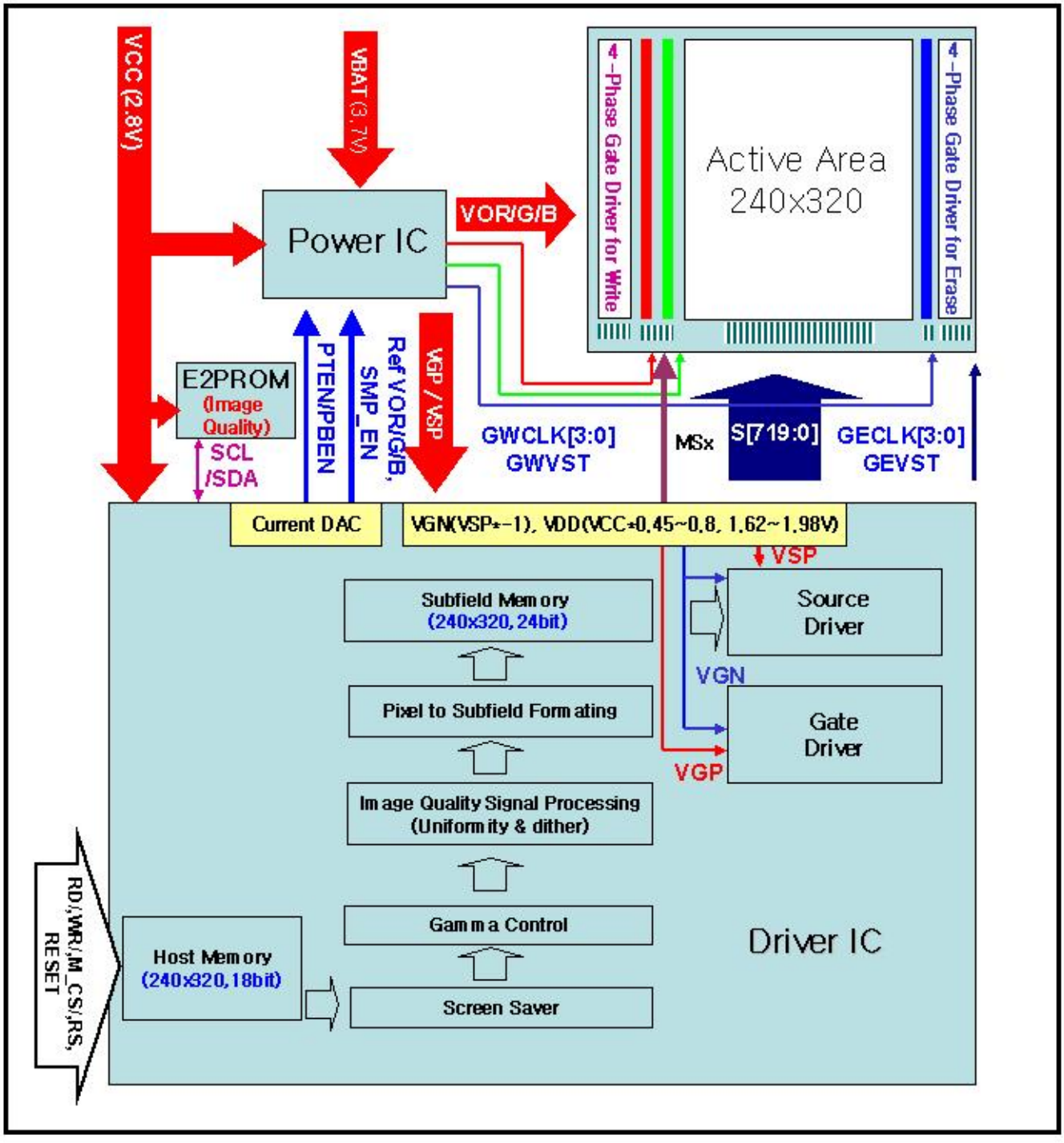


Fig 1.1. Block Diagram

1.2 General Features

Display Color	262K Color (65K Color is selective)
Pixel format (Resolution)	240(H) × 320(V) (RGB Stripe)
Display Mode	Normally Black, Organic Light Emitting Diode
Interface	18bit / 16bit / 9bit / 8bit CPU interface.(Recommendable) ※ RGB I/F & SPI I/F available
Driver IC	LGDP4234 (1 Chip IC / LGE SIC)
Polarizer	Hard coating Polarizer

The contents provide general mechanical characteristics for the model LH240Q02-ED01. In addition the figures in the next are detailed mechanical drawing of the OLED Module.

Item		Specification	Unit
Dimensional Outline	Horizontal	**41.48 ± 0.2**	mm
	Vertical	**73.83 ± 0.2**	mm
	Thickness	**1.5 ± 0.05**	mm
Number of Dots		**240(H)×RGB×320(V)**	dots
Panel Size		**40.88(H)×58.98(V)**	mm
Polarizer Area		**40.2(H)×53.5(V)**	mm
Active Area		**36.72(H)×48.96(V)**	mm
Diagonal Inch		**2.41**	Inch
Pixel Pitch		**0.153(H)×0.153(V)**	mm
Aperture Ratio		**21.2 / 21.2 / 43.7**	%
Weight		**9.5**	g
Glass Thickness		**0.5 ± TBD**	mm

2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 2.1. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Internal logic voltage	V_{CC}	-0.3	3.6	V	1
Interface I/O voltage	IOV_{VCC}	-0.3	3.6	V	1
Input Voltage	V_{BATT}	-0.3	5	V	
Static electricity	V_{SE}	-	±2	KV	
Storage Humidity	H_{stg}	10	90	%(RH)	
Storage Temperature	T_{stg}	-40	80	℃	3
Operating Ambient Humidity	H_{opr}	10	90	%(RH)	2
Operating Ambient Temperature	T_{opr}	-30	70	℃	2

Note 1) If the supply voltage is over, the LSI is all-destroyed.
So, in operating, recommend on using the LSI in maximum rating spec

Note 2) Although humidity is 90%, if operating temperature is over 60℃.
We can't guarantee good driving.

Note 3) Absolute humidity shall be less than 80% RH at 70℃, 24hr

3. Electrical Specifications

3-1. Electrical Characteristics

Table 3.1. ELECTRICAL CHARACTERISTICS

ITEM			Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Logic		IOV_{CC}	1.65	2.8	3.3	V
			V_{CC}	2.6	2.8	3.3	V
	Driving		V_{BATT}	2.8	3.7	4.5	V
Input Voltage for Logic Circuit	High		VIH	$0.8\times IOV_{CC}$	-	IOV_{CC}	V
	Low		VIL	-0.3	-	$0.2\times IOV_{CC}$	V
Output Voltage for Logic Circuit	High		VOH	$0.8\times IOV_{CC}$	-	-	V
	Low		VOL	-	-	$0.2\times IOV_{CC}$	V
Current Consumption	Logic		I_{CC}	-	15	25	mA
	I_{BATT}	30% On (2)	I_{BATT}	-	60	-	mA
	Power save mode (3)		I_{DSTB}		1	10	μA
Power Consumption (1)	Logic		P_{ICC}	-	42	70	mW
	BATT		P_{BATT}			-	
		30% On		-	225	-	mW
Frame Frequency FLM	Normal display			-	60	-	Hz

※ **Power Consumption Measure Condition**

(1) 230[cd/㎡], VCC=2.8[V], I/O VCC=2.8[V], VBATT=3.7[V], Ta=25[℃]
- Power Consumptions were measured under the condition of 30% white pixel on. (include in logic current consumption.)

(2) Measure current consumption of the display pattern
- 30% On current consumption test Pattern

(3) We can calculate I_{DSTB} In condition Display off mode & Power save set and refer to page 18.

3. Electrical Specifications

3-2. Interface Connections

The pin connections are provided in Table 3.2. The mating connector for the flex tail is IRISO IMSA-9671S-35Y902 or equivalent.

Table 3.2. PIN DESCRIPTION

PIN No.	SIGNAL	I/O	FUNCTION	Comment
1	GND	-	Ground	-
2	VBAT	-	Power supply for Power IC (Typical 3.7V)	-
3	VBAT	-		
4	VBAT	-		
5	GND	-	Ground	-
6	WP	I/O	EEPROM Write Protect	WP
7	SCL	I/O	Clock line of I2C signal	SCL
8	SDA	I/O	Data line of I2C signal	SDA
9	IM0	I	MPU interface mode select signal	IM0
10	RESET	I	Reset (Active Low)	RESET
11	D15	I/O	Data Bus (Instruction & Display Data)	DB15
12	D14	I/O	Data Bus (Instruction & Display Data)	DB14
13	D13	I/O	Data Bus (Instruction & Display Data)	DB13
14	D12	I/O	Data Bus (Instruction & Display Data)	DB12
15	D11	I/O	Data Bus (Instruction & Display Data)	DB11
16	D10	I/O	Data Bus (Instruction & Display Data)	DB10
17	D9	I/O	Data Bus (Instruction & Display Data)	DB9
18	D8	I/O	Data Bus (Instruction & Display Data)	DB8
19	D7	I/O	Data Bus (Instruction & Display Data)	DB7
20	D6	I/O	Data Bus (Instruction & Display Data)	DB6
21	D5	I/O	Data Bus (Instruction & Display Data)	DB5
22	D4	I/O	Data Bus (Instruction & Display Data)	DB4
23	D3	I/O	Data Bus (Instruction & Display Data)	DB3
24	D2	I/O	Data Bus (Instruction & Display Data)	DB2
25	D1	I/O	Data Bus (Instruction & Display Data)	DB1
26	D0	I/O	Data Bus (Instruction & Display Data)	DB0
27	RD	I	Read Strobe (Active Low)	RD
28	WR	I	Write Strobe (Active Low)	WR
29	RS	I	Resister Select	RS
30	CS	I	Chip Select (Active Low)	CS
31	FLM	I/O	Frame head pulse signal. Leave the pin open when not in use.	FLM
32	GND	-	Ground	-
33	VCC1	-	Analog Circuit & Interface I/O Power (Typical 2.8V)	-
34	VCC2	-		
35	GND	-	Ground	-

3. Electrical Specifications

3-3. Interface Timing

Table 3.3. Register Selection(80-system 8-/9-/16-/18/bit Parallel Interface)

80-system I/F			Function
WR*	RD*	RS	
0	1	0	Write an index to IR
1	0	0	Read an internal status
0	1	1	Write to control registers or the internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

(a) 16-bit Interface Mode

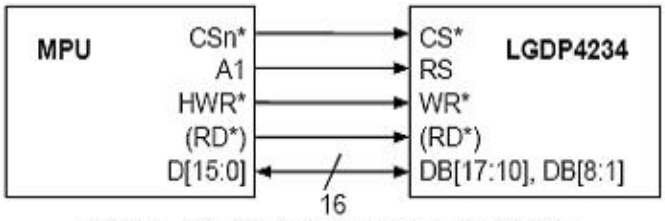
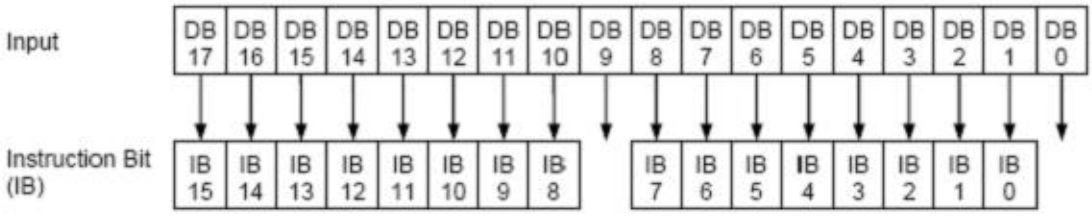
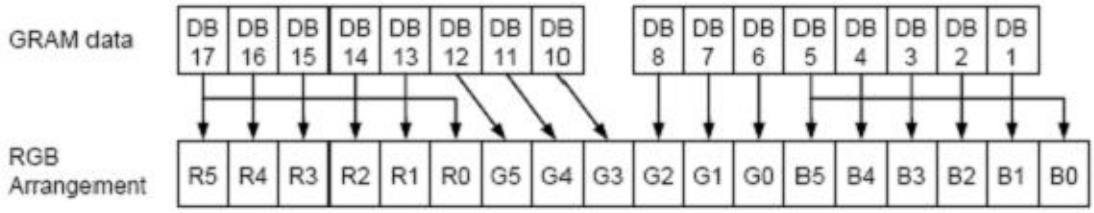


Fig 3.1. 16-bit Interface with LGDP4234

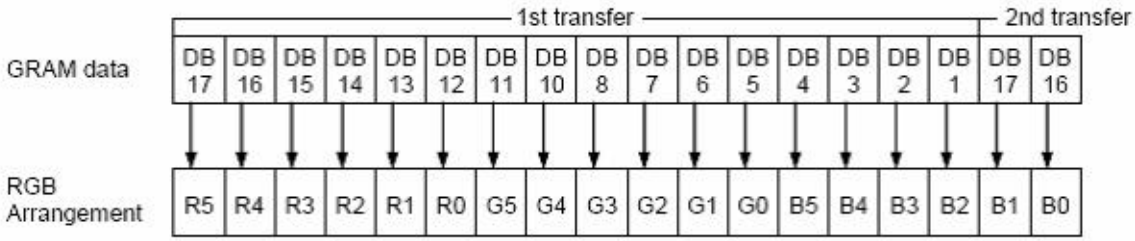
Instruction



RAM data write (1 transfer/pixel, 65k colors) – TRI = "0"

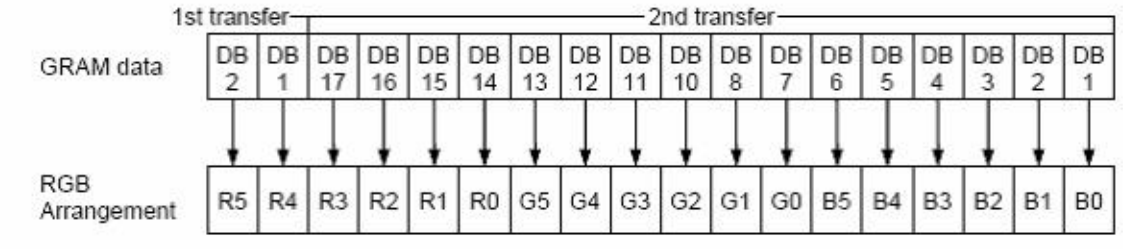


RAM data write (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



(a) 16-bit Interface Mode(continued)

RAM data write (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "1"



3. Electrical Specifications

3-3. Interface Timing

(b) 8-bit Interface Mode

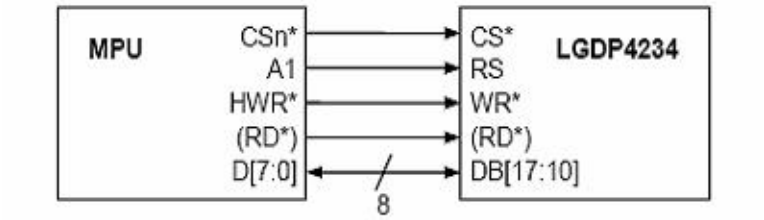
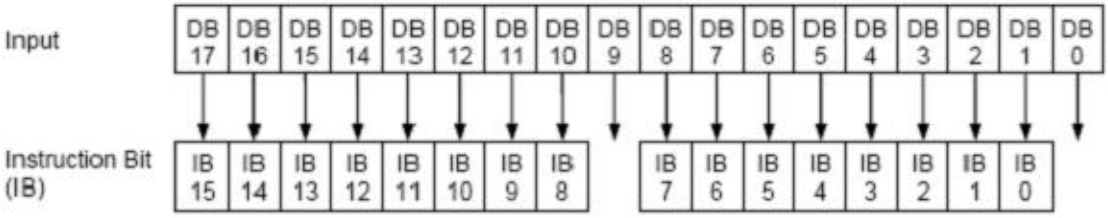
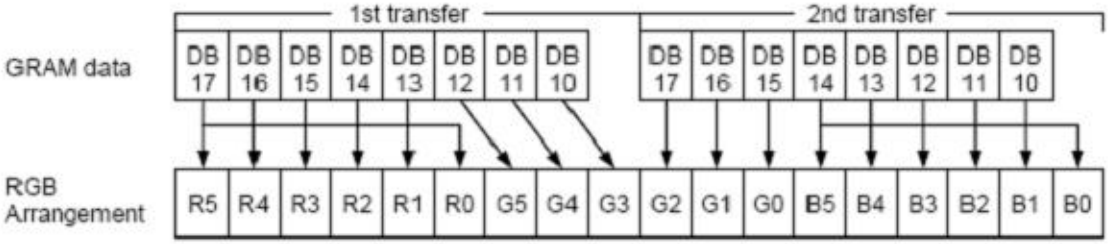


Fig 3.2. 8-bit Interface with LGDP4234

Instruction



RAM data write (2 transfers/pixel, 65k colors) – TRI = "0"

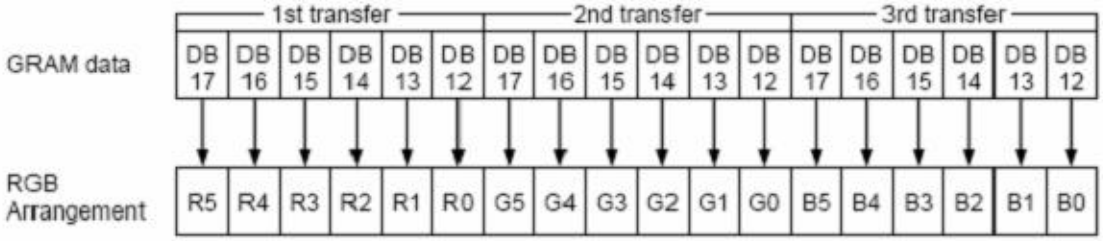


3. Electrical Specifications

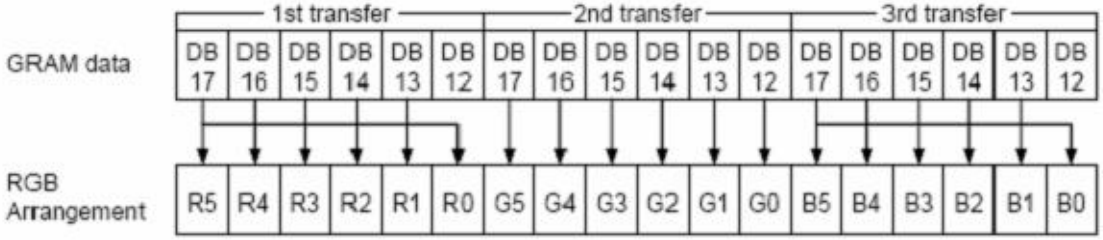
3-3. Interface Timing

(b) 8-bit Interface Mode(continued)

RAM data write (3 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



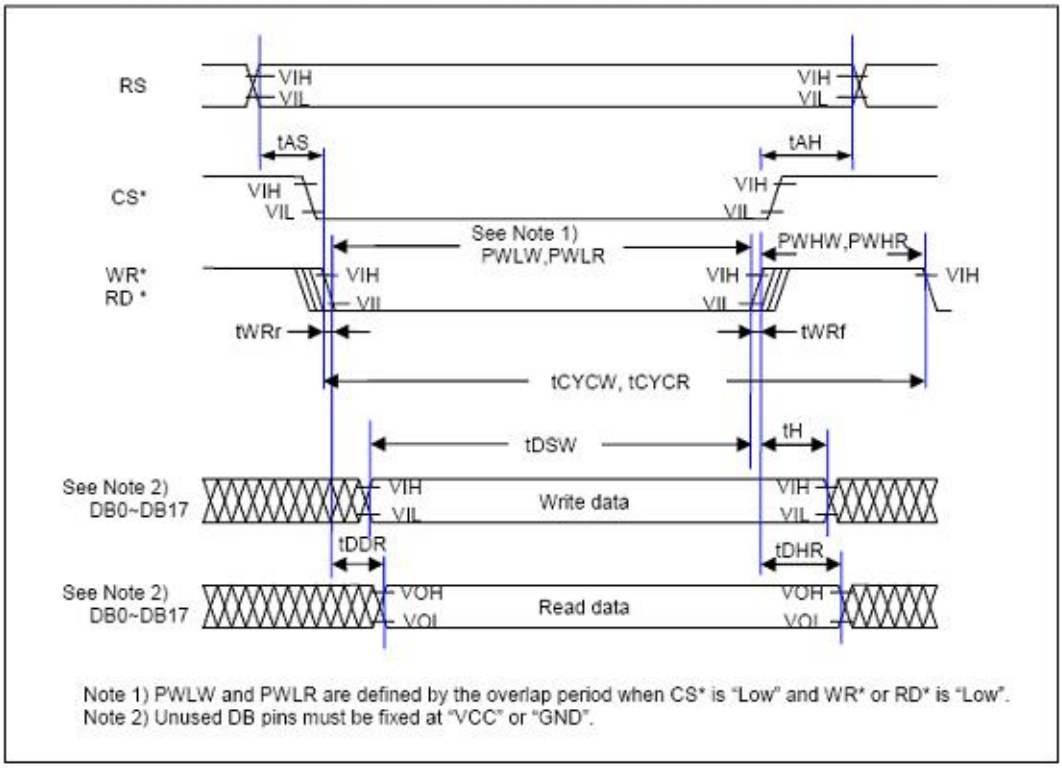
RAM data write (3 transfers/pixel, 65k colors) – TRI = "1", DFM = "1"



3-4. Interface Timing

(a) 80-System 16/8-bit interface

Fig 3.3. AC Timing Parameter and Timing Diagram of 80-system interface



Note 1) PWLW and PWLR are defined by the overlap period when CS* is "Low" and WR* or RD* is "Low".
Note 2) Unused DB pins must be fixed at "VCC" or "GND".

3. Electrical Specifications

3-4. Interface Timing

(b) 80-System 16/8-bit interface

Fig 3.4. AC Timing Characteristics of 80-system interface

Table 34: Write mode, IOVCC=2.6~3.0V, VCC=2.6~3.0V

Item		Symbol	Unit	Timing diagram	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	Figure E1	50		
	Read	t_{CYCR}			100		
Write "Low" level pulse width Read "Low" level pulse width	Write	PW_{LW}	ns	Figure E1	20		
	Read	PW_{LR}			20		
Write "High" level pulse width Read "High" level pulse width	Write	PW_{HW}	ns	Figure E1	20		
	Read	PW_{HR}			20		
Write/Read rise/fall time		t_{WRr}, t_{WRf}	ns	Figure E1	-		5
Setup time	Write(RS~CS*, WR*)	t_{AS}	ns	Figure E1	0		
	READ(RS~CS*, RD*)				0		
Address hold time		t_{AH}	ns	Figure E1	2		
Write data setup time		t_{DSW}	ns	Figure E1	25		
Write data hold time		t_{H}	ns	Figure E1	2		
Read data delay time		t_{DDR}	ns	Figure E1	-		100
Read data hold time		t_{DHR}	ns	Figure E1	5		

3. Electrical Specifications

3-5. Reset Timing

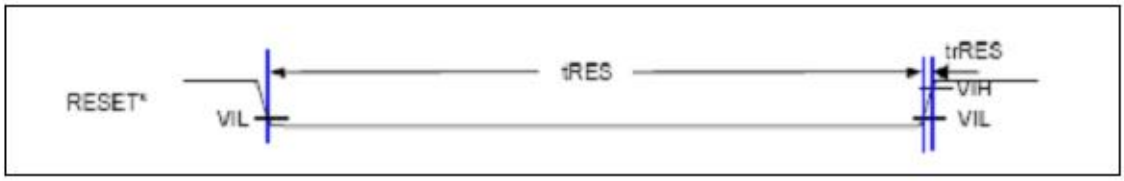


Fig 3.5. Timing Parameter and Timing Diagram of RESET

Item	Symbol	Unit	Timing diagram	Min.	Typ.	Max.
Reset "Low" level width	t_{REG}	ms	Figure E3	1		
Reset rise time	t_{rRES}	us	Figure E3			10

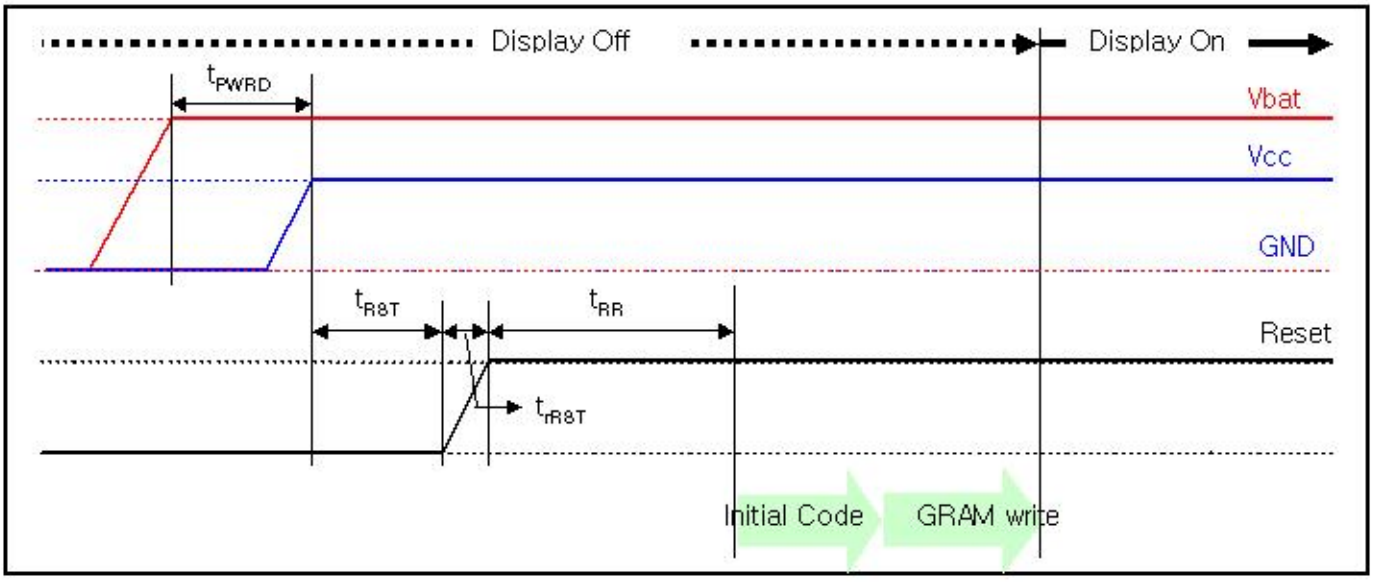
3. Electrical Specifications

3-6. Register setting

(a) Timing characteristic

Item	Symbol	Unit	Min.	Typ.	Max.
Power Supply Delay [Vbat to Vcc]	t_{PWRD}	ms	1	-	-
Reset "Low" Level Width	t_{RST}	ms	1	-	-
Reset Rise Time	t_{rRST}	us	-	-	10
ROM Read Time	t_{RR}	ms	100	-	-

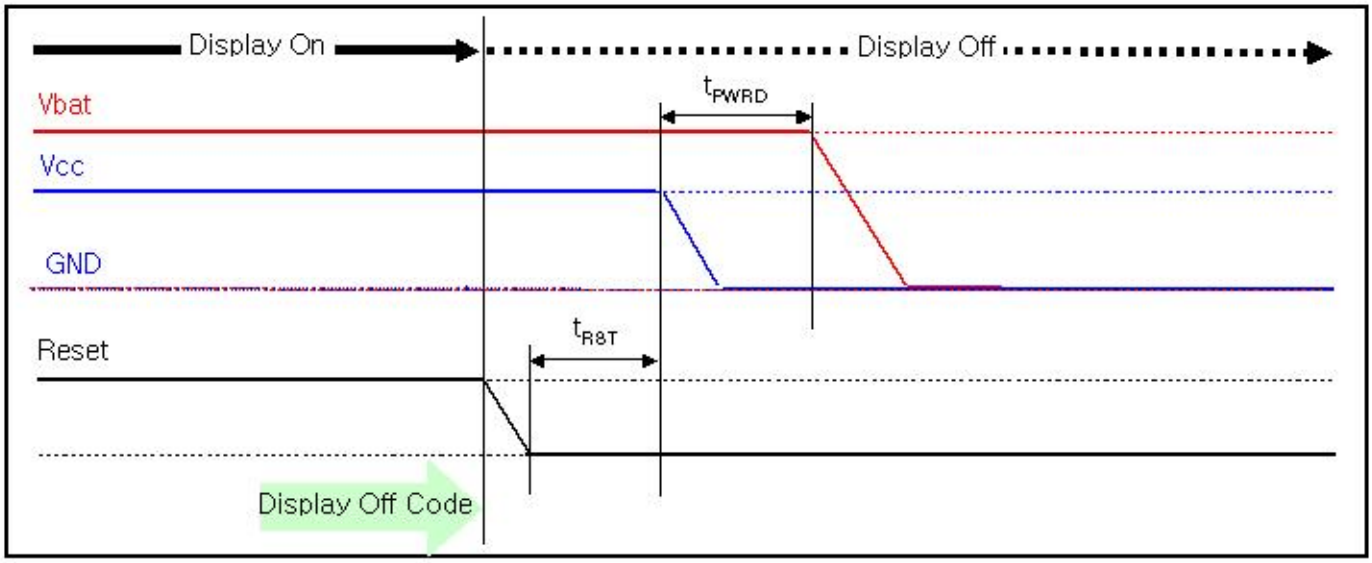
(b) Display On timing Diagram



3. Electrical Specifications

3-6. Register setting

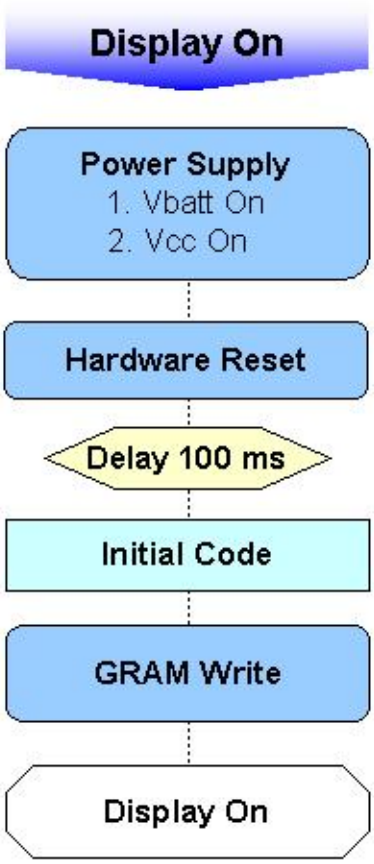
(c) Display Off Timing diagram

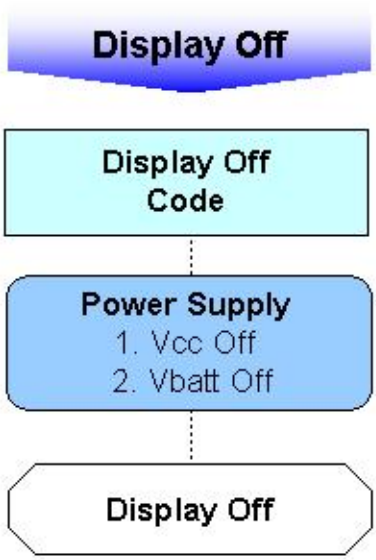


3. Electrical Specifications

3-6. Register setting

(d) Flow Chart





3. Electrical Specifications

3-6. Register setting

(e) Power IC & Driver IC Initial Code

No	Register [Hex]	Data [Hex]	Delay (ms)	Description
1	0X00	0X0001	100	Software Reset
2	0X00	0X0000		Normal Operation
3	0X0C	0X0000		External Display Interface
4	0X10	0X0000		Power Control 1(STDB)
5	0X11	0X1133		Power Control 2(VDD)
6	0X12	0X0123	20	Power Control 3(PBEN & VGN En)
7	0X13	0X0104		Power Control 4(L/S En)
8	0XB4	0X5F00		MSR(Current Setting)
9	0XB5	0X5F00		MSG(Current Setting)
10	0XB6	0X5F00		MSB(Current Setting)
11	0XB7	0X000E		MSR_Duty
12	0XB8	0X000E		MSG_Duty
13	0XB9	0X000E		MSB_Duty
14	0XBA	0X0003		MSX Start Control
15	0XBB	0X0A0C		MSX_Rise/Fall time
16	0X07	0X0030		Display Off
17	0X13	0X0114		Power Control4(DAC En)
18	0X12	0X0133		Power Control 3(PTEN)
19	0X01	0X0000		
20	0X03	0X0030		Entry
21	0X08	0X0000		Display Control 2(Gamma Control)
22	0X07	0X0031		Display On

-Current Set (TBD)

(f) Display Off Code

No	Register [Hex]	Data [Hex]	Delay (ms)	Description
1	0X07	0X0031		Display Off
2	0X13	0X0104		Power Control (DAC Disable)
3	0X12	0X0100		Power Control (VGN Disable)

3. Electrical Specifications

3-7. Power Save Mode

	DSTB	SLP	STB
VDD Regulator	Disabled	Enabled	Enabled
SRAM Data	Flushed	Retained	Retained
Resonator	Disabled	Enabled	Disabled
Internal Clock	Halt	Halt	Halt
Register Setting	Flushed	Retained	Retained
Method to Exit	4 times of asserting CSN or H/W reset	Setting SLP=0	Setting STB =0
Comparison of Power Consumption	Lowest	Low	Lower

4. Optical Characteristics

Table 4.1 Electro-Optical Characteristics

Item			Condition	Min	Typ	Max	Unit
Initial Brightness	Full White **(1)**		Darkroom	**200**	**230**	-	cd/m²
Contrast Ratio	White/Black **(2)**		Darkroom	**20,000**	-	-	
Color Coordinate & Luminance Efficiency	White	x	Darkroom	**0.27**	**0.31**	**0.35**	
		y		**0.29**	**0.33**	**0.37**	
	Red	x	Darkroom	**0.645**	**0.675**	**0.705**	
		y		**0.290**	**0.320**	**0.350**	
	Green	x	Darkroom	**0.225**	**0.255**	**0.285**	
		Y		**0.645**	**0.675**	**0.705**	
	Blue	X	Darkroom	**0.110**	**0.140**	**0.170**	
		y		**0.080**	**0.110**	**0.140**	
Color Gamut			R/G/B	**80**	**85**	-	%
Brightness Uniformity **(3)**			Full White	**80**	-	-	%
Gamma			-	-	**2.2**	-	
CCT				**5500**	**6700**	**8000**	K
Life time (30% Pixel On) $T_{0.5}$			Full White	**20,000**	-	-	hrs
View angle			-	-	**179**	-	degree

(1) Luminance : VCC=2.8[V], I/O VCC=2.8[V], VBATT=3.7[V], Ta=25[℃] (refer to the Note.1)
(2) 100% gray vs. 0% gray
(3) Uniformity = Min/Max (%) of luminance values measured at
9 points with 5mm diameter aperture.
(refer to the Note.3)
(4) Room temperature : 25℃

4. Optical Characteristics

[Note 1] Optical Test Equipment Setup

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the AMOLED surface.

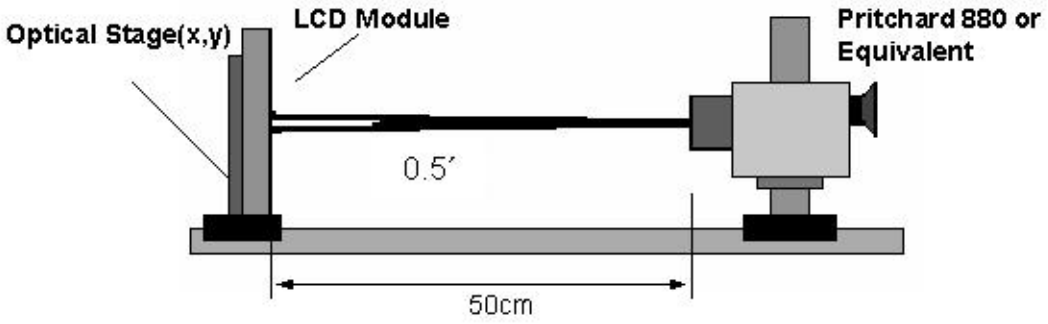


Fig 4.1. Optical Characteristic Measurement Equipment and Method

[Note 2]

Contrast ratio is defined as follows ;

$$\text{Contrast Ratio(CR)} = \frac{\text{Photo detector output with AMOLED being "white"}}{\text{Photo detector output with AMOLED being "black"}}$$

4. Optical Characteristics

[Note 3]

Viewing angle range is defined as follows;

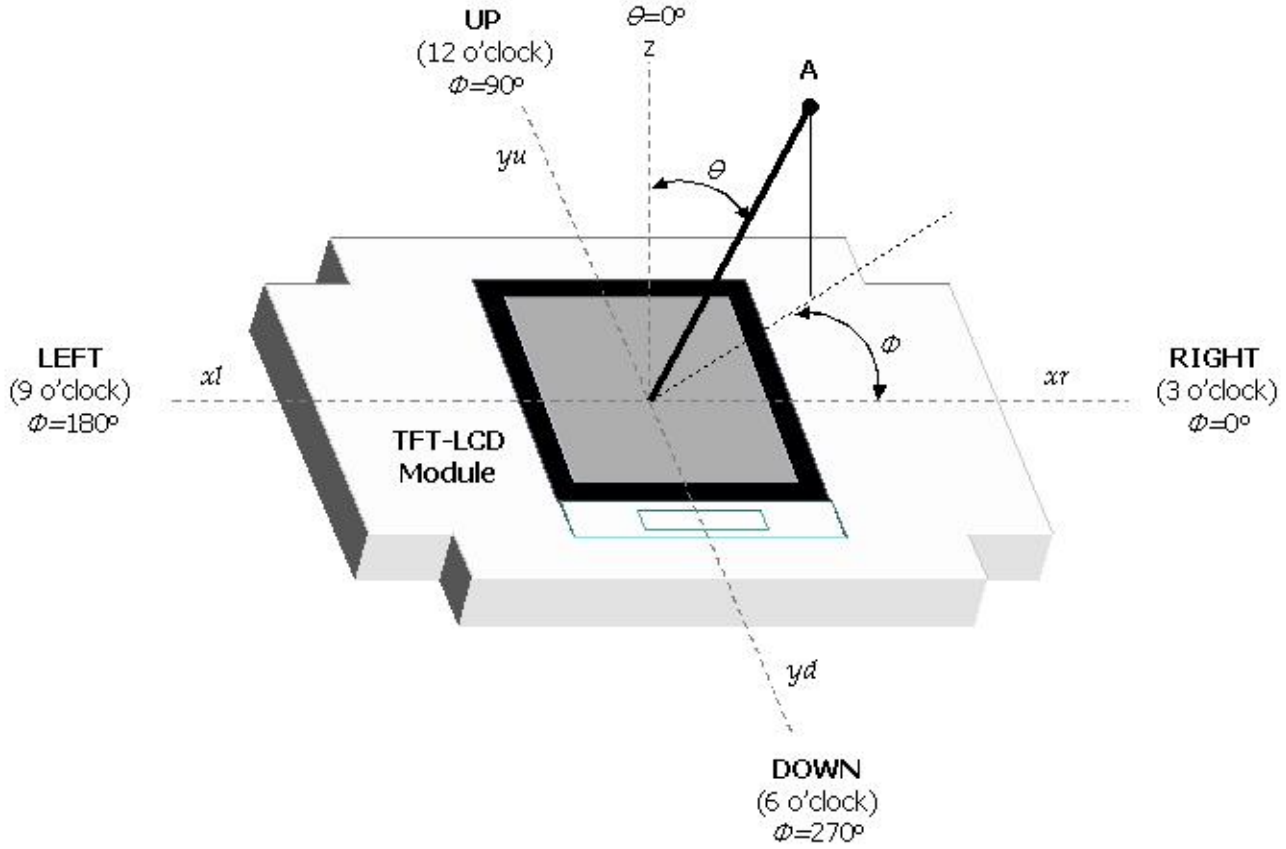


Fig 4.2. Viewing Angle

4. Optical Characteristics

[Note 4]

The brightness measurement is taken at point B5.

$$\text{Brightness Uniformity} = \frac{\text{Minimum Photo detector output for B1-B9 with all pixels white}}{\text{Maximum Photo detector output for B1-B9 with all pixels white}} \times 100(\%)$$

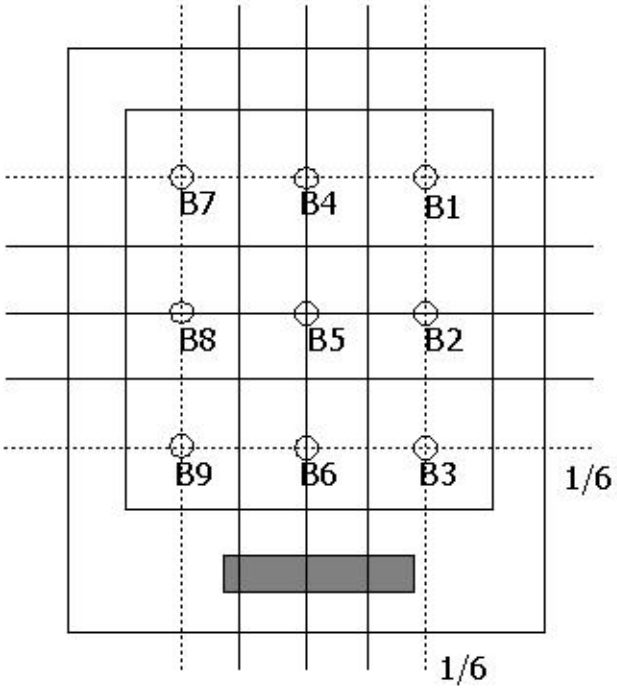
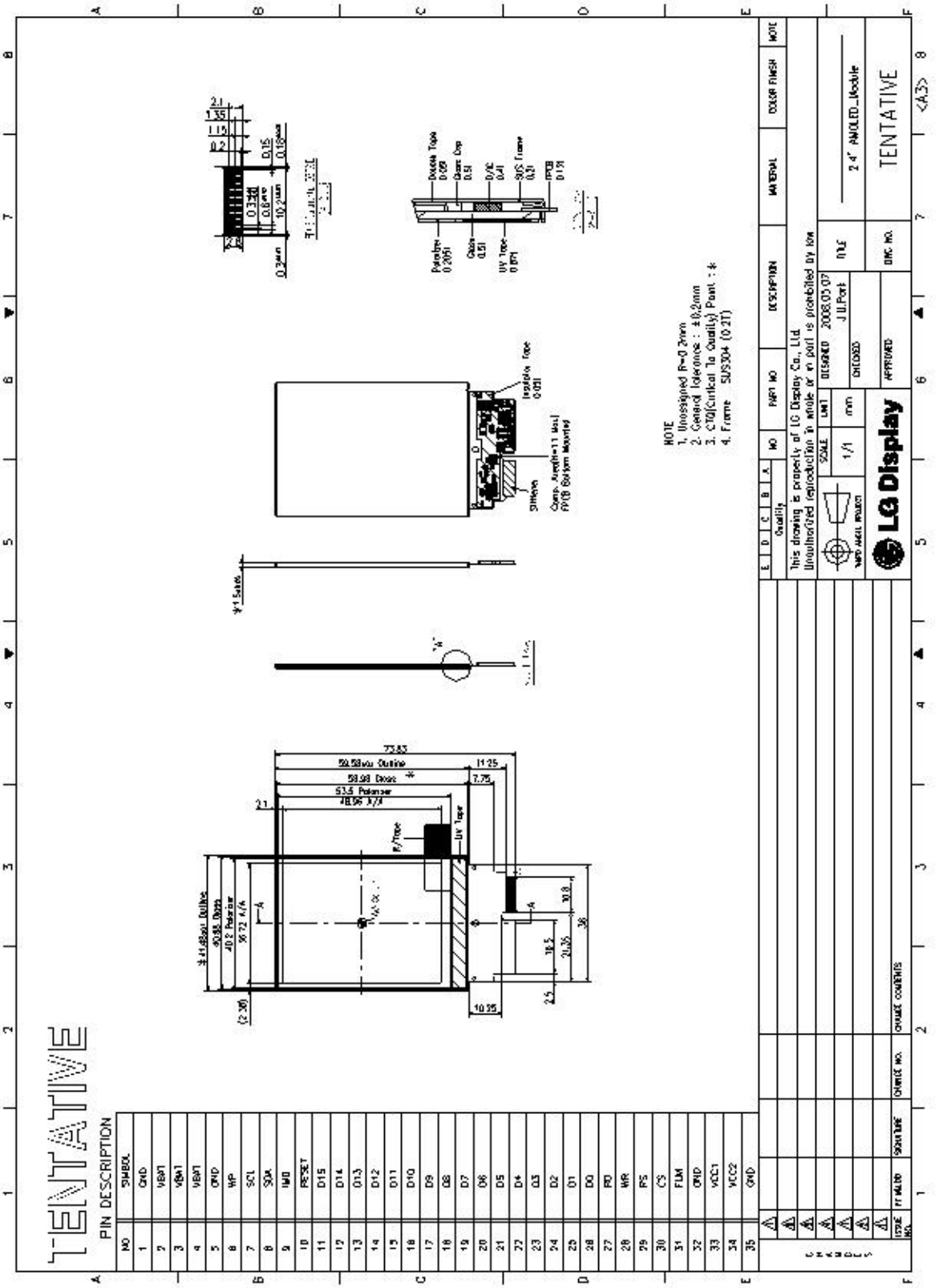


Fig 4.4. Brightness measurement points

5. Mechanical Characteristics

[Outline Dimension]



6. Reliability Test

6-1. Reliability Condition

Item10		Condition	Remark
1	High Temperature & Humidity Operating	60℃/ 90%,240Hrs	
2	High Temperature Operating	70℃,240Hrs	
3	Low Temperature Operating	-30℃,240Hrs	
4	Temperature & Humidity Cycle	-20℃ ~ +50℃/95% 65Hrs	
5	High Temperature Storage	80℃,240Hrs	
6	Low Temperature Storage	-40℃,240Hrs	
7	Thermal Shock Storage	-30~80℃ 30Min_100Cycle	

Item		Condition	Remark
1	PCT	1.4atmospheric[air] pressure (110℃,100%)_ 1Cycle(6Hrs)	
2	ESD	Contact : ±8kV, 5Pts (Window) Air : ±15kV, 5Pts (Window), 330Ω/150PF ● Contact : ±0.2kV, FPC Input, 330Ω/150PF	
3	3 Point Bending	Pressure Jig : diameter 3.0 mm Jig Pressure speed :3mm/Min	
4	COG	Pressure Jig :diameter 5.0 mm Jig Pressure speed :3mm/Min	
5	Drop	Packing Drop -.1 Corner, 3 Edges, 6 Faces, Total 10times drop -.Flat surface: over 1Cm thickness steel plate	
6	Vibration	Box Package condition -.vibration frequency : 3 ~ 300 Hz -.LEVEL : 1.5 Grms -.vibration direction : X / Y / Z -.vibration time : 60 min individually.	

Note 1) The reliability test is guaranteed according to the driving condition of the spec

Note 2) Driving Pattern : White➔Red➔Green➔Blue➔Black(each time : 30 minute)

Note 3) All test result of items should be judged in 2 hours recovery time at Room temperature.

Note 4) The reliability test is guaranteed according to the driving condition of the spec

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. Packing

7-1. Designation of Lot Mark

(1) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

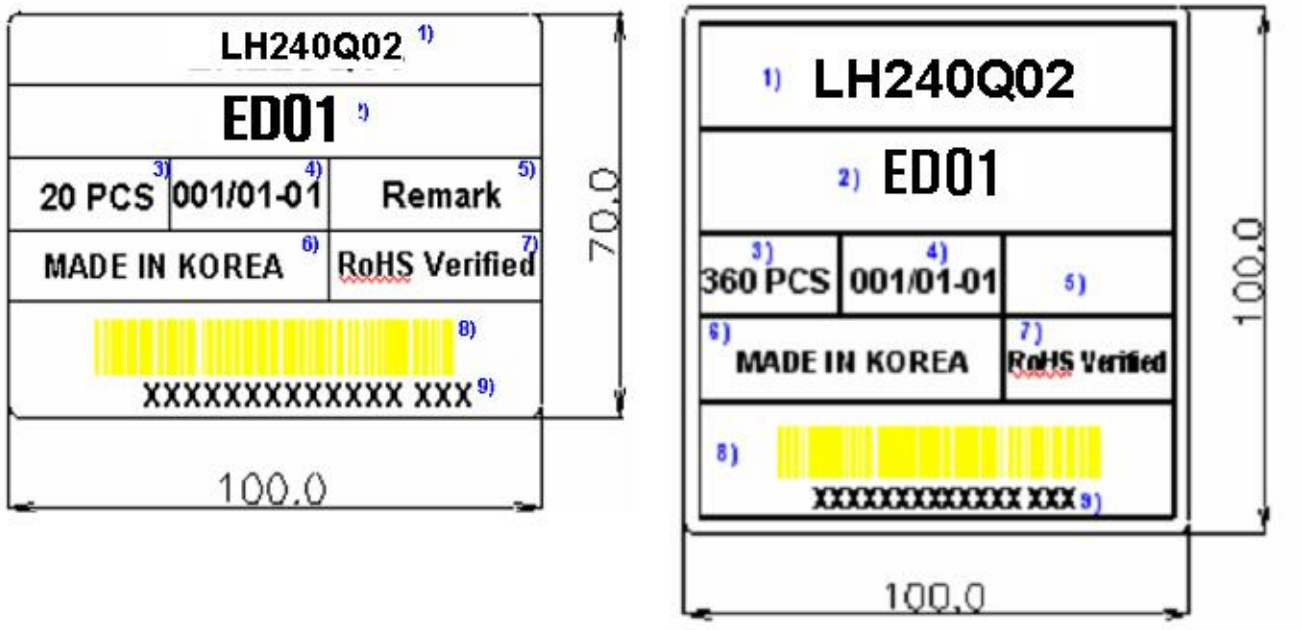
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

(2) Location of Lot Mark

Serial NO. is printed on the surface of LCM
This is subject to change without prior notice.

7. Packing

7-2. Packing Label design



Inner BOX Label

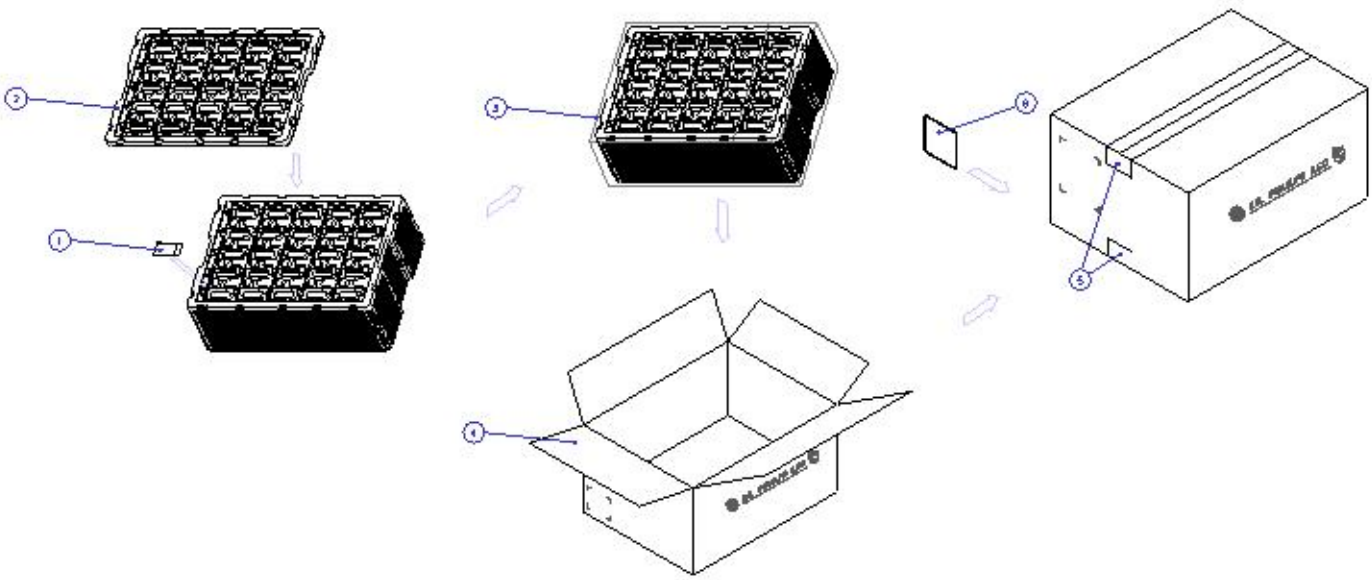
Master BOX Label

1) Base model name
2) Suffix1
3) Product Volume : declaring the volume of product in the BOX/PALLET
4) Lot/MM-DD
   - Lot No : declaring the BOX/PALLET No. in the number according to Production plan in sequence.
   - MM-DD :declaring packing Month/day
5) REMARK
   - Register the Production change facts
6) Origin declaration : (Only Module business)
   - LGD KUMI : MADE IN KOREA
7) Declaration RoHS Verified expression
8) Barcode Type : Code 128A Type
9) Suffix2

7. Packing

7-3. Packing Form

(1) Package quantity in one box : 500 pcs
(2) Box Size : 475mm × 348mm × 210mm
(3) 1Box = tray 20 + 1 tray(dummy , top) = 21 tray



NO.	Description	Material
1	Module	-
2	Packing, Tray	PET(0.8t)
3	Bag	PE, 560mm x 830mm
4	Box	SWR4, 475mm x 348mm x210mm
5	Tape	OPP, 70mm x 300m
6	Label	Art Paper, 100mm x 100mm

8. PRECAUTIONS

Please pay attention to the following when you use this module.

8-1. ASSEMBLING PRECAUTIONS

(1) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(2) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics deteriorate the polarizer.)
(3) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(4) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(5) Do not open the case because inside circuits do not have sufficient strength.
(6) The metal case of a module should be contacted to electrical ground of your system.

8-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

8. PRECAUTIONS

8-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

8-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

8-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.
(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5˚C and 35˚C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

8-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

9. Inspection Standard

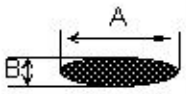
9-1. Inspection Standard for Main OLED

<table>
<tr><th>No</th><th>Item</th><th>Criterion for Defects</th><th>Remark</th></tr>
<tr><td>1</td><td>Non Lighting</td><td>Nothing</td><td>Major</td></tr>
<tr><td>2</td><td>Irregular Operation</td><td>Nothing</td><td>Major</td></tr>
<tr><td>3</td><td>Short</td><td>Nothing</td><td>Major</td></tr>
<tr><td>4</td><td>Open</td><td>Nothing</td><td>Major</td></tr>
<tr><td>5</td><td>Dot Defect</td><td>
<table>
<tr><th>Item</th><th>Bright Dot</th><th>Dark Dot</th></tr>
<tr><td>Acceptable No.</td><td>0</td><td>(Note 1)</td></tr>
</table>
Note1) Case of Dot defect is below
① Bright Dot (whit spot) : "0"
② Dark Dot (black spot) : "0" (In case of Dark Dot on Main TFT LCD)
- NG if there's full Dot defect.
- Damaged less than half size of sub-pixel is not counted as defect
- Dots darker than half size of sub-pixel are not defined as bright dot defect
</td><td>Minor</td></tr>
<tr><td>6</td><td>Blemish & Foreign matters Black/White Spot

Size :
Φ=(A+B)/2</td><td>
<table>
<tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr>
<tr><td>Φ ≤ 0.10
0.10 < Φ ≤ 0.20
0.20 < Φ</td><td>Ignore
1
0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>7</td><td>Black/White Line</td><td>
<table>
<tr><th>Length (mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr>
<tr><td>Linear
L≤1.0</td><td>W ≤0.02
0.02 < W ≤0.03</td><td>Ignore
1</td></tr>
</table>
<table>
<tr><th>Length (mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr>
<tr><td>Linear
L≤2.0</td><td>W ≤0.03
0.03 < W ≤0.05</td><td>Ignore (Note 2)
1</td></tr>
</table>
</td><td>Minor</td></tr>
</table>

9. Inspection Standard

9-1. Inspection Standard for Main OLED

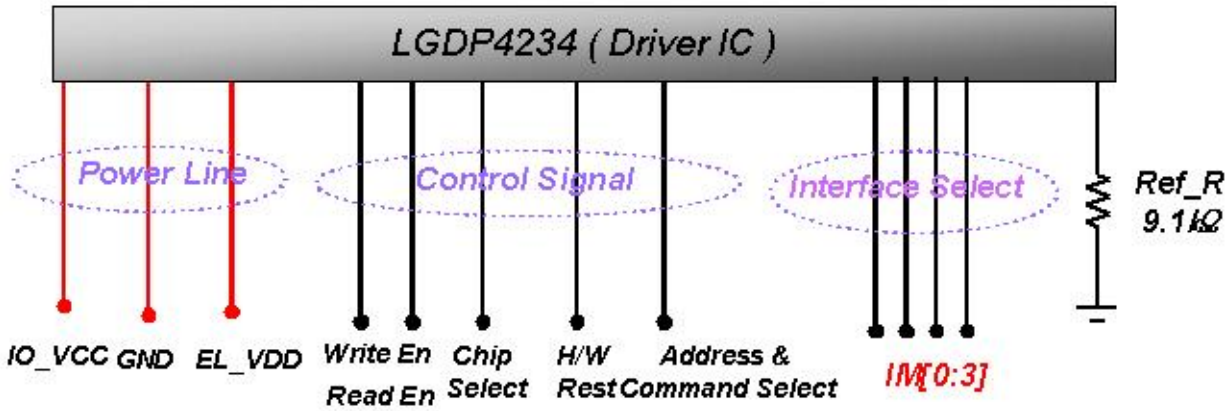
<table>
<tr><th>No</th><th>Item</th><th>Criterion for Defects</th><th>Remark</th></tr>
<tr><td>8</td><td>Scratch on Polarizer
  </td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W ≤ 0.03
0.03 < W ≤ 0.05
0.05 < W</td><td>Ignore
L ≤ 2.0
L>2.0</td><td>Ignore
1
0</td></tr></table></td><td>Minor</td></tr>
<tr><td>9</td><td>Bubble in Polarizer</td><td><table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>Φ ≤ 0.20
0.20 < Φ ≤ 0.50
0.50 < Φ ≤ 0.80
0.80 < Φ</td><td>Ignore
3
2
0</td></tr></table></td><td>Minor</td></tr>
<tr><td>10</td><td>Stains on Panel Surface</td><td>Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td></tr>
<tr><td>11</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td></tr>
<tr><td>12</td><td>Defect of land surface Contact</td><td>Evident crevices which is visible are rejectable.</td><td>Minor</td></tr>
<tr><td>13</td><td>Parts Mounting</td><td>① Failure to mount parts
② Parts not in the specifications are mounted
③ Polarity, for example, is reversed</td><td>Major
Major
Major</td></tr>
<tr><td>14</td><td>Parts Alignment</td><td>① LSI, IC Lead width is more than 50% beyond pad outline.
② Chip component is off center and more tan 50% of the leads is off the pad outline.</td><td>Minor
Minor</td></tr>
<tr><td>15</td><td>Conductive Foreign matter</td><td>① On open space(GND, manual solder) solder ball is allowed up to Φ0.1mm(1EA).
② In case of shield space is allowed up to Φ0.2mm(1EA)</td><td>Major</td></tr>
<tr><td>16</td><td>Faculty PWB correction</td><td>① Due to PWB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair ; 2 or more places are corrected per PWB
② Short circuited part is cut, and no resist coating has been performed.</td><td>Minor
Minor</td></tr>
</table>

Appendix. External Interface

The interface is selected by hardware pins setting the IM[0:3] as follows. The RGB interface is used to access RAM.

Name	# pins	I/O	Connected to	Function
IM[3:0]/ID	4	I	GND/IOVCC	MPU interface mode select signal. In SPI mode, the IM[0] pin is used to set the ID of device code.

IM[3:0]	Interface mode	Data pins
0000	68-system 16 bit interface	DB[17:10], DB[8:1]
0001	68-system 8 bit interface	DB[17:10],
0010	80-system 16 bit interface	DB[17:10], DB[8:1]
0011	80-system 8 bit interface	DB[17:10]
010*	Serial peripheral interface (SPI)	SDI, SDO
1000	68-system 18 bit interface	DB[17:0]
1001	68-system 9 bit interface	DB[17:9]
1010	80-system 18 bit interface	DB[17:0]
1011	80-system 9 bit interface	DB[17:9]
11**	Setting disabled	-

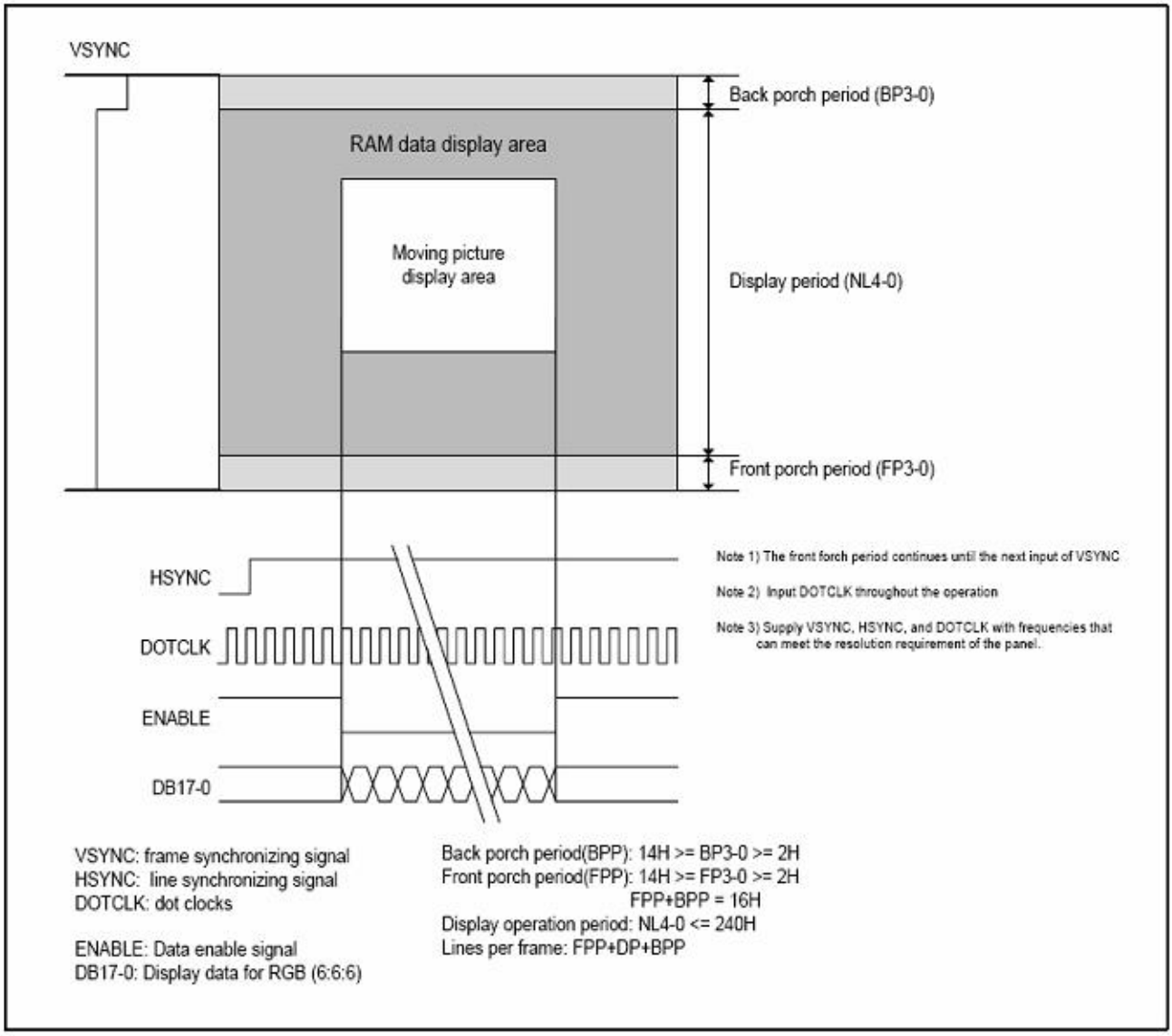


And also the interface is selected by setting the RIM1-0 bits as follows. The RGB interface is used to access RAM.

RIM[1:0]	RGB interface	DB pins
00	18-bit RGB interface	DB[17:0]
01	16-bit RGB interface	DB[17:10], DB[8:1]
10	6-bit RGB interface	DB[17:12]
11	Setting disabled	

1-1. RGB Interface

The display operation via the RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface enables transferring minimum necessary data and rewriting the RAM area need to be overwritten with use of window address function and high-speed write mode. In RGB interface mode, it is necessary to set back and front porch periods before and after a display period, respectively.



ENABLE signal

The combinations of EPL and ENABLE bits and the functions are as follows. Note that it is necessary to set both EPL and ENABLE bits to automatically update RAM address in the AC when writing data to the internal RAM. The EPL bit inverts the polarity of ENABLE signal.

EPL	ENABLE	RAM write	RAM address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

Moving picture display

The LGDP4234 has the RGB interface for moving picture display and incorporates RAM for storing moving picture data, which has following merits in displaying a moving picture.

• The window address function enables transferring minimum necessary data to be written on the moving picture RAM area.

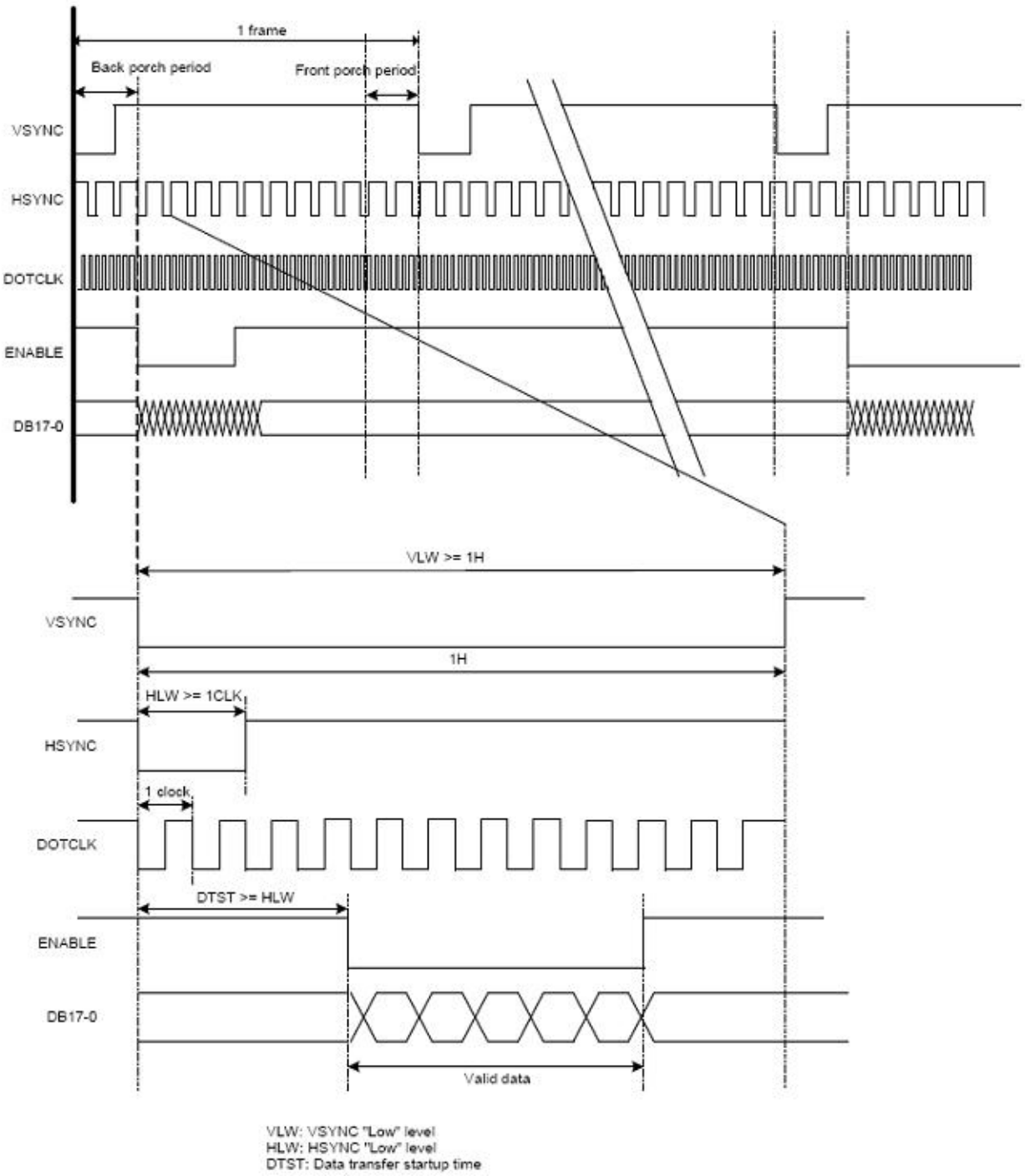
• Data are transferred only to the moving picture RAM area.

• The reduction in data transfer contributes to the reduction in power consumption by the entire system.

• Allowing the use of system interface to rewrite data, such as icons, in still picture RAM area while displaying a moving picture.

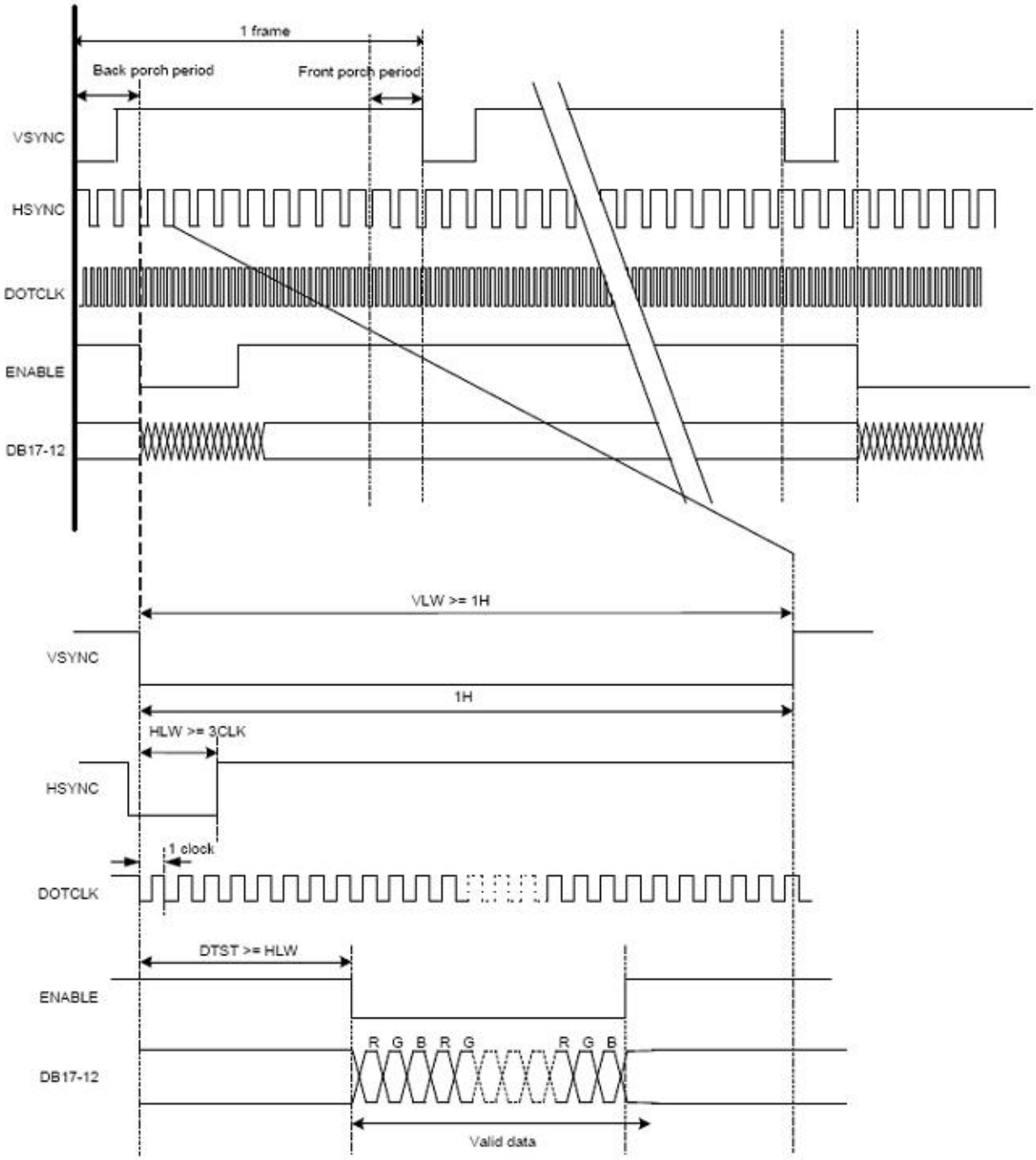
RGB interface timing

The timing chart of signals in 16/18-bit RGB interface mode is as follows.



Note: Use the high-speed write mode (either HWM or LHWM = "1") when writing display data to the internal RAM in RGB interface mode

The timing chart of signals in 6-bit RGB interface mode is as follows.



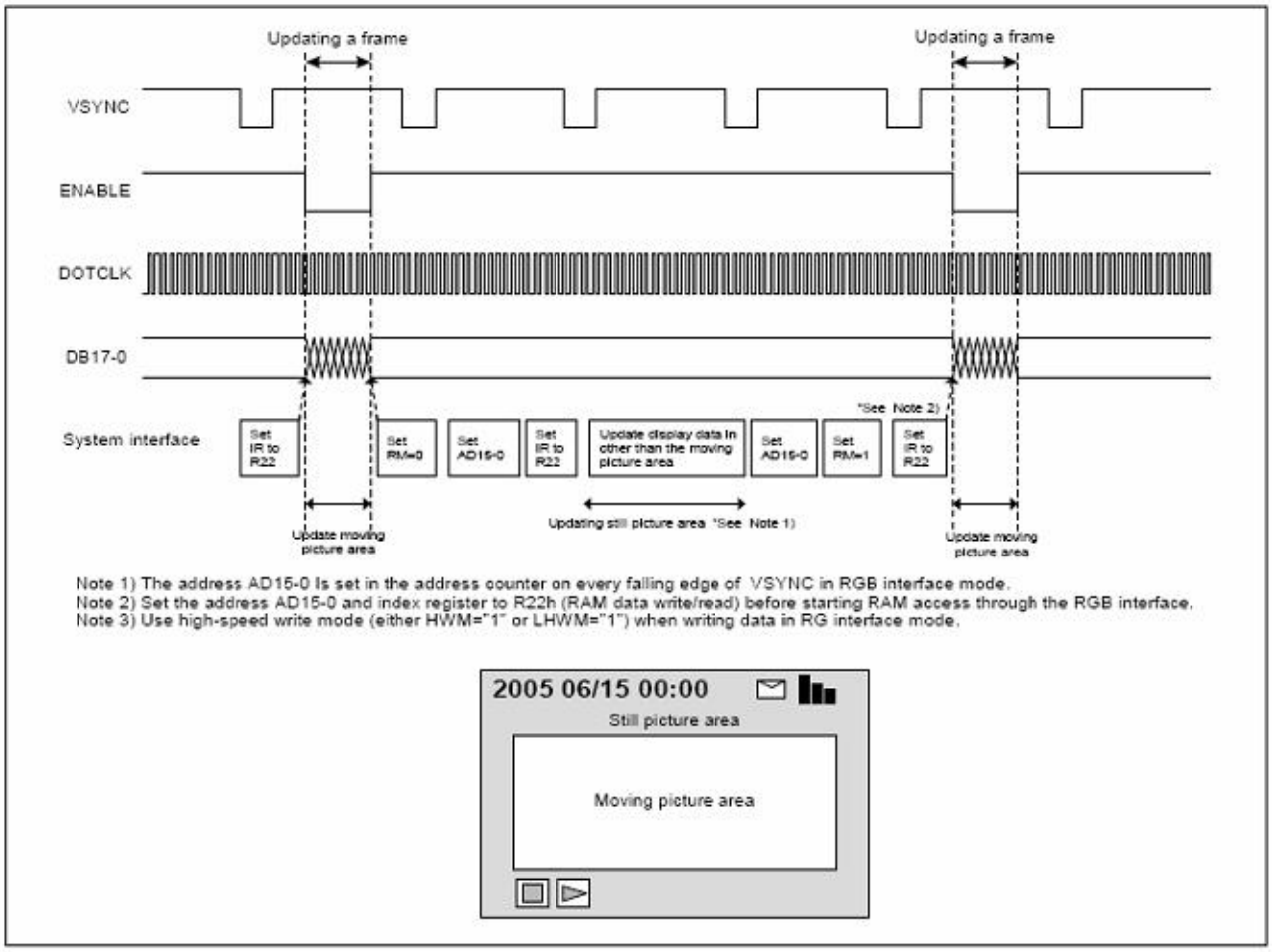
VLW: VSYNC "Low" level
HLW: HSYNC "Low" level
DTST: Data transfer startup time

Note 1) Use the high-speed write mode (either HWM or LHWM = "1") when writing display data to the internal RAM in RGB interface mode
Note 2) In 6-bit RGB interface mode, RGB dots are transferred each in synchronization with one DOTCLK input.
For this reason, set the cycle of each signal (HSYNC, VSYNC, ENABLE) to contain DOTCLK inputs of a multiple of 3.

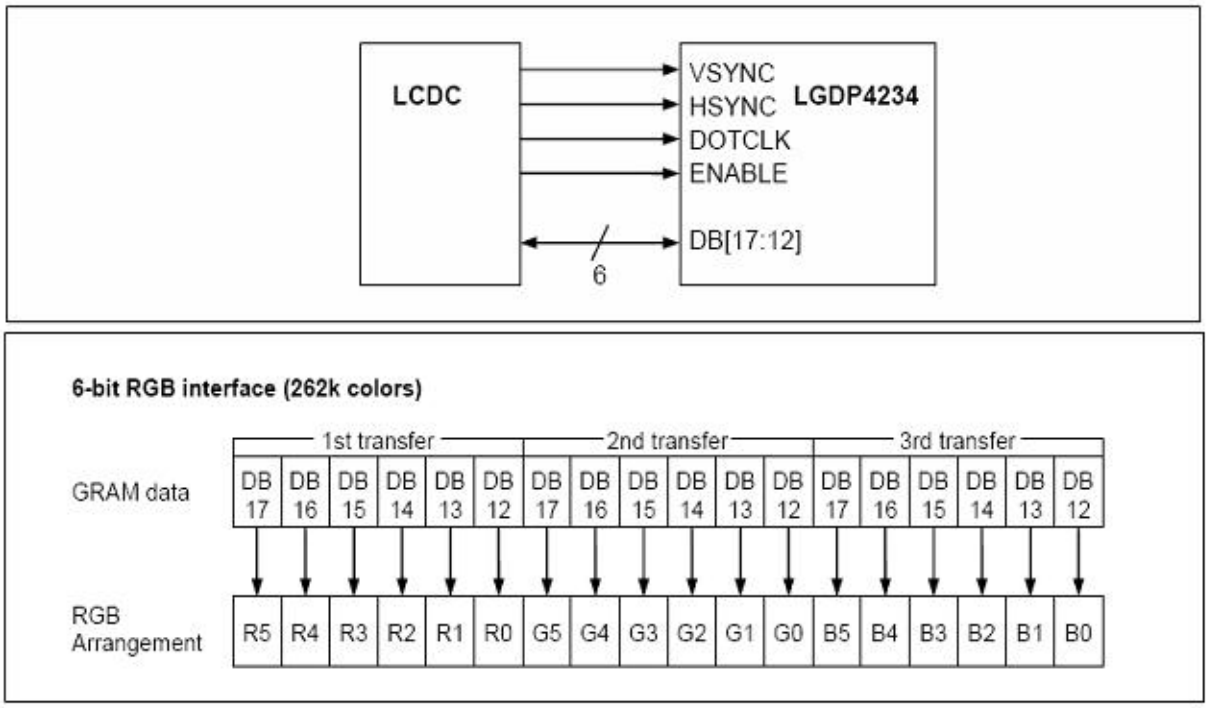
RAM access via a system interface in RGB-I/F mode

The LGDP4234 allows RAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the internal RAM via the system interface, set ENABLE high" to stop writing data via the RGB interface. Then set RM = "0" to make RAM accessible via the system interface. When restarting RAM access in RGB interface mode, wait a time for one read/write bus cycle. Then, set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal RAM.

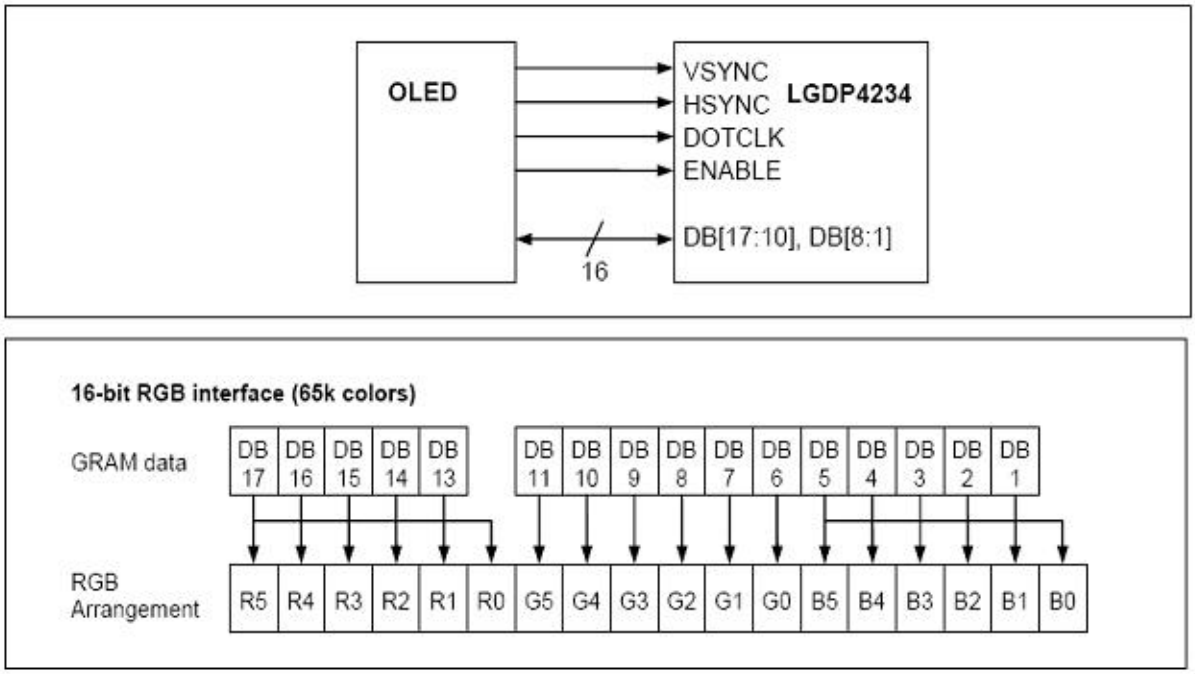
The following figure illustrates the operation of the LGDP4251 when displaying a moving picture via the RGB interface and rewriting data in the still picture RAM area via the system interface.



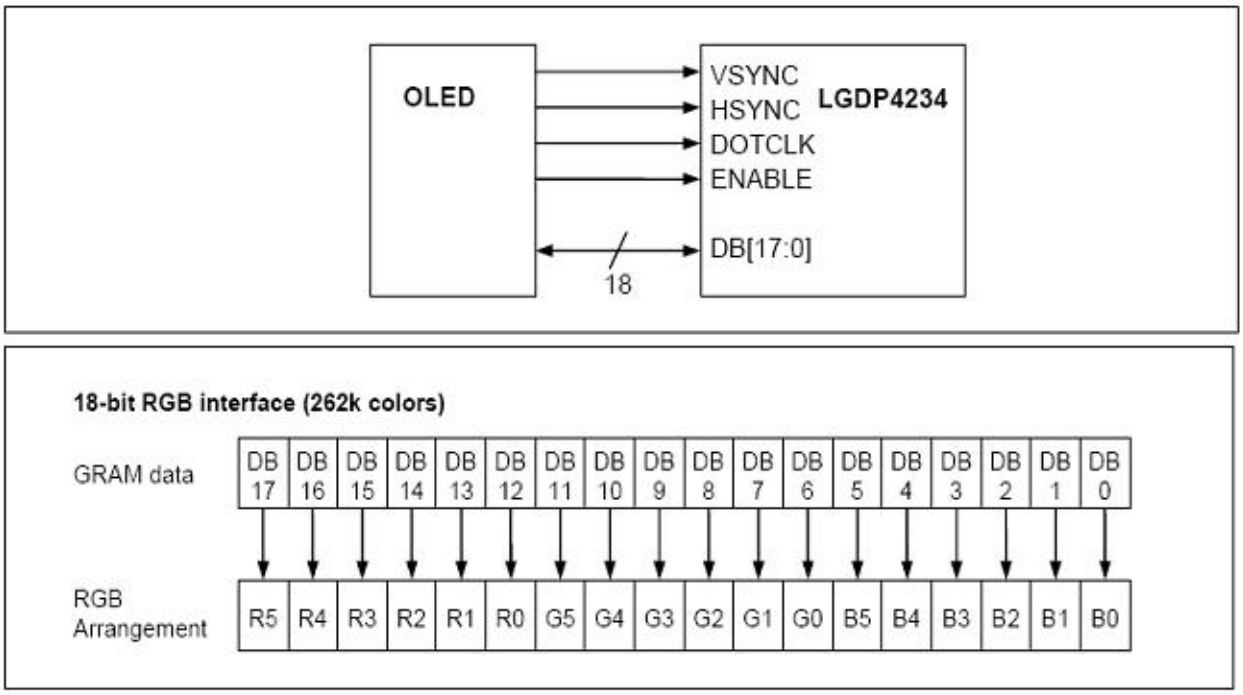
6-bit RGB interface



16-bit RGB interface



18-bit RGB interface



The RGB interface is selected by setting the RIM1-0 bits. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE).

1-2. SPI Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:1] pins to the GND/IOVCC/GND levels respectively. The SPI is available via the chip select line (CS*), the serial transfer clock line (SCL), the serial data input (SDI), and the serial data output (SDO). In SPI mode, the IM0/ID pin functions as the ID pin and the DB[17:0] pins, which are not used, must be fixed at either IOVCC or GND level.

Name	# pins	I/O	Connected to	Function
IM[3:0]/ID	4	I	GND/IOVCC	MPU interface mode select signal. In SPI mode, the IM[0] pin is used to set the ID of device code.

IM[3:0]	Interface mode	Data pins
0000	68-system 16 bit interface	DB[17:10], DB[8:1]
0001	68-system 8 bit interface	DB[17:10],
0010	80-system 16 bit interface	DB[17:10], DB[8:1]
0011	80-system 8 bit interface	DB[17:10]
010*	Serial peripheral interface (SPI)	SDI, SDO
1000	68-system 18 bit interface	DB[17:0]
1001	68-system 9 bit interface	DB[17:9]
1010	80-system 18 bit interface	DB[17:0]
1011	80-system 9 bit interface	DB[17:9]
11**	Setting disabled	-

Transferred bits	1	2	3	4	5	6	7	8
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

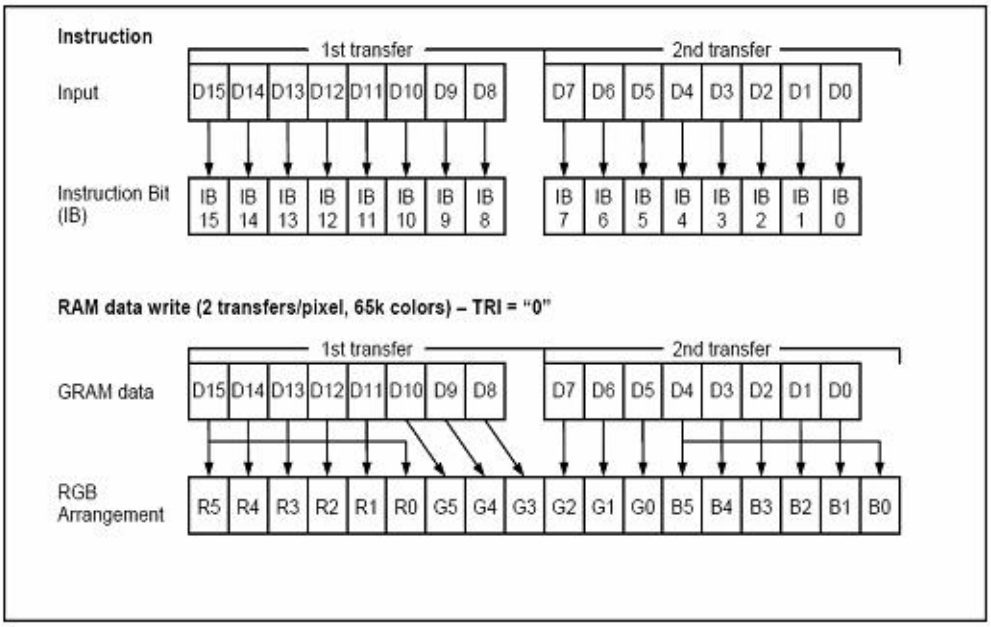
Note: ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

The LGDP4234 recognizes the start of data transfer on the falling edge of CS* input and transfers the start byte. It recognizes the end of data transfer on the rising edge of CS* input. The LGDP4251 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LGDP4234 correspond as a result of comparison. When selected, the LGDP4234 starts taking subsequent data. The ID pin sets the least significant bit of the identification code. Send "01110" to the identification code, which is the five upper bits of the start byte. Two different chip addresses must be assigned to the LGDP4234 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = "0", either index register write operation or status read operation is executed. When RS = "1", either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). Data are received when the R/W bit is "0", and are transferred when the R/W bit is "1".

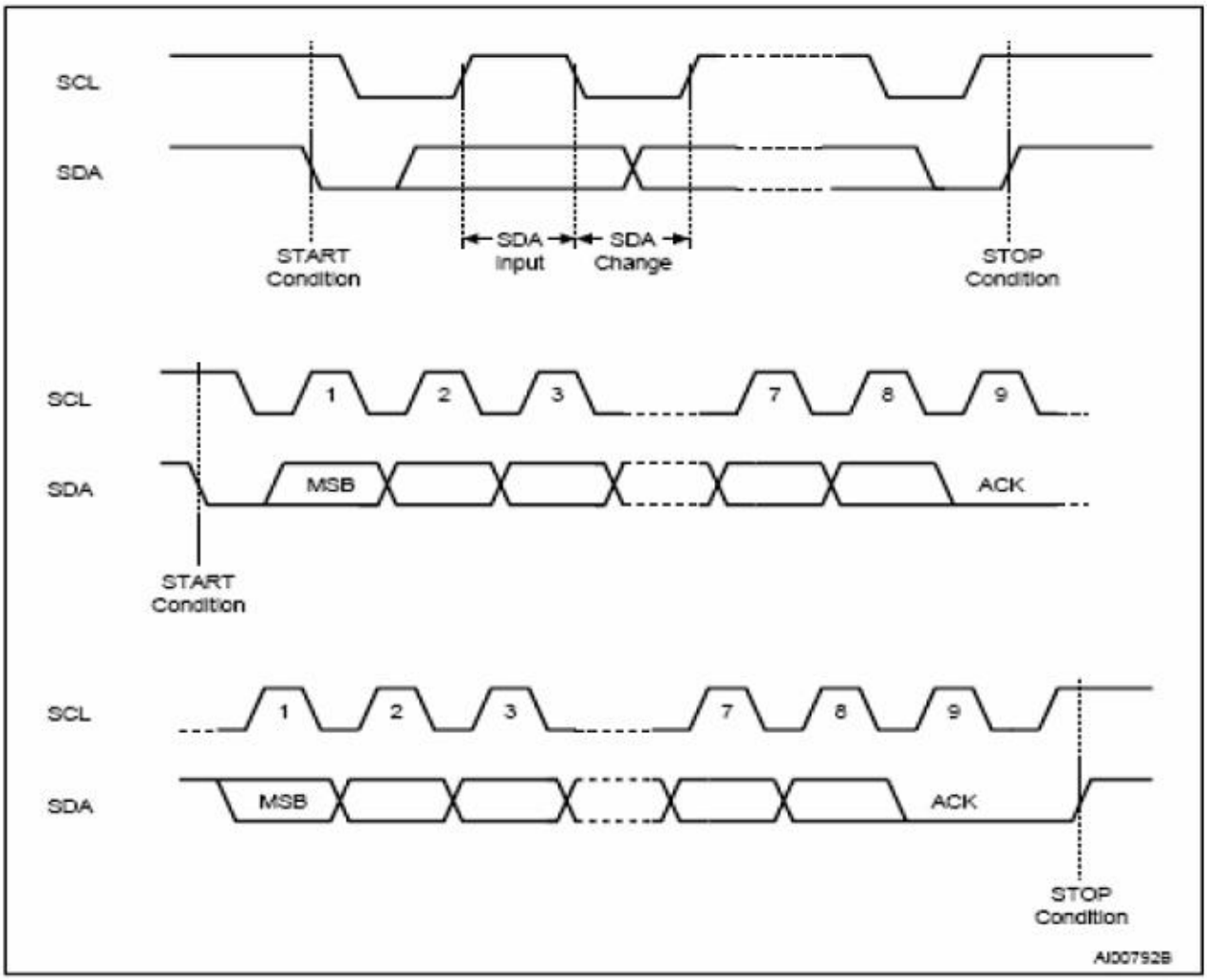
After receiving the start byte, the LGDP4234 starts transferring or receiving data in units of bytes. Data transfer is executed from the MSB. All instructions of the LGDP4234 take a 16-bit format and are executed internally after transferring two bytes (DB[15:0]) from the MSB. GRAM write data are internally expanded into 18 bits. After receiving the start byte, the LGDP4234 takes the first and the second byte as the upper and the lower eight bits of a 16-bit instruction, respectively.

In SPI mode, invalid data are sent to the data bus until 5-byte data are read out from the internal GRAM after the start byte. Valid data are read out as the LGDP4234 reads out the 6th byte data from the internal GRAM.



1-3. I2C Interface

The IIC Interface is used for both reading configuration data from configuration EEPROM and programming the external DC-DC power IC. The IIC is available via the serial transfer clock line (SCL) and the serial data in-output (SDA). The clock frequency is selected in configuration EEPROM(002h).
The frequency of SCL = Main clock frequency / {(SCL Clock Speed in EEPROM+1) x 5}
The default of SCL Clock Speed is 0Fh. The following diagram is typical IIC interface protocol.



The LGDP4234 recognizes the start of data transfer on the falling edge of CS* input and transfers the start byte. It recognizes the end of data transfer on the rising edge of CS* input. The LGDP4251 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LGDP4234 correspond as a result of comparison. When selected, the LGDP4234 starts taking subsequent data. The ID pin sets the least significant bit of the identification code. Send "01110" to the identification code, which is the five upper bits of the start byte. Two different chip addresses must be assigned to the LGDP4234 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = "0", either index register write operation or status read operation is executed. When RS = "1", either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). Data are received when the R/W bit is "0", and are transferred when the R/W bit is "1".

After receiving the start byte, the LGDP4234 starts transferring or receiving data in units of bytes. Data transfer is executed from the MSB. All instructions of the LGDP4234 take a 16-bit format and are executed internally after transferring two bytes (DB[15:0]) from the MSB. GRAM write data are internally expanded into 18 bits. After receiving the start byte, the LGDP4234 takes the first and the second byte as the upper and the lower eight bits of a 16-bit instruction, respectively.

In SPI mode, invalid data are sent to the data bus until 5-byte data are read out from the internal GRAM after the start byte. Valid data are read out as the LGDP4234 reads out the 6th byte data from the internal GRAM.