SHARP

Data Sheet

LH28F016SCT
16M Flash Memory

FEATURES

- SmartVoltage Technology
  - 2.7 V (Read Only), 3.3 V or 5 V V_{CC}
  - 3.3 V, 5 V, or 12 V V_{PP}
- High Performance Read Access Time
  - 95 ns (5 V ±0.25 V)
  - 100 ns (5 V ±0.5 V)
  - 120 ns (3.3 V ±0.3 V)
  - 150 ns (2.7 V - 3.6 V)
- High Density Symmetrically-Blocked Architecture
  - Thirty-two 64KB Erasable Blocks
- Low Power Management
  - Deep Power Down Mode
  - Automatic Power Savings Mode Decreases I_{CC} in Static Mode
- Enhanced Data Protection Features
  - Absolute Protection with V_{PP} = GND
  - Flexible Block Locking
  - Block Erase/Byte Write Lockout during Power Transitions
- Automated Byte Write and Block Erase
  - Command User Interface
  - Status Register
- Enhanced Automated Suspend Options
  - Byte Write Suspend to Read
  - Block Erase Suspend to Byte Write
  - Block Erase Suspend to Read
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
  - 3.2 Million Block Erase Cycles/Chip
- SRAM Compatible Write Interface
- Industry Standard Packaging
  - 40-Lead TSOP
- Operating Temperature
  - 0°C to +70°C
- ETOX™ Nonvolatile Flash Technology
- CMOS Process (P-type Silicon Substrate)
- Not Designed or Rated as Radiation Hardened

DESCRIPTION

SHARP's LH28F016SCT Flash memory with Smart-Voltage technology is a high density, low cost, nonvolatile, read/write storage solution for a wide range of applications. Its symmetrically blocked architecture, flexible voltage, and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code and data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F016SCT offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F016SCT is manufactured on SHARP's 0.38 μm ETOX™ V process technology. Available in the industry-standard package of 40-lead TSOP, it is ideal for board-constrained applications. The LH28F0016SCT is based on the 28F008SA architecture, and is a quick and easy upgrade for designs demanding the state-of-the-art.

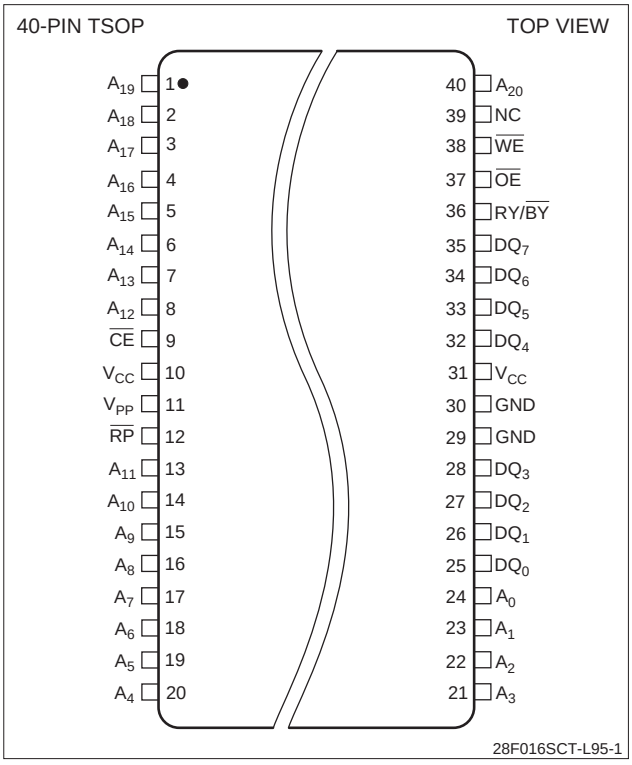


Figure 1. LH28F016SCT Pinout

* ETOX is a trademark of Intel Corporation.

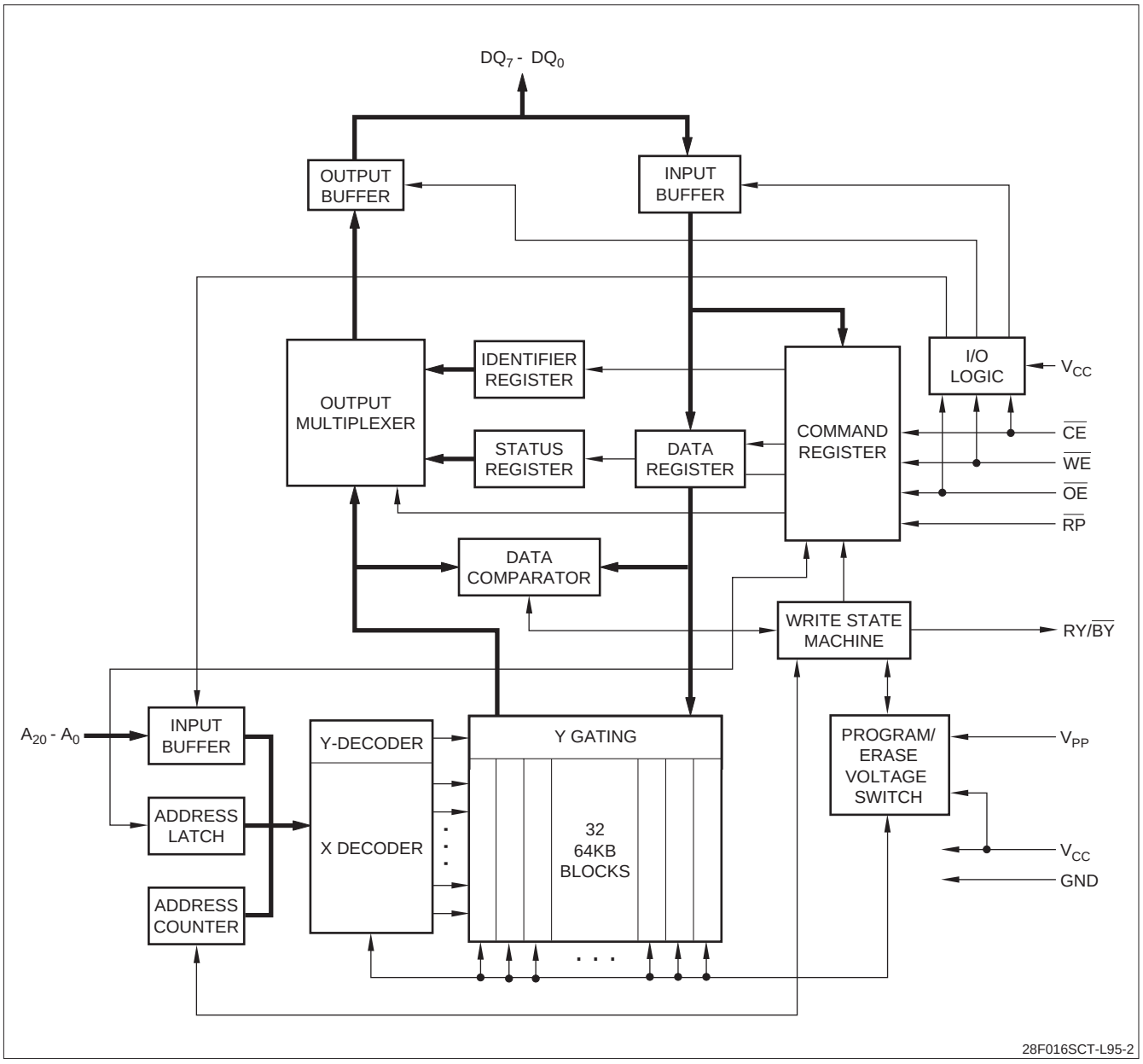


Figure 2. LH28F016SCT Block Diagram

Table 1. Pin Descriptions

SYMBOL	TYPE	DESCRIPTION
A_{20} - A_0	Input	**Address Inputs** Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle.
DQ_7 - DQ_0	Input/ Output	**Data Input/Outputs** Inputs data and commands during CUI write cycles; outputs data during memory array, status register, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	Input	**Chip Enable** Activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$ HIGH deselects the device and reduces power consumption to standby levels.
$\overline{RP}$	Input	**Reset/Deep Power-down** Puts the device in deep power-down mode and resets internal automation. $\overline{RP}$ HIGH enables normal operation. When driven LOW, $\overline{RP}$ inhibits write operations which provides data protection during power transitions. Exiting from deep power-down sets the device to read array mode. $\overline{RP}$ at V_{HH} enables setting of the master lock-bit and enables configuration of block lock-bits when the master lock-bit is set. $\overline{RP} = V_{HH}$ overrides block lock-bits thereby enabling block erase and byte write operations to locked memory blocks. Block erase, byte write, or lock-bit configuration with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.
$\overline{OE}$	Input	**Output Enable** Gates the device's outputs during a read cycle.
$\overline{WE}$	Input	**Write Enable** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.
RY/$\overline{BY}$	Output	**Read/$\overline{Busy}$** Indicates the status of the internal WSM. When LOW, the WSM is performing an internal operation (block erase, byte write, or lock-bit configuration). RY/$\overline{BY}$ HIGH indicates that the WSM is ready for new commands, block erase is suspended, and byte write is inactive, byte write is suspended, or the device is in deep power-down mode. RY/$\overline{BY}$ is always active and does not float when the chip is deselected or data outputs are disabled.
V_{PP}	Supply	**Block Erase, Byte Write, Lock Bit Configuration Power Supply** For erasing array blocks, writing bytes, or configuring lock-bits. With $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. Block erase, byte write, and lock-bit configuration with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attemped.
V_{CC}	Supply	**Device Power Supply** Internal detection configures the device for 2.7 V, 3.3 V, or 5 V operation. To switch from one voltage to another, ramp V_{CC} down to GND and then ramp V_{CC} to the new voltage. Do not float any power pins. With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see 'DC Characteristics) produce spurious results and should not be attempted. Block erase, byte write and lock-bit configuration operations with $V_{CC} < 3.0$ V are not supported.
GND	Supply	**Ground** Do not float any ground pins.
NC		**Non-connect** Lead is not internal connected; it may be driven or floated.

OVERVIEW

The LH28F160SCT-L95 is a high-performance 16M SmartVoltage Flash memory organized as 2MB × 8 bits. The 2MB of data is arranged in thirty-two 64KB blocks which are indivdually eraseable, lockable, and unlockable in-system. The memory map is shown in Figure 3.

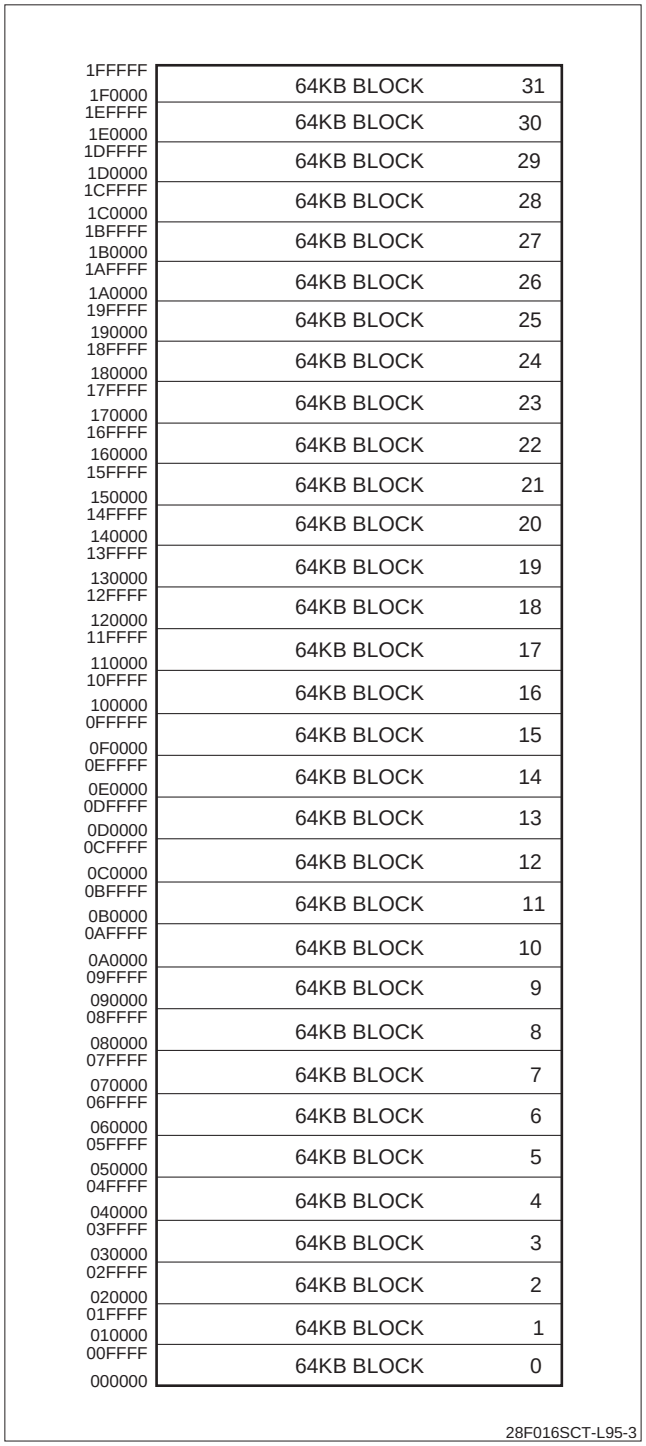


Figure 3. Memory Map

SmartVoltage technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 2, to meet system performance and power expectations. 2.7 V V_{CC} consumes approximately one-fifth the power of 5 V V_{CC}, V_{PP} at 3.3 V, and 5 V eliminates the need for a separate 12 V converter, while V_{PP} = 12 V maximizes block erase and byte write performance. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 2. V_{CC} and V_{PP} Voltage Combinations Offered by SmartVoltage Technology

V_{CC} VOLTAGE	V_{PP} VOLTAGE
2.7 V (See Note)	
3.3 V	3.3 V, 5 V, 12 V
5 V	5 V, 12 V

NOTE: Block erase, byte write and lock-bit configuration operations with V_{CC} < 3 V are not supported.

Internal V_{CC} and V_{PP} detection cicuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interfaces between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, byte write, and lock-bit configuration operations.

A block erase operation erases one of the device's 64KB blocks typically within 1 second (5 V V_{CC}, 12 V V_{PP}) independent of other blocks. Each block can be independently erased 100,000 times. (3.2 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read from or write data to any other block.

Writing memory data is performed in byte increments typically within 6 µs (5 V V_{CC}, 12 V V_{PP}). Byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits, thirty-two block lock-bits and a master lock-bit, to lock and unlock blocks. Block lock-bits gate block erase and byte write operations, while the master lock-bit gates block lock-bit modification. Lock-bit confifuration operations (Set Block Lock-Bit, Set Master Lock-Bit, and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM's block erase, byte write, or lock-bit configuration operation is finished.

The RY/$\overline{BY}$ output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/$\overline{BY}$ minimizes both CPU overhead and system power consumption. When LOW, RY/$\overline{BY}$ indicates that the WSM is performing a block erase, byte write, or lock-bit configuration.

RY/$\overline{BY}$ HIGH indicates that the WSM is ready for a new command, block erase is suspended (and byte write is inactive), byte is suspended, (and byte write is inactive), byte write is suspended, or the device is in deep power-down mode.

The access time is 95 ns (t_{AVQV}) over the commerical temperature range (0°C to 70°C) and V_{CC} supply voltage range of 4.75 V - 5.25 V. At lower V_{CC} voltages, the access times are 100 ns (4.5 V - 5.5 V), 120 ns (3.0 V - 3.6 V) and 150 ns (2.7 V - 3.6 V).

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (address not switching). In APS mode, the typical I_{CCR} current is 1 mA at 5 V V_{CC}.

When $\overline{CE}$ and $\overline{RP}$ pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the $\overline{RP}$ pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during Reset. A reset time (t_{PHQV}) is required from $\overline{RP}$ going HIGH until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from $\overline{RP}$ HIGH until writes to the CUI are recognized. With $\overline{RP}$ at GND, the WSM is reset and the status register is cleared. The device is available in 40-pin TSOP packaging. Pinout is as shown in Figure 1.

PRINCIPLES OF OPERATION

The LH28F016SCT SmartVoltage flash memory includes an on-chip Write State Machine (WSM) to manage block erase, byte write, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, byte write, and lock-bit configuration, and minimal process overhead with RAM-like interface timings.

After initial device power-up or return from Reset mode (see 'Bus Operations' section), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the Command User Interface (CUI), independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erase, byte writing, and lock-bit configuration. All functions associated with altering memory contents-block erase, byte write, lock-bit configuration, status, and identifier codes are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, byte write, and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase, byte write, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Byte write suspend allows system software to suspend a byte write to read data from any other flash memory array location.

Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erase, byte writes, or lock-bit configurations are required) or hardwired to $V_{PPH1/2/3}$. The device accommodates either design practice and encourages optimaization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with the two-step block erase, byte write, or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when $\overline{RP}$ is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, and byte write operations.

BUS OPERATION

The local CPU reads and writes the flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Read

Information, identifier codes, or a status register can be read from any block, independent of the V_{PP} voltage. $\overline{RP}$ can be either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to Read Array mode. Four control pins dictate the data flow in and out of the device: $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, $\overline{RP}$, and $\overline{RP}$. $\overline{CE}$ and $\overline{OE}$ must be driven active to obtain data at the outputs. $\overline{CE}$ is the device selection control and when active enables the selected memory device. $\overline{OE}$ is the data output (DQ_7 - DQ_0) control and when active, drives the selected memory data onto the I/O bus. $\overline{WE}$ must be at V_{IH} or V_{HH}. See Figure 15 for Read Cycle waveforms.

Output Disable

With $\overline{OE}$ at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ_7 - DQ_0 are placed in a high-impedance state.

Standby

$\overline{CE}$ at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_7 - DQ_0 outputs are placed in a high-impedance state independent of $\overline{OE}$. If deselected during block erase, byte write, or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

Deep Power-down

$\overline{RP}$ at V_{IL} initiates the deep power-down mode.

In read modes, $\overline{RP}$ LOW deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. $\overline{RP}$ must be held LOW for a minimum of 100 ns. Time t_{PHQV} is required after the return from power-down mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to Read Array mode and status register is set to 80H.

During block erase, byte write, or lock bit configuration modes, $\overline{RP}$ at LOW will abort the operation. RY/$\overline{BY}$ remains LOW until the Reset operation is complete. Memory contents in the process of being altered are no longer valid; data may be partially erased or written. Time t_{PHWL} is required after $\overline{RP}$ goes HIGH (V_{IH}) before another command can be written.

As with any automated device, it is important to assert $\overline{RP}$ during system reset. When the system comes out of Reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, byte write or block lock bit configuration. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the $\overline{RP}$ input. For this application, $\overline{RP}$ is controlled by the same $\overline{RESET}$ signal that resets the system CPU.

Read Identifier Codes

The Read Identifier Codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and the master lock configuration code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and the master lock-bit setting.

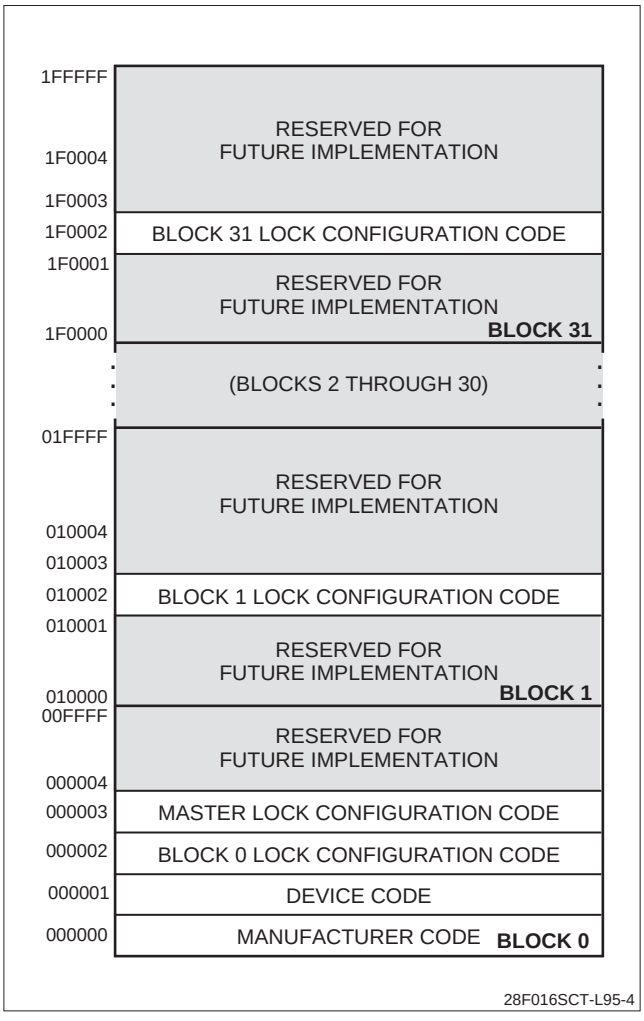


Figure 4. Device Identifier Code Memory Map

Write

Writing commands to the CUI controls the reading of device data and identifier codes. They also control inspection and clearing of the status register. When $V_{PP} = V_{PP1/2/3}$ the CUI also controls block erase, byte write and block write, and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/Byte Write command requires the command and address of the location to be written. Set Block Lock Bit commands require the command and block address within the device (Block Lock) to be locked. The Clear Block Lock bits command requires the command and an address within the device.

The CUI does not occupy an addressable memory location. It is written when $\overline{WE}$ and $\overline{CE}$ are active. The address and data needed to execute a command are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes HIGH first). Standard microprocessor write timing is used. Figures 16 and 17 illustrate $\overline{WE}$ and $\overline{CE}$ controlled write operations.

Table 3. Bus Operations

MODE	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS	V_{PP}	DQ_7 - DQ_0	RY/$\overline{BY}$	NOTES
Read	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	x	x	D_{OUT}	x	1, 2, 3, 8
Output Disable	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	x	x	High-Z	x	3
Standby	V_{IH} or V_{HH}	V_{IH}	x	x	x	x	High-Z	x	3
Deep Power-down	V_{IL}	x	x	x	x	x	High-Z	V_{OH}	4
Read Identifier Codes	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	x	See Note 5	V_{OH}	8
Write	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	x	x	D_{IN}	x	3, 6, 7, 8

NOTES:

1. x = don't care. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered. Refer to DC Characteristics.
2. 'x' (don't care) can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/32}$ for V_{PP}. For V_{PPLK} and $V_{PPH1/2/3}$ voltages see DC Characteristics.
3. RY/$\overline{BY}$ is V_{OL} when the WSM is executing internal block erase, byte write, or lock-bit configuration algorithms. It is VOH during when the WSM is not busy, in block erase suspend mode (with byte write inactive), byte write suspend mode, or deep power-down mode.
4. $\overline{RP}$ at GND +0.2 V ensures the lowest deep power-down current.
5. See the Read Identifier Codes Command section.
6. Command writes involving block erase, write, or lock-bit configuration are reliably executed when $V_{PP} = V_{PPH1/2/3}$ and $V_{CC} = V_{CC2/3/4}$. Block erase, byte write, or lock-bit configuration with $V_{CC} < 3.0$ V or $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attemped.
7. See Table 4 for valid D_{IN} during a write operation.
8. Do not hold both $\overline{OE}$ and $\overline{WE}$ at V_{IL} at the same time.

COMMAND DEFINITIONS

When $V_{PP} \leq V_{PPLK}$, Read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{PPH1/2/3}$ on V_{PP} enables block erase, byte write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 4. Command Definitions

COMMAND	BUS CYCLES REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTES
		OPER.[1]	ADDR.[2]	DATA[3]	OPER.[1]	ADDR.[2]	DATA[3]	
Read Array/Reset	1	Write	x	FFH				
Read Identifier Codes	≥ 2	Write	x	90H	Read	IA	ID	4
Read Status Register	2	Write	x	70H	Read	x	SRD	
Clear Status Register	1	Write	x	50H				
Block Erase	2	Write	BA	20H	Write	BA	D0H	5
Byte Write	2	Write	WA	40H or 10H	Write	WA	WD	5, 6
Block Erase and Byte Write Suspend	1	Write	x	B0H				5
Block Erase and Byte Write Resume	1	Write	x	D0H				5
Set Block Lock-Bit	2	Write	BA	60H	Write	BA	01H	7
Set Master Lock-Bit	2	Write	x	60H	Write	x	F1H	7
Clear Block Lock-Bits	2	Write	x	60H	Write	x	D0H	8

NOTES:

1. Bus operations are defined in Table 3.
2. x = don't care; in this case, any valid address within the device.
   IA = Identifier Code Address, see Figure 4.
   BA = Address within the block being erased or locked.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. For a description of the status register bits see Table 7.
   WD = Data to be written at location WA. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes HIGH first).
   ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. For read identifier code data see 'Read Identifier Codes Command' section.
5. If the block is locked $\overline{RP}$ must be at V_{HH} to enable block erase or byte write operations. Attempts to issue a block erase or byte write to a locked block while $\overline{RP}$ is V_{IH} will fail.
6. Either 40H or 10H is recognized by the WSM as the byte write setup.
7. If the master lock-bit is set, RP must be at V_{HH} to set a block lock-bit. RP must be at V_{HH} to set the master lock-bit. If the master lock-bit is not set, a block lock-bit can be set while RP is V_{IH}.
8. If the master lock-bit is set, $\overline{RP}$ must be at V_{HH} to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits. If the master lock-bit is not set, the Clear Block Lock-Bits command can be done while $\overline{RP}$ is V_{IH}.
9. Commands other than those shown in Table 4 are reserved by SHARP for future device implementations and should not be used.

Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to Read Array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, byte write or block lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Byte Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and $\overline{RP}$ must be V_{IH} or V_{HH}.

Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer, device, block lock configuration and master lock configuration codes (see Table 5 for identifier code values). To terminate the operation, write another valid command, such as a Read Array command. The Read Identifier Codes command functions independently of the V_{PP} voltage and $\overline{RP}$ must be at V_{IH} or V_{HH}. After issuing the the Read Identifier Codes command, the information can be read:

Table 5. Identifier Codes

CODE	ADDRESS	DATA
Manufacturer Code	00000	89
Device Code	00001	AA
Block Lock Configuration	x0002*	
Block is Unlocked		$DQ_0 = 0$
Block is Locked		$DQ_0 = 1$
Reserved for Future Use		$DQ_7 = DQ_1$
Master Lock Configuration	00003	
Block is Unlocked		$DQ_0 = 0$
Device is Locked		$DQ_0 = 1$
Reserved for Future Use		$DQ_7 = DQ_1$

NOTE: *'x' Selects the specific block lock configuration code to be read. See Figure 4 for the device identifier code memory map.

Read Status Register Command

The status register may be read to determine when a block erase, byte write or block lock bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$ whichever occurs first. $\overline{OE}$ or $\overline{CE}$ must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. $\overline{RP}$ must be V_{IH} or V_{HH}.

Clear Status Register Command

When status register bits SR.5, SR.4, SR.3, or SR.1 are set to '1' by the WSM, they can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 7). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} voltage. $\overline{RP}$ can be V_{IH} or V_{HH}. This command does not function during block erase or byte write suspend modes.

Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by a block erase confirm. This command sequence requires appropriate sequencing plus an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing the output data of the RY/$\overline{BY}$ pin or status register bit SR.7. When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to '1'. Also reliable block erasure can only occur when $V_{CC} = V_{CC2/3/4}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to '1'. Successful block erase requires that the corresponding block lock-bit be cleared or, if set, that $\overline{RP} = V_{HH}$. If block erase is attempted when the corresponding block lock-bit is set and $\overline{RP} = V_{HH}$, SR.1 and SR.5 will be set to '1'. Block erase operations with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

Byte Write Command

Word/Byte writes are executed by a two-cycle command sequence. Byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of $\overline{WE}$). The WSM then takes over, controlling the byte write and write verify algorithms internally. After the byte write sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect the completion of the byte write event by analyzing the RY/$\overline{BY}$ pin or status register bit SR.7.

When the byte write is complete, status register bit SR.4 should be checked. If a byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for '1' bits that do not successfully write to '0'. The CUI remains in read status register mode until it receives another command.

Reliable byte writes can only occur when $V_{CC} = V_{CC2/3/4}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against byte writes. If a byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to '1'. A successful byte write requires that the corresponding block lock bit be cleared or, if set, that the corresponding block lock-bit be cleared or, if set, that $RP = V_{HH}$. If byte write is attempted when the corresponding block lock-bit is set and $\overline{RP} = V_{IH}$, SR.1 and SR.4 will be set to '1'. Byte write operations with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or byte-write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to '1'). RY/$\overline{BY}$ will also transition to V_{OH}. Specification t_{WHRh2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which are suspended. A Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Byte Write Suspend command, a (multi) word/byte write operation can also be suspended. During a byte write operation with block erase suspended, status register bit SR.7 will return to '0' and the RY/$\overline{BY}$ output will transition to V_{OL}. However, SR.6 will remain '1' to indicate the block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/$\overline{BY}$ will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 7). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for block erase) while block erase is suspended. $\overline{RP}$ must also remain at V_{IH} or V_{HH}. (the same $\overline{RP}$ level used for block erase). Block erase cannot resume until (multi) word/byte write operations initiated during block erase suspend have completed.

Byte Write Suspend Command

The Byte Write Suspend command allows for a byte write interruption to read data in other flash memory locations. Once the byte write process starts, writing the Byte Write Suspend command requests that the WSM suspend the byte write sequence. The device continues to output status register data when read after the Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the byte write operation has been suspended (both will be set to '1'). RY/$\overline{BY}$ will also transition to V_{OH}. The timing of t_{WHRH1} defines the byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which are suspended. The only other valid commands while byte write is suspended are Read Status Register and Byte Write Resume. After the Byte Write Resume command is written to the flash memory, the WSM will continue the byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/$\overline{BY}$ will return to V_{OL}. After the Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 8). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for byte write) while in byte write suspend mode. $\overline{RP}$ must also remain at V_{IH} or V_{HH}. (the same $\overline{RP}$ level used for write).

Set Block and Master Lock Bit Commands

A flexible block locking and unlocking scheme is implemented via a combination of block lock bits and a master lock bit. The block lock bits gate program and erase operations while the master lock bit gates block lock bit modification. With the master lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Master Lock-Bit command, in conjunction with $\overline{RP} = V_{HH}$, sets the master lock-bit. After the master lock-bit is set, subsequent setting of block lock-bits requires both the Set Block Lock-Bit command and V_{HH} on the $\overline{RP}$ pin. See Table 6 for a summanry of hardware and software write protection options.

The set block lock bit is executed by a two-cycle command sequence. The set block or master lock bit setup along with appropriate block or device address is written followed by the set block lock bit confirm (and an address within the block to be locked) or the set master lock bit confirm (and any device address). The WSM then controls the set block lock bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 9). The CPU can detect the completion of the set lock bit event by analyzing the RY/$\overline{BY}$ pin output or status register bit SR.7.

When the set lock bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that block lock bits are not accidentally set. An invalid Set Block or Master Lock-Bit command will result in status register bits SR.4 and SR.5 being set to '1'. Also, reliable operations occur only when $V_{CC} = V_{CC2/3/4}$ and $V_{PPW} = V_{PPH1/2/3}$. In the absence of this high voltage, lock bit contents are protected against alteration.

A successful set block lock bit operation also requires that the master lock bit be cleared or, if the master lock bit is set, that $\overline{RP} = V_{HH}$. If it is attempted with the master lock bit set and $\overline{RP} = V_{IH}$, SR.1 and SR.4 will be set to '1' and the operation will fail. Set block lock bit operations while $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted. A successful set master lock bit operation requires that $\overline{RP} = V_{IH}$. If it is attempted with $\overline{RP} = V_{IH}$, SR.1 and SR.4 will be set to '1' and the operation will fail. Set master lock bit operations with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

Clear Block Lock Bit Command

All set block lock bits are cleared in parallel via the Clear Block Lock Bits command. With the master lock bit cleared, block lock bits can be cleared using only the Clear Block Lock Bits command. If the master lock bit is set, clearing block lock bits requires both the Clear Block Lock Bits command and V_{HH} on the $\overline{RP}$ pin. See Table 6 for a summary of hardware and software write protection options.

The Clear Block Lock Bits operation is executed by a two-cycle command sequence. First, a clear block lock bit setup code is written. After the command is written, the device automatically outputs status register data when read (see Figure 10). The CPU can detect completion of the clear block lock bit event by analyzing the RY/$\overline{BY}$ pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock bits are not accidentally cleared. An invalid Clear Block Lock bits command sequence will fail, and result in status register bits SR.4 and SR.5 being set to '1'. Also, a reliable clear block lock bits operation can only occur when $V_{CC} = V_{CC2/3/4}$ and $V_{PP} = V_{PP1/2/3}$. If a clear block lock bits operation is attempted while $V_{PP} \leq V_{PPLK}$, it will fail. SR.3 and SR.5 will be set to '1'. In the absence of this high voltage, the block lock bits are protected against alteration. A successful clear block lock bits operation requires that the master lock bit is cleared or, if the master lock bit is set, that $\overline{RP} = V_{HH}$. If it is attempted with the master lock-bit set and $\overline{RP} = V_{IH}$, SR.1 and SR.5 will be set to '1' and the operation will fail. A clear lock bits operation with $V_{IH} < RP < V_{HH}$ produce spurious results and should not be attempted.

If a clear block lock bits operation is aborted due to a V_{PP} or V_{CC} transition out of valid range or a $\overline{RP}$ active transition, block lock bit values are left in an unpredictable state. A repeat of the clear block lock bits operation is required to initialize block lock bit contents to known values. Once the master lock bit is set, it cannot be cleared.

Table 6. Write Protection Methods

OPERATION	MASTER LOCK BIT	BLOCK LOCK-BIT	$\overline{RP}$	EFFECT
Block Erase or Byte Write	x	0	V_{IH} or V_{HH}	Block Erase and Byte Write enabled
		1	V_{IH}	Block is locked. Block Erase and Byte Write disabled
			V_{HH}	Block Lock Bit override. Block Erase and Byte Write enabled
Set Block Lock Bit	0	x	V_{IH} or V_{HH}	Set Block Lock Bit enabled
	1	x	V_{IH}	Master Lock Bit is set. Set Block Lock Bit disabled
			V_{HH}	Master Lock Bit override. Set Block Lock Bit enabled
Set Master Lock Bit	x	x	V_{IH}	Set Master Lock Bit disabled
			V_{HH}	Set Master Lock Bit enabled
Clear Block Lock Bits	0	x	V_{IH} or V_{HH}	Clear block lock bits enabled
	1	x	V_{IH}	Master Lock Bit is set. Clear Block Lock Bits disabled
			V_{HH}	Master Lock Bit override. Clear Block Lock Bits enabled

Status Register

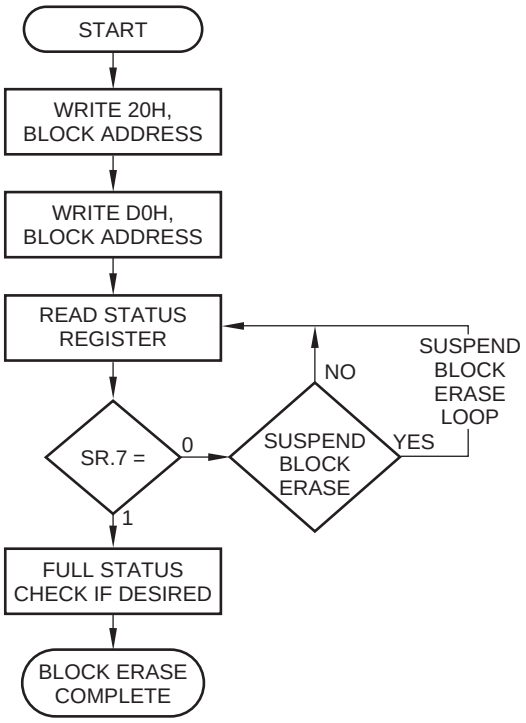
7	6	5	4	3	2	1	0
WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	///

Table 7. Status Register Definitions

REGISTER NUMBER	REGISTER SYMBOL	DEFINITION	NOTES
SR.7	WSMS	Write State Machine Status 1 = Ready 0 = Busy	1
SR.6	ESS	Erase Suspend Status 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5	ECLBS	Erase and Clear Lock Bits Status 1 = Error in Block Erase, or Clear Block Lock Bits 0 = Successful Block Erase, or Clear Block Lock Bits	2
SR.4	BWSLBS	Byte Write and Set Lock Bit Status 1 = Error in Byte Write or Set Block Lock Bit 0 = Successful Byte Write or Set Master/Block Lock Bit	2
SR.3	VPPS	V_{PP} Status 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	3
SR.2	BWSS	Byte Write Suspend Status 1 = Byte Write Suspended 0 = Byte Write in Progress/Completed	
SR.1	DPS	Device Protect Status 1 = Block Lock Bit, Block lock bit and/or $\overline{RP}$ lock detected, operation abort 0 = Unlock	4
SR.0	///	Reserved for Future Enhancements	5

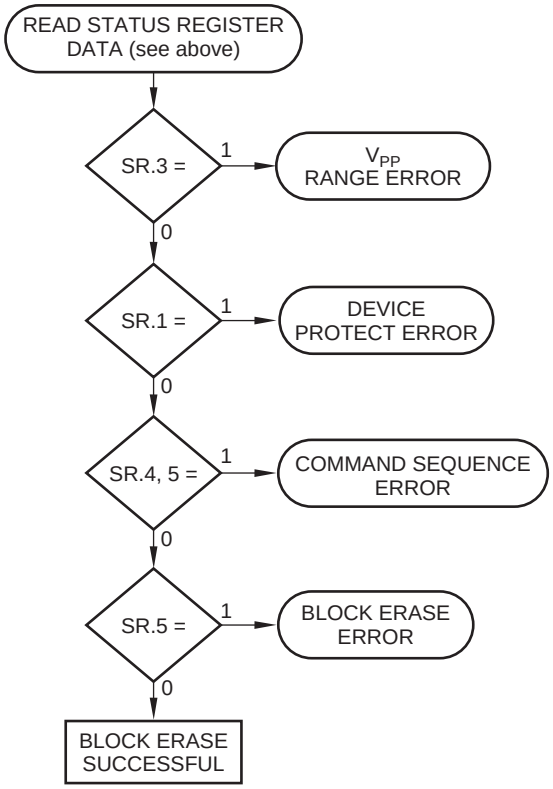
NOTES:

1. Check RY/$\overline{BY}$ or SR.7 to determine block erase, byte write or block lock bit configuration completion. SR.6 - SR.0 are invalid while SR.7 = 0.
2. If both SR.5 and SR.4 =1 after a block erase, or block lock bit configuration attempt, an improper command sequence was entered.
3. SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after block erase, byte write, set block/master or lock bit or Clear Block lock bits command sequences. SR.3 does not report accurate feedback when $V_{PP} \neq V_{PPH1/2/3}$.
4. SR.1 does not provide a continuous indication of master and block lock bit values. The WSM interrogates the master lock bit, block lock bit, and $\overline{RP}$ only after block erase, byte write, or lock bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set, master lock bit is set, and/or $\overline{RP}$ is not V_{HH}. Reading the block lock and master lock configuration codes after writing the Read Identifier Codes command indicates master and block lock bit status.
5. SR.0 is reserved for future use and should be masked out when polling the status register.



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each block erase or after a sequence of block erasures. Write FFH after the last operation to place the device into read array mode.		

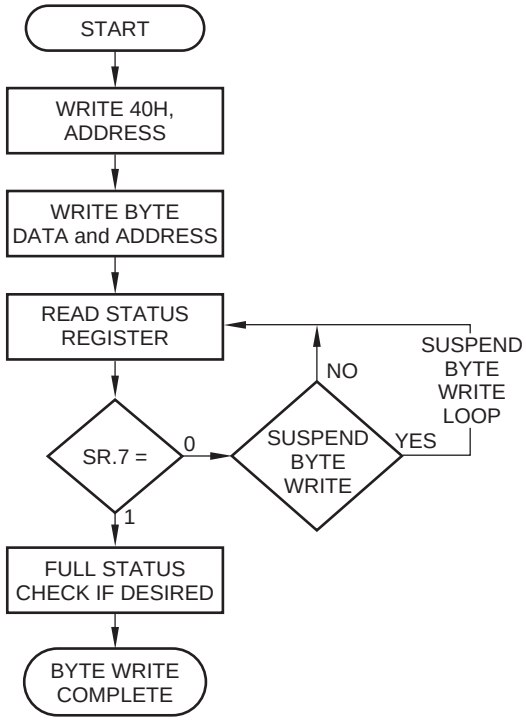
FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect $\overline{RP}$ = V_{IH}, Block Lock-Bit is Set. Only required for systems implementing lock-bit configuration.
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
CSR.5, SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If an error is detected, clear the Status Register before attempting a retry or other error recovery operations.		

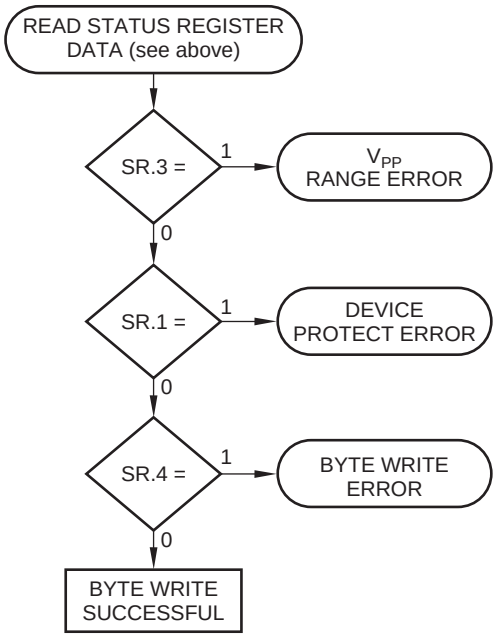
28F016SCT-L95-5

Figure 5. Automated Block Erase Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Setup Byte Write	Data = 40H Addr = Location to be Written
Write	Byte Write	Data = Data to be Written Addr = Location to be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent byte writes. SR full status check can be done after each byte write, or after a sequence of byte writes. Write FFH after the last byte write operation to place the device into read array mode.		

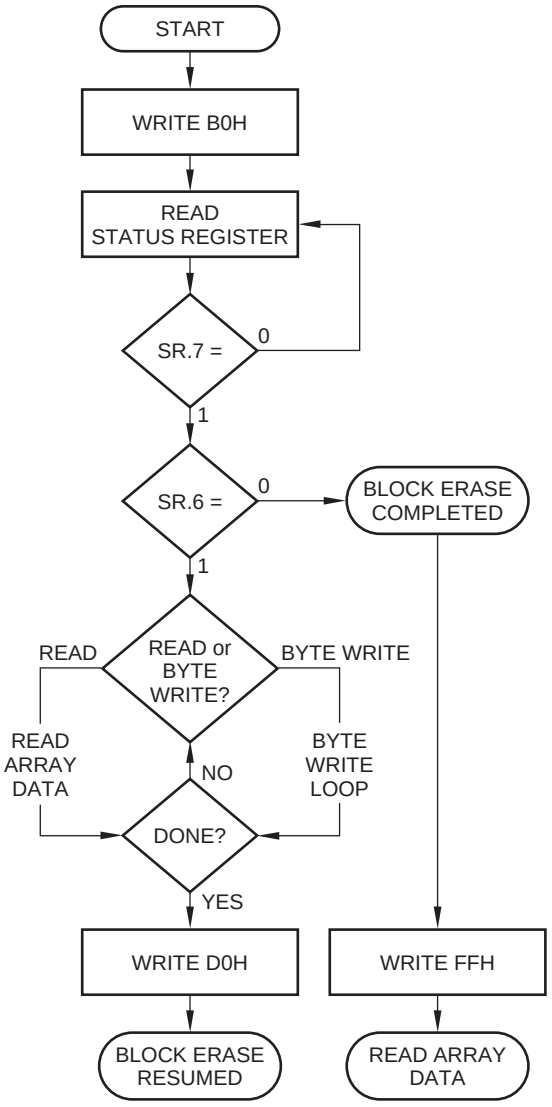
FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect $\overline{RP}$ = V_{IH}, Block Lock-Bit is Set. Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1 = Data Write Error
SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked. If an error is detected, clear the Status Register before attempting a retry or other error recovery operations.		

28F016SCT-L95-6

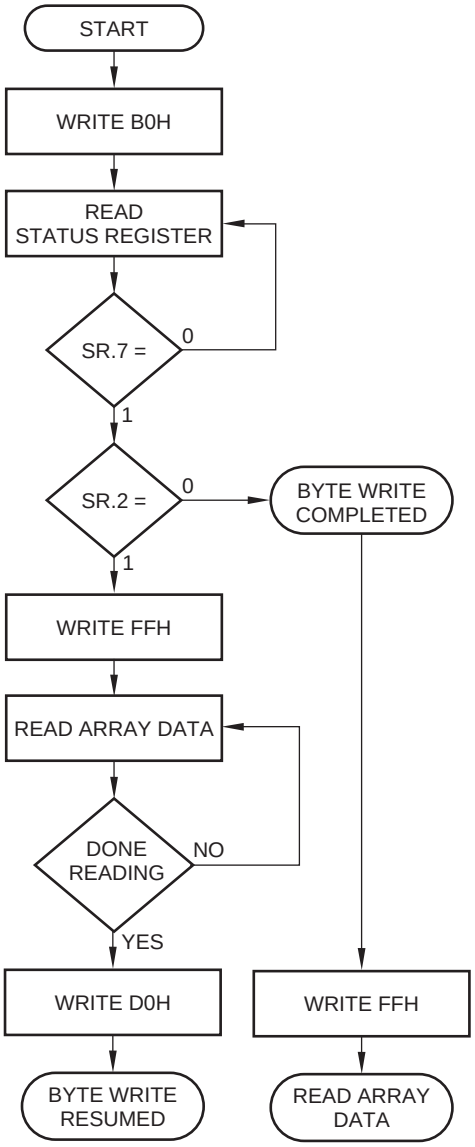
Figure 6. Automated Byte Write Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

28F016SCT-L95-7

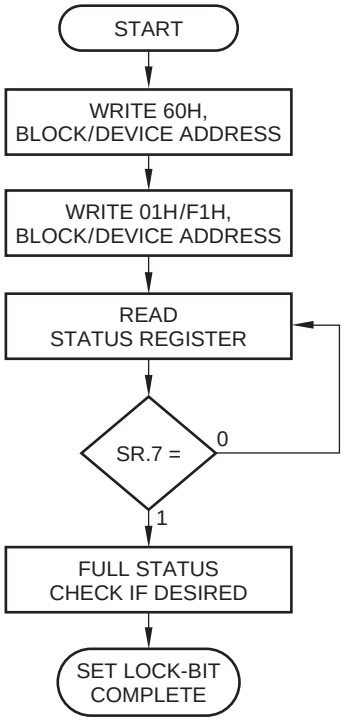
Figure 7. Block Erase Suspend/Resume Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Byte Write Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Byte Write Suspended 0 = Byte Write Completed
Write	Read Array	Data = FFH Addr = X
Read		Read Array locations other than that being written
Write	Byte Write Resume	Data = D0H Addr = X

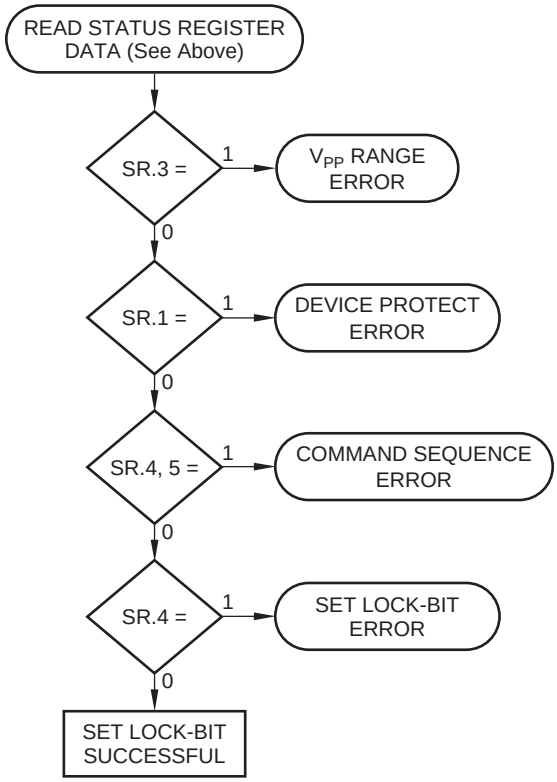
28F016SCT-L95-8

Figure 8. Byte Write Suspend/Resume Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Set Block/Master Lock-Bit Setup	Data = 60H Addr = Block Address (Block), Device Address (Master)
Write	Set Block or Master Lock-Bit Confirm	Data = 01H (Block), F1H (Master) Addr = Block Address (Block), Device Address (Master)
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent lock-bit set operations. Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations. Write FFH after the last lock-bit set operation to place the device into read array mode.		

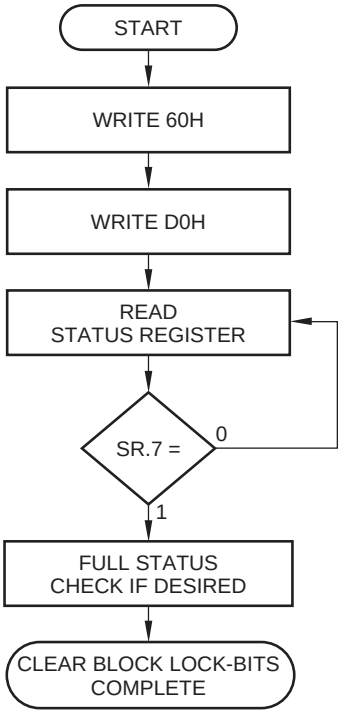
FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect $\overline{RP}$ = V_{IH} (Set Master Lock-Bit Operation) $\overline{RP}$ = V_{IH}, Master Lock-Bit is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Error
SR.5, SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked. If an error is detected, clear the Status Register before attempting a retry or other error recovery operations.		

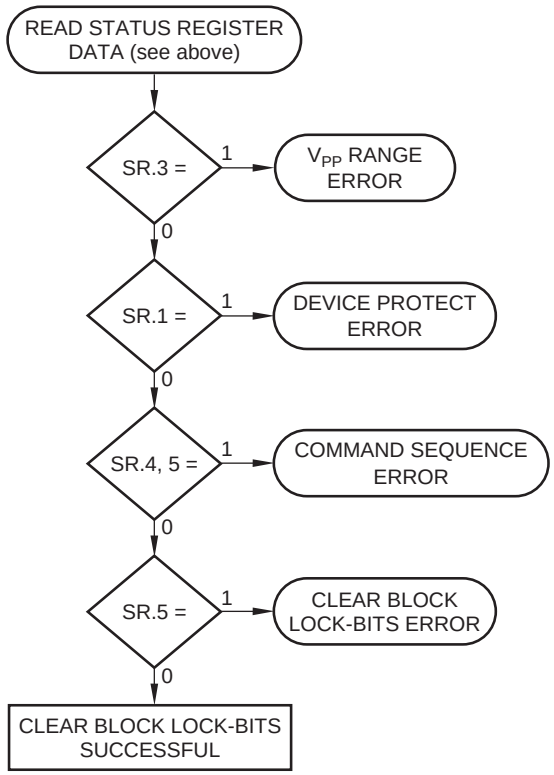
28F016SCT-L95-9

Figure 9. Set Block and Master Lock-bit Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the Clear Block Lock-Bits operation to place the device into read array mode.		

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect $\overline{RP}$ = V_{IH} Master Lock-Bit is Set
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error
SR.5, SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register command. If an error is detected, clear the Status Register before attempting a retry or other error recovery operation.		

28F016SCT-L95-10

Figure 10. Clear Block Lock-bits Flowchart

DESIGN CONSIDERATIONS

Three-line Output Control

Since this device will often be used in large memory arrays, SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

- Lowest possible memory power dissipation
- Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable $\overline{CE}$ while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. $\overline{RP}$ should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

RY/$\overline{BY}$ and Block Erase, Byte Write, and Block Lock Bit Configuration Polling

RY/$\overline{BY}$ is a full CMOS output that provides a hardware method of detecting block erase, byte write and lock bit configuration completion. It transitions LOW after block erase, byte write, or lock bit configuration commands and returns to V_{OH} when the WSM has finished executing the internal algorithm.

RY/$\overline{BY}$ can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/$\overline{BY}$ is also V_{OH} when the device is in block erase suspend (with byte write inactive), byte write suspend or deep power-down modes.

Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of $\overline{CE}$ and $\overline{OE}$. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

V_{PP} Trace On Printed Circuit Boards

Updating Flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for byte writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

V_{CC}, V_{PP}, $\overline{RP}$ Transitions

Block erase, full chip erase, (multi) word/byte writes and lock bit configurations are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2/3}$ range, if V_{CC} falls outside of a valid $V_{CC1/2}$ range, or $\overline{RP} \neq V_{IL}$. If a V_{PP} error is detected, status register bit SR.3 is set to '1' along with SR.4 or SR.5, depending on the attempted operation. If $\overline{RP}$ transitions to V_{IL} during block erase, full chip erase, (multi) word/byte write or block lock bit configuration (RY/$\overline{BY}$ will remain LOW until the reset operation is complete) the operation will abort and the device will enter reset mode. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or $\overline{RP}$ transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Upon power-up, its state is read array mode after exiting from reset mode or after V_{CC} transitions below V_{LKO}.

After block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

Power-Up/Down Protection

The device is designed to offer protection against accidental block erase, byte write or block lock bit configuration during power transitions. The device is indifferent as to which power supply (V_{PP} or V_{CC}) powers up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against accidental writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be LOW for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides an added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while $\overline{RP} = V_{IL}$ regardless of its control input states.

Power Dissipation

When designing portable systems, designers will consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power needs to remain applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume far less power by lowering $\overline{RP}$ to V_{IL} standby or sleep modes. If access is needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after $\overline{RP}$ is first raised to V_{IH}. See 'AC Characterstics, Read Only and Write Operations' and Figures 15, 16, and 17 for more information.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	CONDITION	MIN.	MAX.	NOTE
Operating Temperature	During Read, Block Erase, Byte Write, and Lock Bit Configuration	0°C	70°C	1
	Under Bias	-10°C	80°C	
Storage Temperature		-65°C	125°C	
Voltage on any pin	Except V_{CC}, V_{PP}, and $\overline{RP}$	-2.0 V	7.0 V	2
V_{CC} Supply Voltage		-2.0 V	7.0 V	2
V_{PP} Supply Voltage	During Block Erase, Byte Write and Lock Bit Configuration	-2.0 V	14.0 V	2, 3
$\overline{RP}$ Voltage	With respect to GND during Lock Bit Configuration Operations	-2.0 V	14.0 V	2, 3
Output Short Circuit Current			100 mA	4

NOTES:
1. 'Operating temperature' is for the commercial temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5 V on input/output pins and -0.2 V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
3. Maximum DC voltage on V_{PP} and $\overline{RP}$ may overshoot to +14.0 V for periods < 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

CAUTION

Stressing the device beyond the 'Absolute Maximum Ratings' may cause permanent damage. These are stress ratings only. Operation beyond the 'Operating Conditions' is not recommended and extended exposure beyond the 'Operating Conditions' may affect device reliability.

OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
T_A	Operating Temperature	Ambient Temperature	0	+70°	C
V_{CC1}	V_{CC} Supply Voltage (2.7 V to 3.6 V)		2.70	3.60	V
V_{CC2}	V_{CC} Supply Voltage (3.3 V ±0.3 V)*		3.00	3.60	V
V_{CC3}	V_{CC} Supply Voltage (5.0 V ±0.25 V)		4.75	5.25	V
V_{CC4}	V_{CC} Supply Voltage (5.0 V ±0.50 V)		4.50	5.50	V

NOTE: *Block erase, byte write and lock-bit configuration operations with V_{CC} < 3.0 V should not be attempted.

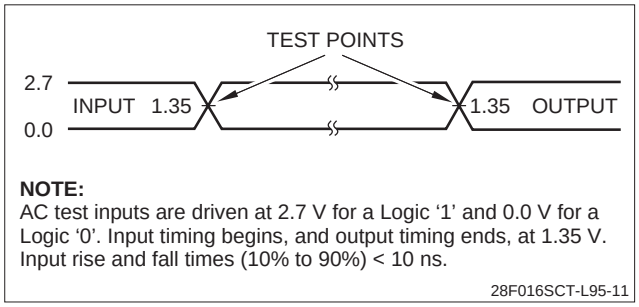
CAPACITANCE

T_A = +25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITION	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0.0 V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0.0 V	8	12	pF

NOTE: Sampled, not 100% tested.

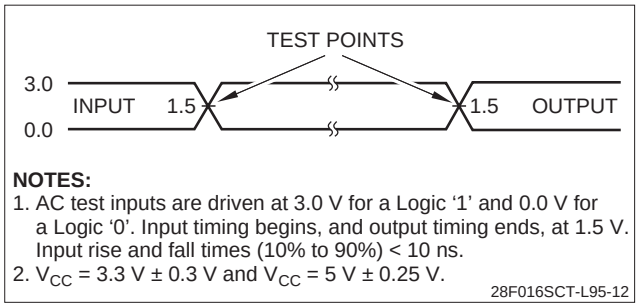
AC Input/Output Test Conditions



NOTE:
AC test inputs are driven at 2.7 V for a Logic '1' and 0.0 V for a Logic '0'. Input timing begins, and output timing ends, at 1.35 V. Input rise and fall times (10% to 90%) < 10 ns.

28F016SCT-L95-11

Figure 11. Transient Input/Output Reference Waveform for V_{CC} = 2.7 V - 3.6 V



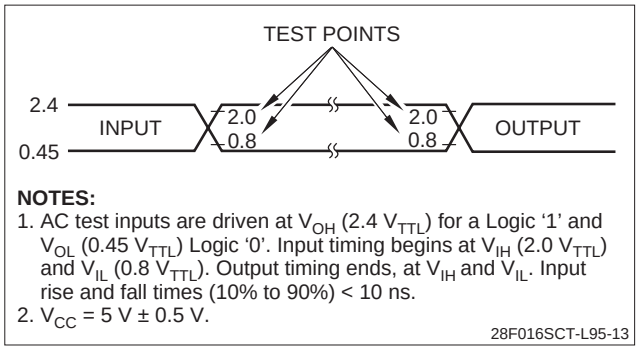
NOTES:
1. AC test inputs are driven at 3.0 V for a Logic '1' and 0.0 V for a Logic '0'. Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) < 10 ns.
2. V_{CC} = 3.3 V ± 0.3 V and V_{CC} = 5 V ± 0.25 V.

28F016SCT-L95-12

Figure 12. Transient Input/Output Reference Waveform (High Speed Testing Configuration)

Table 8. Test Configuration

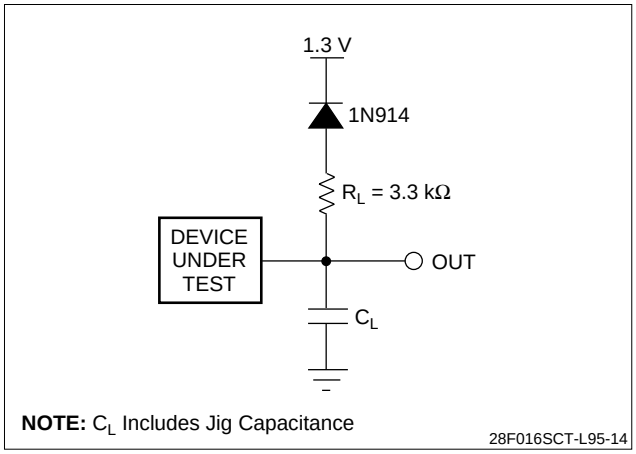
PARAMETER	VALUE
V_{CC} = 3.3 V ±0.3 V, 2.7 V - 3.6 V	50 C_L (pF)
V_{CC} = 5 V ±0.25 V	30 C_L (pF)
V_{CC} = 5 V ±0.50 V	30 C_L (pF)



NOTES:
1. AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic '1' and V_{OL} (0.45 V_{TTL}) Logic '0'. Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends, at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) < 10 ns.
2. V_{CC} = 5 V ± 0.5 V.

28F016SCT-L95-13

Figure 13. Transient Input/Output Reference Waveform (Standard Speed Testing Configuration)



NOTE: C_L Includes Jig Capacitance

28F016SCT-L95-14

Figure 14. Transient Equivalent Testing Load Circuit

Table 9. DC Characteristics

SYMBOL	PARAMETER	V_{CC} = 2.7 V		V_{CC} = 3.3 V		V_{CC} = 5 V		UNIT	TEST CONDITIONS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
I_{LI}	Input Load Current		±0.5		±0.5		±1	µA	$V_{CC} = V_{CC}$ MAX., $V_{IN} = V_{CC}$ or GND	1
I_{LO}	Output Leakage Current		±0.5		±0.5		±10	µA	$V_{CC} = V_{CC}$ MAX., $V_{OUT} = V_{CC}$ or GND	1
I_{CCS}	V_{CC} Standby Current	20	100	20	100	25	100	µA	CMOS Inputs $V_{CC} = V_{CC}$ MAX., $\overline{CE} = \overline{RP} = V_{CC}$ ±0.2 V	1, 3, 6
		0.1	2	0.2	2	0.4	2	mA	TTL Level Inputs $V_{CC} = V_{CC}$ MAX., $\overline{CE} = \overline{RP} = V_{IH}$	
I_{CCD}	V_{CC} Deep Power-Down Current		20		20		20	µA	$\overline{RP}$ = GND = ±0.2 V, I_{OUT} (RY/$\overline{BY}$) = 0 mA	1
I_{CCR}	V_{CC} Read Current	6	12	7	12	17	35	mA	CMOS Inputs $V_{CC} = V_{CC}$ MAX.,$\overline{CE}$ = GND f = 5 MHz, (3.3 V, 2.7 V), 8 MHz (5 V) I_{OUT} = 0 mA	1, 5, 6
		7	18	8	18	20	50	mA	TTL Inputs $V_{CC} = V_{CC}$ MAX., $\overline{CE}$ = GND f = 5 MHz (3.3 V, 2.7 V), 8 MHz (5 V) I_{OUT} = 0 mA	
I_{CCW}	V_{CC} Byte Write or Set Lock Bit Current				17			mA	V_{PP} = 3.3 V ±0.3 V	1, 7
					17		35	mA	V_{PP} = 5.0 V ±0.5 V	
					12		30	mA	V_{PP} = 12.0 V ±0.6 V	
I_{CCE}	V_{CC} Block Erase or Clear Block Lock Bits Current				17			mA	V_{PP} = 3.3 V ±0.3 V	1, 7
					17		30	mA	V_{PP} = 5.0 V ±0.5 V	
					12		25	mA	V_{PP} = 12.0 V ±0.6 V	
I_{CCWS} I_{CCES}	V_{CC} Byte Write or Block Erase Suspend Current			1	6	1	10	mA	$\overline{CE} = V_{IH}$	1, 2
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	±2	±15	±2	±15	±2	±15	µA	$V_{PP} \leq V_{CC}$	1
		10	200	10	200	10	200	µA	$V_{PP} > V_{CC}$	
I_{PPD}	V_{PP} Deep Power-Down Current	0.1	5	0.1	5	0.1	5	µA	$\overline{RP}$ = GND ±0.2 V	1
I_{PPW}	V_{PP} Byte Write or Set Lock Bit Current				40			mA	V_{PP} = 3.3 V ±0.3 V	1, 7
					40		40	mA	V_{PP} = 5.0 V ±0.5 V	
					15		15	mA	V_{PP} = 12.0 V ±0.6 V	
I_{PPE}	V_{PP} Block Erase or Clear Lock-Bit Current				20			mA	V_{PP} = 3.3 V ±0.3 V	1, 7
					20		20	mA	V_{PP} = 5.0 V ±0.5 V	
					15		15	mA	V_{PP} = 12.0 V ±0.6 V	
I_{PPWS} I_{PPES}	V_{PP} Byte Write or Block Erase Suspend Current			10	200	10	200	µA	$V_{PP} = V_{PPH1/2/3}$	1

Table 9. DC Characteristics (Cont'd)

SYMBOL	PARAMETER	V_{CC} = 2.7 V		V_{CC} = 3.3 V		V_{CC} = 5 V		UNIT	TEST CONDITIONS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
V_{IL}	Input LOW Voltage	-0.5	0.8	-0.5	0.8	-0.5	0.8	V		7
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	V		7
V_{OL}	Output LOW Voltage		0.4		0.4		0.45	V	V_{CC} = V_{CC} MIN., I_{OL} = 5.8 mA (V_{CC} = 5 V) I_{OL} = 2.0 mA (V_{CC} = 3.3 V, 2.7 V)	3, 7
V_{OH1}	Output HIGH Voltage (TTL)	2.4		2.4		2.4		V	V_{CC} = V_{CC} MIN., I_{OH} = -2.5 mA (V_{CC} = 5 V), I_{OH} = -2.0 mA (V_{CC} = 3.3 V), I_{OH} = -1.5 mA (V_{CC} = 2.7 V)	3, 7
V_{OH2}	Output HIGH Voltage (CMOS)	0.85 V_{CC}		0.85 V_{CC}		0.85 V_{CC}		V	V_{CC} = V_{CC} MIN., I_{OH} = -2.0 mA	3, 7
		V_{CC} -0.4		V_{CC} -0.4		V_{CC} ±0.4		V	V_{CC} = V_{CC} MIN., I_{OH} = -100 µA	
V_{PPLK}	V_{PP} Lockout during Normal Operations		1.5		1.5		1.5	V		4, 7
V_{PPH1}	V_{PP} during Byte Write, Block Erase or Lock Bit Operations			3.0	3.6			V		
V_{PPH2}	V_{PP} during Byte Write, Block Erase or Lock Bit Operations			4.5	5.5	4.5	5.5	V		
V_{PPH3}	V_{PP} during Byte Write, Block Erase or Lock Bit Operations			11.4	12.6	11.4	12.6	V		
V_{LKO}	V_{CC} Lockout Voltage	2.0		2.0		2.0		V		
V_{HH}	$\overline{RP}$ Unlock Voltage			11.4	12.6	11.4	12.6	V	Set master lock bit; override master and block lock bit	8, 9

NOTES:

1. All current values are RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A = +25°C.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word/byte codes are written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/$\overline{BY}$.
4. Block erases, byte writes and lock bit configurations are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (MAX.) and V_{PPH1} (MIN.), between V_{PPH1} (MAX.) and V_{PPH2} (MIN.), between V_{PPH2} (MAX.) and V_{PPH3} (MIN.) and above V_{PPH3} (MAX.).
5. The Automatic Power Savings (APS) reduces typical I_{CCR} to 1 mA at 5 V V_{CC} and 3 mA at 2.7 V and 3.3 V V_{CC} in static operation.
6. CMOS inputs are either V_{CC} ±0.2 V or GND ±0.2 V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. Master lock bit set operations are inhibited when $\overline{RP}$ = V_{IH}. Block lock bit configuration operations are inhibited when the master lock bit is set and $\overline{RP}$ = V_{IH}. Block erases and byte writes are inhibited when the corresponding block lock bit is set and $\overline{RP}$ = V_{IH}. Block erase, byte write, and lock bit configuration operations are not guaranteed with V_{CC} < 3.0 V or V_{IH} < $\overline{RP}$ < V_{HH} and should not be attempted.
9. RP connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.

AC CHARACTERISTICS — READ ONLY OPERATIONS(4)

V_{CC} = 2.7 V - 3.6 V, T_A = 0°C to +70°C (L150) V_{CC} = 3.3 V ±0.3 V, T_A = 0°C to +70°C (L120)

SYMBOL	PARAMETER	LH28F016SC-L150			LH28F016SC-L120			NOTES
		MIN.	MAX.	UNIT	MIN.	MAX.	UNIT	
t_{AVAV}	Read Cycle Time	150		ns	120		ns	
t_{AVQV}	Address to Output Delay		150	ns		120	ns	
t_{ELQV}	$\overline{CE}$ to Output Delay		150	ns		120	ns	1
t_{PHQV}	$\overline{RP}$ HIGH to Output Delay		600	ns		600	ns	
t_{GLQV}	$\overline{OE}$ to Output Delay		50	ns		50	ns	1
t_{ELQX}	$\overline{CE}$ to Output in Low-Z	0		ns	0		ns	2
t_{EHQZ}	$\overline{CE}$ HIGH to Output in High-Z		55	ns		55	ns	2
t_{GLQX}	$\overline{OE}$ to Output in Low-Z	0		ns	0		ns	2
t_{GHQZ}	$\overline{OE}$ HIGH to Output in High-Z		20	ns		20	ns	2
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change, Whichever Occurs First	0		ns	0		ns	2

NOTES:
1. $\overline{OE}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{CE}$ without impact on t_{ELQV}.
2. Sampled, not 100% tested.
3. $\overline{BYTE}$ mode reads will affect these timings.
4. See 'AC Input/Output Reference Waveforms' for maximum allowable input slew rate.

V_{CC} = 5 V ±0.5 V, 5 V ±0.25 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	LH28F016SC-L95			LH28F016SC-L100			NOTES
		MIN.	MAX.	UNIT	MIN.	MAX.	UNIT	
t_{AVAV}	Read Cycle Time	95		ns	100		ns	
t_{AVQV}	Address to Output Delay		95	ns		100	ns	
t_{ELQV}	$\overline{CE}$ to Output Delay		95	ns		100	ns	1
t_{PHQV}	$\overline{RP}$ HIGH to Output Delay		400	ns		400	ns	
t_{GLQV}	$\overline{OE}$ to Output Delay		40	ns		45	ns	1
t_{ELQX}	$\overline{CE}$ to Output in Low-Z	0		ns	0		ns	2
t_{EHQZ}	$\overline{CE}$ HIGH to Output in High-Z		55	ns		55	ns	2
t_{GLQX}	$\overline{OE}$ to Output in Low-Z	0		ns	0		ns	2
t_{GHQZ}	$\overline{OE}$ HIGH to Output in High-Z		10	ns		10	ns	2
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change, Whichever Occurs First	0		ns	0		ns	2

NOTES:
1. $\overline{OE}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{CE}$ without impact on t_{ELQV}.
2. Sampled, not 100% tested.
3. $\overline{BYTE}$ mode reads will affect these timings.
4. See 'AC Input/Output Reference Waveforms' for maximum allowable input slew rate.

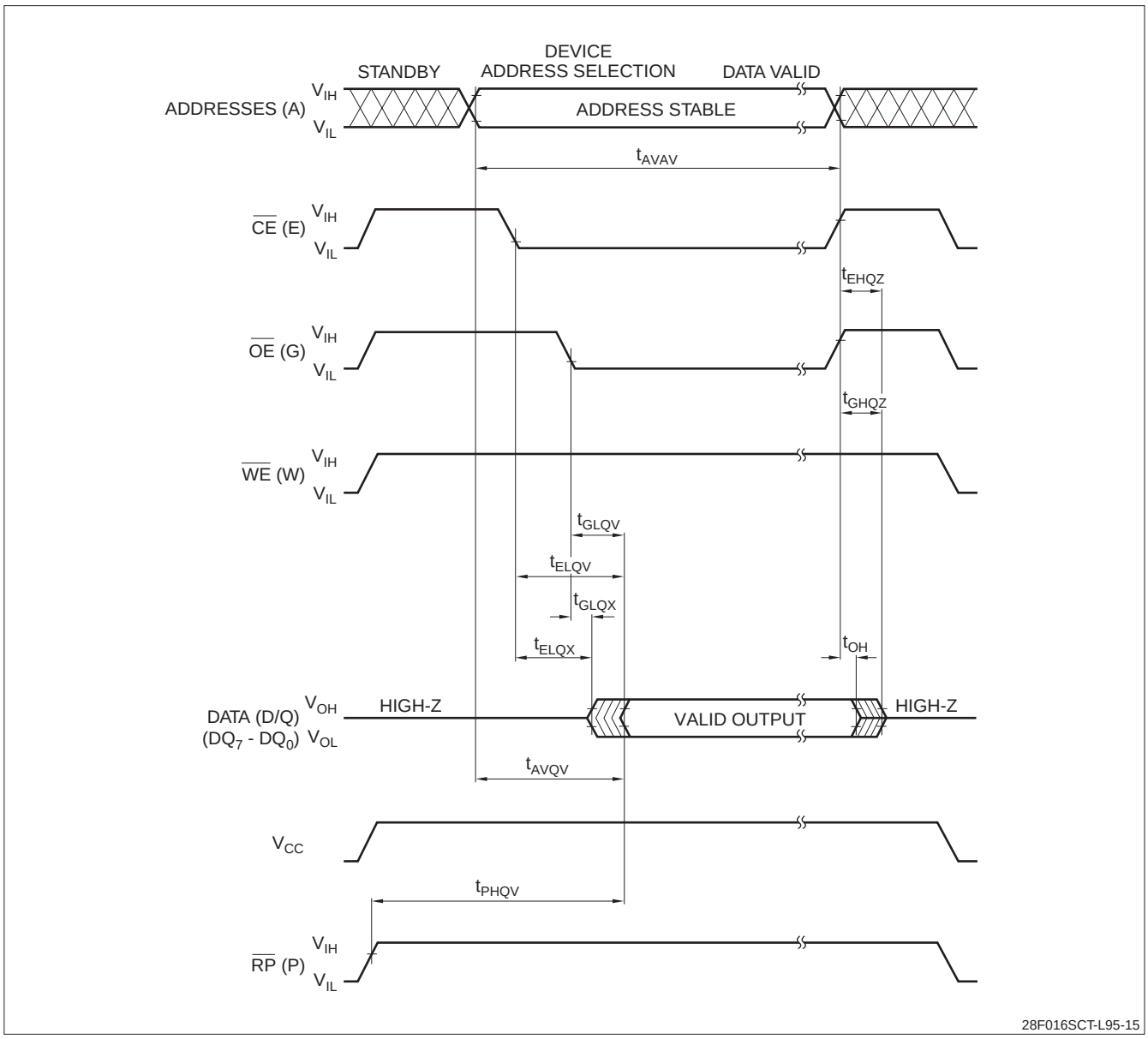


Figure 15. AC Waveforms for Read Operations

AC Characteristics

WRITE OPERATIONS

V_{CC} = 2.7 V - 3.6 V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	LH28F016SC-L150		UNIT	NOTES
		MIN.	MAX.		
t_{AVAV}	Write Cycle Time	150		ns	
t_{PHWL}	$\overline{RP}$ HIGH Recovery to $\overline{WE}$ Going LOW	1		µs	1
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going LOW	0		ns	
t_{WLWH}	$\overline{WE}$ Pulse Width	70		ns	
t_{AVWH}	Address Setup to $\overline{WE}$ Going HIGH	50		ns	2
t_{DVWH}	Data Setup to $\overline{WE}$ Going HIGH	50		ns	2
t_{WHDX}	Data Hold from $\overline{WE}$ HIGH	5		ns	
t_{WHAX}	Address Hold from $\overline{WE}$ HIGH	5		ns	
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ HIGH	0		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width HIGH	25		ns	
t_{WHGL}	Write Recovery Before Read	0		ns	

NOTES:

1. Sampled, not 100% tested.
2. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase byte write or lock bit configuration.
3. V_{PP} should be held at $V_{PPH1/2/3}$, (and if necessary, $\overline{RP}$ should be held at V_{HH}) until determination of block erase, full chip erase, (multi) word/byte write or lock bit configuration success (SR.1, SR.3, SR.4, SR.5 = 0).
4. Read timing characteristics during block erase, full chip erase, word/byte write and lock bit configuration operations are the same as during read-only operations. Refer to 'AC Characteristics' for read-only operations.

V_{CC} = 3.3 V ±0.3 V, T_A = -40°C to +85°C

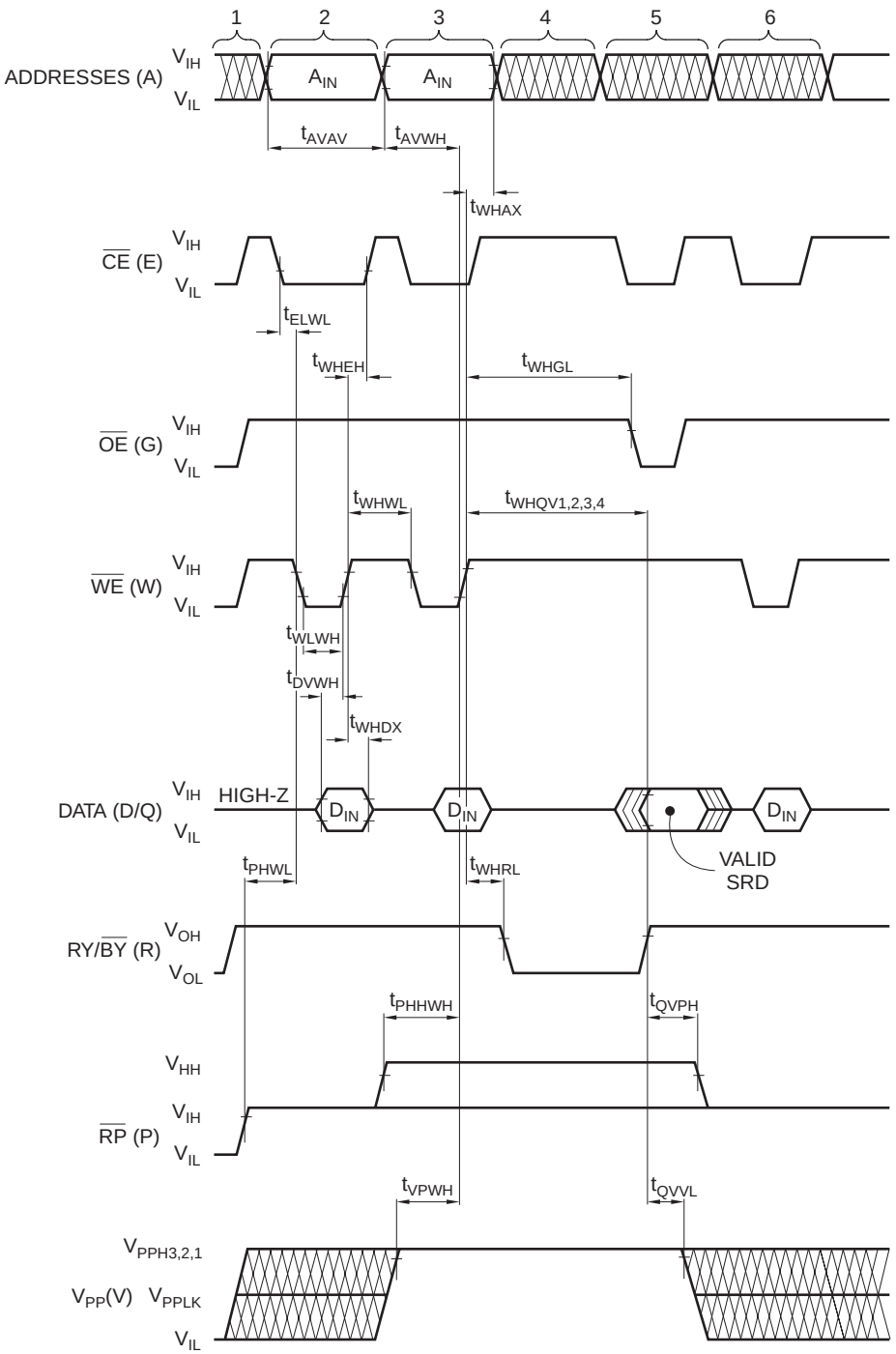
SYMBOL	PARAMETER	LH28F016SC-L120		UNIT	NOTES
		MIN.	MAX.		
t_{AVAV}	Write Cycle Time	120		ns	
t_{PHWL}	$\overline{RP}$ HIGH Recovery to $\overline{WE}$ Going LOW	1		µs	1
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going LOW	0		ns	
t_{WLWH}	$\overline{WE}$ Pulse Width	70		ns	
t_{PHHWH}	$\overline{RP}$ V_{HH} Setup to $\overline{WE}$ Going HIGH	100			
t_{VPWH}	V_{CCW} Setup to $\overline{WE}$ Going HIGH	100		ns	1
t_{AVWH}	Address Setup to $\overline{WE}$ Going HIGH	50		ns	2
t_{DVWH}	Data Setup to $\overline{WE}$ Going HIGH	50		ns	2
t_{WHDX}	Data Hold from $\overline{WE}$ HIGH	5		ns	
t_{WHAX}	Address Hold from $\overline{WE}$ HIGH	5		ns	
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ HIGH	0		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width HIGH	25		ns	
t_{WHRL}	$\overline{WE}$ High to RY/$\overline{BY}$ Going LOW or SR.7 Going '0'		100	ns	
t_{WHGL}	Write Recovery before Read	0		ns	
t_{QVVL}	V_{CCW} Hold from Valid SRD, RY/$\overline{BY}$ High-Z	0		ns	1, 3
t_{QVPH}	$\overline{WP}$ V_{IH} Hold from Valid SRD, RY/$\overline{BY}$ High-Z	0		ns	1, 3

NOTES:
1. Sampled, not 100% tested.
2. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase byte write or lock bit configuration.
3. V_{PP} should be held at $V_{PPH1/2/3}$, (and if necessary, $\overline{RP}$ should be held at V_{HH}) until determination of block erase, full chip erase, (multi) word/byte write or lock bit configuration success (SR.1, SR.3, SR.4, SR.5 = 0).
4. Read timing characteristics during block erase, full chip erase, word/byte write and lock bit configuration operations are the same as during read-only operations. Refer to 'AC Characteristics' for read-only operations.

V_{CC} = 5 V ±0.5 V (L100), 5 V ±0.25 V (L95), T_A = -40°C to +85°C

SYMBOL	PARAMETER	LH28F016SC-L95		LH28F016SC-L100		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time	95		100		ns	
t_{PHWL}	$\overline{RP}$ HIGH Recovery to $\overline{WE}$ Going LOW	1		1		µs	1
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going LOW	0		0		ns	
t_{WLWH}	$\overline{WE}$ Pulse Width	50		50		ns	
t_{PHHWH}	$\overline{RP}$ V_{HH} Setup to $\overline{WE}$ Going HIGH	100		100			
t_{VPWH}	V_{CCW} Setup to $\overline{WE}$ Going HIGH	100		100		ns	1
t_{AVWH}	Address Setup to $\overline{WE}$ Going HIGH	40		40		ns	2
t_{DVWH}	Data Setup to $\overline{WE}$ Going HIGH	40		40		ns	2
t_{WHDX}	Data Hold from $\overline{WE}$ HIGH	5		5		ns	
t_{WHAX}	Address Hold from $\overline{WE}$ HIGH	5		5		ns	
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ HIGH	0		0		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width HIGH	25		25		ns	
t_{WHRL}	$\overline{WE}$ High to RY/$\overline{BY}$ Going LOW or SR.7 Going ‘0’		90		90	ns	
t_{WHGL}	Write Recovery before Read	0		0		ns	
t_{QVVL}	V_{CCW} Hold from Valid SRD, RY/$\overline{BY}$ High-Z	0		0		ns	1, 3
t_{QVPH}	$\overline{WP}$ V_{IH} Hold from Valid SRD, RY/$\overline{BY}$ High-Z	0		0		ns	1, 3

NOTES:
1. Sampled, not 100% tested.
2. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase byte write or lock bit configuration.
3. V_{PP} should be held at $V_{PPH1/2/3}$, (and if necessary, $\overline{RP}$ should be held at V_{HH}) until determination of block erase, full chip erase, (multi) word/byte write or lock bit configuration success (SR.1, SR.3, SR.4, SR.5 = 0).
4. Read timing characteristics during block erase, full chip erase, word/byte write and lock bit configuration operations are the same as during read-only operations. Refer to ‘AC Characteristics’ for read-only operations.



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

28F016SCT-L95-16

Figure 16. AC Waveforms for $\overline{WE}$-Controlled Write Operations

ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES

V_{CC} = 2.7 V - 3.6 V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	LH28F016SC-L150		UNIT	NOTES
		MIN.	MAX.		
t_{AVAV}	Write Cycle Time	150		ns	
t_{PHEL}	$\overline{RP}$ HIGH Recovery to $\overline{CE}$ Going LOW	1		µs	1
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going LOW	0		ns	
t_{ELEH}	$\overline{CE}$ Pulse Width	70		ns	
t_{AVEH}	Address Setup to $\overline{CE}$ Going HIGH	50		ns	2
t_{DVEH}	Data Setup to $\overline{CE}$ Going HIGH	50		ns	2
t_{EHDX}	Data Hold from $\overline{CE}$ HIGH	5		ns	
t_{EHAX}	Address Hold from $\overline{CE}$ HIGH	5		ns	
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ HIGH	0		ns	
t_{EHEL}	$\overline{CE}$ Pulse Width HIGH	25		ns	
t_{EHGL}	Write Recovery before Read	0		ns	

NOTES:
1. Sampled, not 100% tested.
2. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, byte write or lock bit configuration.
3. V_{CCW} should be held at $V_{PPH1/2/3}$, (and if necessary, $\overline{RP}$ should be held at V_{HH}) until determination of block erase, byte write or lock bit configuration success (SR.1, SR.3, SR.4, SR.5 = 0).
4. In systems where $\overline{CE}$ defines the write pulse width (within a longer $\overline{WE}$ timing waveform), all setup, hold, and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.

V_{CC} = 3.3 V ±0.3 V, T_A = -40°C to +85°C

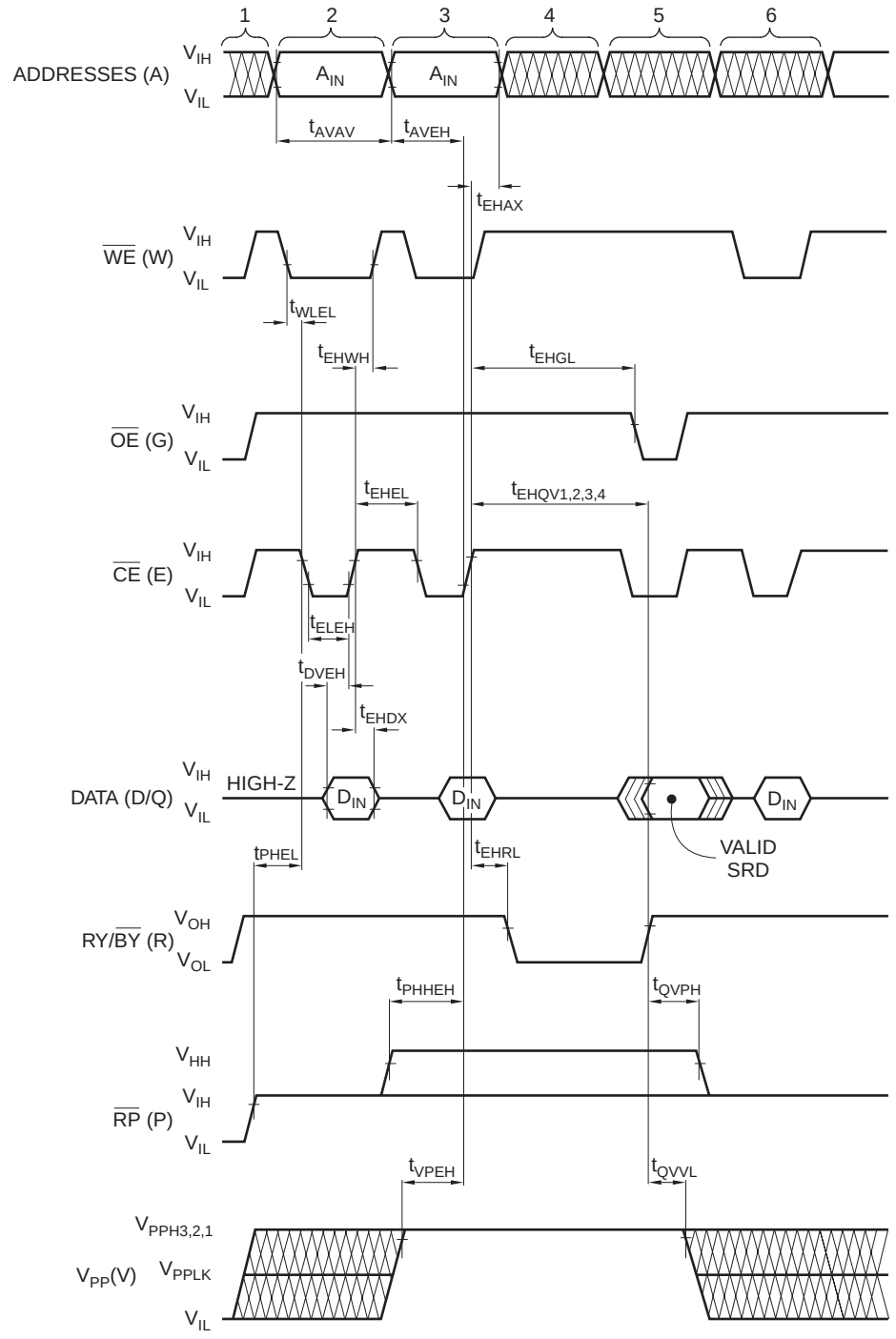
SYMBOL	PARAMETER	LH28F016SC-L120		UNIT	NOTES
		MIN.	MAX.		
t_{AVAV}	Write Cycle Time	120		ns	
t_{PHEL}	$\overline{RP}$ HIGH Recovery to $\overline{CE}$ Going LOW	1		µs	1
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going LOW	0		ns	
t_{ELEH}	$\overline{CE}$ Pulse Width	70		ns	
t_{PHHEH}	$\overline{RP}$ V_{HH} Setup to $\overline{CE}$ Going HIGH	100		ns	
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going HIGH	100		ns	
t_{AVEH}	Address Setup to $\overline{CE}$ Going HIGH	50		ns	2
t_{DVEH}	Data Setup to $\overline{CE}$ Going HIGH	50		ns	2
t_{EHDX}	Data Hold from $\overline{CE}$ HIGH	5		ns	
t_{EHAX}	Address Hold from $\overline{CE}$ HIGH	5		ns	
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ HIGH	0		ns	
t_{EHEL}	$\overline{CE}$ Pulse Width HIGH	25		ns	
t_{EHRL}	$\overline{CE}$ HIGH to RY/$\overline{BY}$ Going LOW		100	ns	
t_{EHGL}	Write Recovery before Read	0		ns	
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/$\overline{BY}$ HIGH	0		ns	
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD, RY/$\overline{BY}$ HIGH	0		ns	

NOTES:
1. Sampled, not 100% tested.
2. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, byte write or lock bit configuration.
3. V_{CCW} should be held at $V_{PPH1/2/3}$, (and if necessary, $\overline{RP}$ should be held at V_{HH}) until determination of block erase, byte write or lock bit configuration success (SR.1, SR.3, SR.4, SR.5 = 0).
4. In systems where $\overline{CE}$ defines the write pulse width (within a longer $\overline{WE}$ timing waveform), all setup, hold, and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.

V_{CC} = 5 V ±0.5 V (L100), 5 V ±0.25 V (L95), T_A = -40°C to +85°C

SYMBOL	PARAMETER	LH28F016SC-L95		LH28F016SC-L100		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time	95		100		ns	
t_{PHEL}	$\overline{RP}$ HIGH Recovery to $\overline{CE}$ Going LOW	1		1		µs	1
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going LOW	0		0		ns	
t_{ELEH}	$\overline{CE}$ Pulse Width	50		50		ns	
t_{PHHEH}	$\overline{RP}$ V_{HH} Setup to $\overline{CE}$ Going HIGH	100		100		ns	1
t_{VPEH}	V_{CCW} Setup to $\overline{CE}$ Going HIGH	100		100		ns	1
t_{AVEH}	Address Setup to $\overline{CE}$ Going HIGH	40		40		ns	2
t_{DVEH}	Data Setup to $\overline{CE}$ Going HIGH	40		40		ns	2
t_{EHDX}	Data Hold from $\overline{CE}$ HIGH	5		5		ns	
t_{EHAX}	Address Hold from $\overline{CE}$ HIGH	5		5		ns	
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ HIGH	0		0		ns	
t_{EHEL}	$\overline{CE}$ Pulse Width HIGH	25		25		ns	
t_{EHRL}	$\overline{CE}$ HIGH to RY/$\overline{BY}$ Going LOW		90		90	ns	
t_{EHGL}	Write Recovery before Read	0		0		ns	
t_{QVVL}	V_{CCW} Hold from Valid SRD, RY/$\overline{BY}$ HIGH	0		0		ns	1, 3
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD, RY/$\overline{BY}$ HIGH	0		0		ns	1, 3

NOTES:
1. Sampled, not 100% tested.
2. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, byte write or lock bit configuration.
3. V_{CCW} should be held at $V_{PPH1/2/3}$, (and if necessary, $\overline{RP}$ should be held at V_{HH}) until determination of block erase, byte write or lock bit configuration success (SR.1, SR.3, SR.4, SR.5 = 0).
4. In systems where $\overline{CE}$ defines the write pulse width (within a longer $\overline{WE}$ timing waveform), all setup, hold, and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

28F016SCT-L95-17

Figure 17. AC Waveforms for $\overline{CE}$-controlled Write Operations

RESET OPERATIONS

Table 10. Reset AC Specifications

SYMBOL	PARAMETER	V_{CC} = 2.7 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{PLPH}	$\overline{RP}$ Pulse LOW Time	100		100		100		ns	1
t_{PLRH}	$\overline{RP}$ LOW to Reset during Block Erase, Byte Write or Lock bit Configuration				20		12	µs	2, 3
t_{235VPH}	V_{CC} 2.7 V to $\overline{RP}$ HIGH V_{CC} 3.0 V to $\overline{RP}$ HIGH V_{CC} 4.5 V to $\overline{RP}$ HIGH	100		100		100		ns	2, 4

NOTES:
1. If $\overline{RP}$ is tied to V_{CC}, this specification does not apply.
2. An $\overline{RP}$ asserted reset will complete within 100 ns unless a block erase, lock bit, or chip erase operation is being performed.
3. A reset time, t_{PHQV}, is required from the later of RY/$\overline{BY}$ or $\overline{RP}$ going HIGH until outputs are valid.
4. When the device is powered up, holding $\overline{RP}$ LOW a minimum 100 ns is required after V_{CC} reaches nominal voltage and stabilizes.

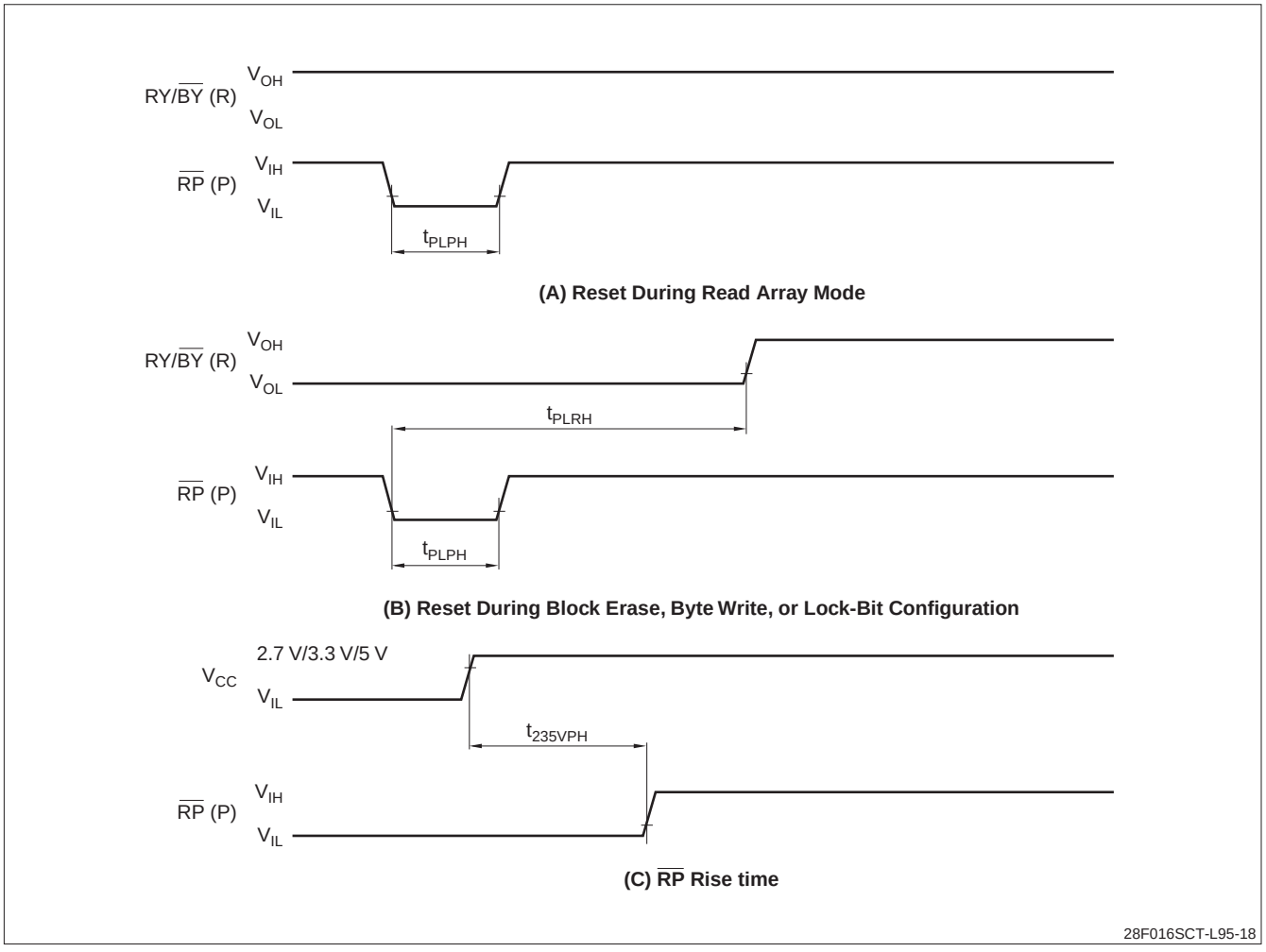


Figure 18. AC Waveform for Reset Operation

BLOCK ERASE, FULL CHIP ERASE, WORD/BYTE WRITE AND LOCK BIT CONFIGURATION PERFORMANCE

V_{CC} = 3.3 V ±0.3 V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	V_{PP} = 3.3 V		V_{PP} = 5 V		V_{PP} = 12 V		UNIT	NOTES
		TYP.	MAX.	TYP.	MAX.	TYP.	MAX.		
t_{WHQV1}, t_{EHQV1}	Byte Write Time	19	300	10	150	7	125	µs	1
	Block Write Time	1.2	4	0.7	2	0.5	1.5	s	1
t_{WHQV2}, t_{EHQV2}	Block Erase Time	0.8	6	0.4	5	0.3	4	s	1
t_{WHQV3}, t_{EHQV3}	Set Lock Bit Time	21	300	13.3	150	11.6	125	µs	1
t_{WHQV4}, t_{EHQV4}	Clear Block Lock Bits Time	1.8	6	1.2	5	1.1	4	s	1
t_{WHRH1}, t_{EHRH1}	Byte Write Suspend Latency Time to Read	7.1	10	6.6	9.3	7.4	10.4	µs	1
t_{WHRH2}, t_{EHRH2}	Erase Suspend Latency Time to Read	15.2	21.1	12.3	17.2	12.3	17.2	µs	1

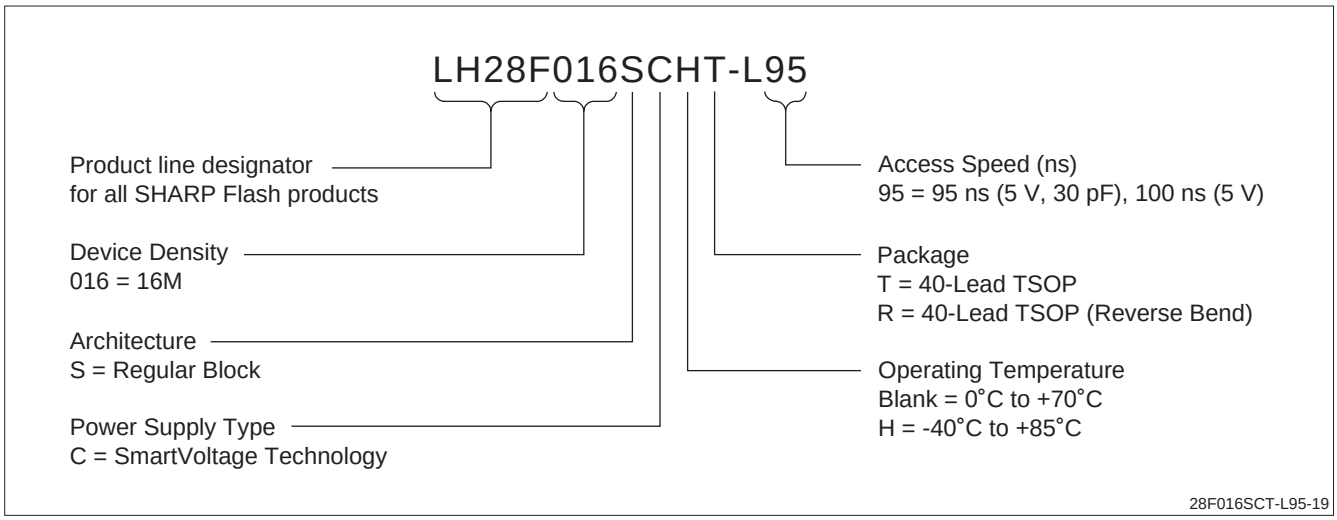
NOTES:
1. Excludes system-level overhead.
2. A latency time is required from issuing the suspend command ($\overline{WE}$ or $\overline{CE}$ going HIGH) until RY/$\overline{BY}$ going high-Z or SR.7 going HIGH.
3. Sampled but not 100% tested.
4. Typical values measured at T_A = +25°C and V_{CC} at nominal. Assumes corresponding lock bits are not set. Subject to change based on device characterization.

V_{CC} = 5 V ±0.5 V, 5 V ±0.25 V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	V_{PP} = 5 V		V_{PP} = 12 V		UNIT	NOTES
		TYP.	MAX.	TYP.	MAX.		
t_{WHQV1}, t_{EHQV1}	Byte Write Time	8	150	6	100	µs	1
	Block Write Time	0.5	1.5	0.4	1	s	1
t_{WHQV2}, t_{EHQV2}	Block Erase Time	0.4	5	0.3	4	s	1
t_{WHQV3}, t_{EHQV3}	Set Lock-Bit Time	12	150	10	100	µs	1
t_{WHQV4}, t_{EHQV4}	Clear Block Lock-Bits Time	1.1	5	1	4	s	1
t_{WHRH1}, t_{EHRH1}	Byte Write Suspend Latency Time to Read	5.6	7	5.2	7.5	µs	1
t_{WHRH2}, t_{EHRH2}	Erase Suspend Latency Time to Read	9.4	13.1	9.8	12.6	s	1

NOTES:
1. Excludes system-level overhead.
2. A latency time is required from issuing the suspend command ($\overline{WE}$ or $\overline{CE}$ going HIGH) until RY/$\overline{BY}$ going high-Z or SR.7 going HIGH.
3. Sampled but not 100% tested.
4. Typical values measured at T_A = +25°C and V_{CC} at nominal. Assumes corresponding lock bits are not set. Subject to change based on device characterization.

ORDERING INFORMATION



SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

Suggested applications (if any) are for standard use; See Important Restrictions for limitations on special applications. See Limited Warranty for SHARP's product warranty. The Limited Warranty is in lieu, and exclusive of, all other warranties, express or implied. ALL EXPRESS AND IMPLIED WARRANTIES, INCLUDING THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR USE AND FITNESS FOR A PARTICULAR PURPOSE, ARE SPECIFICALLY EXCLUDED. In no event will SHARP be liable, or in any way responsible, for any incidental or consequential economic or property damage.

SHARP®

NORTH AMERICA

SHARP Microelectronics of the Americas
5700 NW Pacific Rim Blvd.
Camas, WA 98607, U.S.A.
Phone: (1) 360-834-2500
Fax: (1) 360-834-8903
www.sharpsma.com

EUROPE

SHARP Microelectronics Europe
Division of Sharp Electronics (Europe) GmbH
Sonninstrasse 3
20097 Hamburg, Germany
Phone: (49) 40-2376-2286
Fax: (49) 40-2376-2232
www.sharpsme.com

JAPAN

SHARP Corporation
Electronic Components & Devices
22-22 Nagaike-cho, Abeno-Ku
Osaka 545-8522, Japan
Phone: (81) 6-6621-1221
Fax: (81) 6117-725300/6117-725301
www.sharp-world.com

TAIWAN

SHARP Electronic Components
(Taiwan) Corporation
8F-A, No. 16, Sec. 4, Nanking E. Rd.
Taipei, Taiwan, Republic of China
Phone: (886) 2-2577-7341
Fax: (886) 2-2577-7326/2-2577-7328

SINGAPORE

SHARP Electronics (Singapore) PTE., Ltd.
438A, Alexandra Road, #05-01/02
Alexandra Technopark,
Singapore 119967
Phone: (65) 271-3566
Fax: (65) 271-3855

KOREA

SHARP Electronic Components
(Korea) Corporation
RM 501 Geosung B/D, 541
Dohwa-dong, Mapo-ku
Seoul 121-701, Korea
Phone: (82) 2-711-5813 ~ 8
Fax: (82) 2-711-5819

CHINA

SHARP Microelectronics of China
(Shanghai) Co., Ltd.
28 Xin Jin Qiao Road King Tower 16F
Pudong Shanghai, 201206 P.R. China
Phone: (86) 21-5854-7710/21-5834-6056
Fax: (86) 21-5854-4340/21-5834-6057
Head Office:
No. 360, Bashen Road,
Xin Development Bldg. 22
Waigaoqiao Free Trade Zone Shanghai
200131 P.R. China
Email: smc@china.global.sharp.co.jp

HONG KONG

SHARP-ROXY (Hong Kong) Ltd.
3rd Business Division,
17/F, Admiralty Centre, Tower 1
18 Harcourt Road, Hong Kong
Phone: (852) 28229311
Fax: (852) 28660779
www.sharp.com.hk
Shenzhen Representative Office:
Room 13B1, Tower C,
Electronics Science & Technology Building
Shen Nan Zhong Road
Shenzhen, P.R. China
Phone: (86) 755-3273731
Fax: (86) 755-3273735