



## LH4118/LH4118A/LH4118C Low Gain Wide Band RF Amplifier

### General Description

The LH4118 is a wideband amplifier optimized for high speed, low gain applications. It is an ideal alternative to low precision amplifiers. It features a closed loop  $-3$  dB unity gain bandwidth in excess of 200 MHz. Unlike conventional op-amps, the bandwidth is relatively independent of closed loop gain between 1 and 5. A high current output stage is also incorporated, allowing the LH4118 to drive  $50\Omega$  terminated lines directly. It is an ideal choice for video distribution, flash converter input buffering and ATE pin driver.

### Features

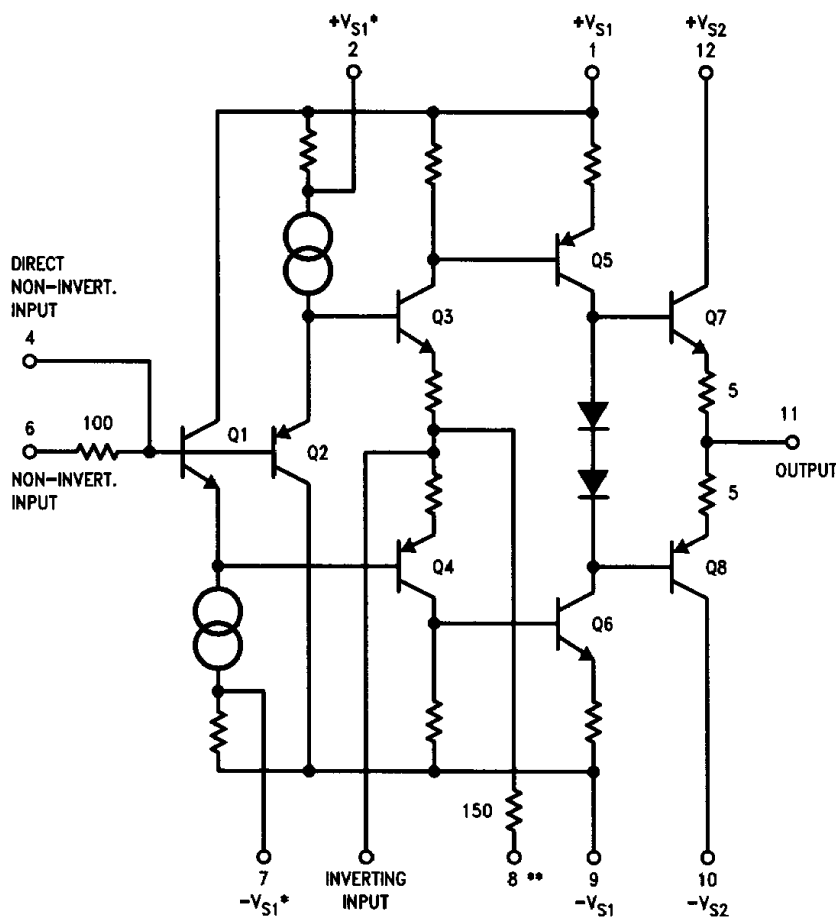
- 250 MHz bandwidth
- 15 ns settling time to 0.1%

- 2.5 ns rise and fall times
- Output current to 100 mA
- 2 mV offset voltage
- 2500 V/ $\mu$ s slew rate (100 $\Omega$  load)
- $\pm 0.5$  dB gain flatness (AV = 5)

### Applications

- Unity gain buffers
- Low gain op amp
- High speed peak detectors
- Video amplifier
- Flash converter driver

### Simplified Schematic



\*Pins 2 and 7 can also be left disconnected (floating)

\*\*The built-in 150 $\Omega$  can be used as feedback resistor for  $A_V = 1$ . For details see applications section.

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## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, $V_S$	$\pm 18V$
Power Dissipation, $P_D$ (See Graph)	1.65W
Output Current	125 mA
Non-Inverting Input Voltage Range, $V_{CM}$ (For $V_S \leq +15V$ ) (Note 1)	$\pm V_S$

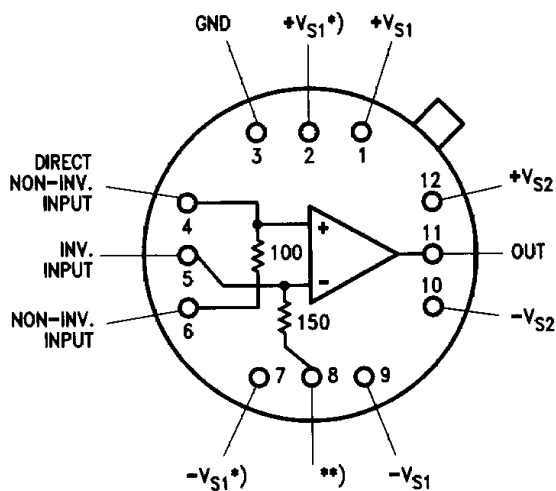
Operating Temperature Range, $T_A$	
LH4118CG	$-25^\circ\text{C}$ to $+85^\circ\text{C}$
LH4118G, LH4118AG	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Storage Temperature Range, $T_{STG}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Maximum Junction Temperature, $T_J$	$175^\circ\text{C}$
Lead Temperature (Soldering, < 10 sec.)	$300^\circ\text{C}$
ESD Tolerance (Note 2)	650V

## DC Electrical Characteristics

Unless otherwise noted,  $R_S = 50\Omega$ ,  $T_A = T_C = 25^\circ\text{C}$ ,  $V_S = \pm 15V$  (Notes 3, 4)

Symbol	Parameter	Conditions	LH4118AG			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 5)	Design Limit (Note 6)	
$V_{OS}$	Non-Inverting Input Offset Voltage	$V_{IN} = 0V$	$\pm 2$	$\pm 2$ $\pm 5$		mV
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage Drift		10			$\mu\text{V}/^\circ\text{C}$
$I_B$	Non-Inverting Input Bias Current		$\pm 5$	$\pm 25$ $\pm 30$		$\mu\text{A}$
$V_O$	Output Voltage Swing	$R_L = 500\Omega$	$\pm 13$	$\pm 11$ $\pm 10.5$		V (Min)
$V_O$	Output Voltage Swing	$R_L = \infty$	$\pm 14$	$\pm 12$ $\pm 11.5$		V (Min)
$I_O$	Output Current Swing	$R_L = 50\Omega$ (Note 7)		$\pm 100$		mA (Min)
CMRR	Common Mode Rejection Ratio	$V_{IN} = -11V$ to $+11V$ , $V_S = \pm 18V$	54	<b>50</b>		dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm V_S = 9V$ to $15V$ $\Delta V = 6V$	72	<b>62</b>		dB (Min)
$I_S$	Quiescent Supply Current	$V_{IN} = 0V$	20	<b>25</b>		mA
$P_D$	Quiescent Power Dissipation	(Note 7)	600	<b>750</b>		mW
$C_{IN}$	Input Capacitance		1.5			pF

## Connection Diagram



Top View

\*Pins 2 and 7 can also be left disconnected (floating)

\*\*The built-in 150 $\Omega$  can be used as feedback resistor for  $A_V = 1$ . For details see applications section.

Order Number LH4118G, LH4118AG or LH4118CG  
See NS Package Number H12B

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**DC Electrical Characteristics**Unless otherwise noted,  $R_S = 50\Omega$ ,  $T_A = T_C = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$  (Notes 3, 4)

Symbol	Parameter	Conditions	LH4118G			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 5)	Design Limit (Note 6)	
$V_{OS}$	Non-Inverting Input Offset Voltage	$V_{IN} = 0\text{V}$	$\pm 2$	$\pm 5$		mV
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage Drift		10			$\mu\text{V}/^\circ\text{C}$
$I_B$	Non-Inverting Input Bias Current		$\pm 5$	$\pm 25$ $\pm 30$		$\mu\text{A}$
$V_O$	Output Voltage Swing	$R_L = 500\Omega$	$\pm 13$	$\pm 11$ $\pm 10.5$		V (Min)
$V_O$	Output Voltage Swing	$R_L = \infty$	$\pm 14$	$\pm 12$ $\pm 11.5$		V (Min)
$I_O$	Output Current Swing	$R_L = 50\Omega$ (Note 7)		$\pm 100$		mA (Min)
CMRR	Common Mode Rejection Ratio	$V_{IN} = -11\text{V to } +11\text{V}$ , $V_S = \pm 18\text{V}$	54	<b>50</b>		dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm V_S = 9\text{V to } 15\text{V}$ $\Delta V = 6\text{V}$	72	<b>62</b>		dB (Min)
$I_S$	Quiescent Supply Current	$V_{IN} = 0\text{V}$	20	<b>25</b>		mA
$P_D$	Quiescent Power Dissipation	(Note 7)	600	<b>750</b>		mW
$C_{IN}$	Input Capacitance		1.5			pF

**DC Electrical Characteristics**Unless otherwise noted,  $R_S = 50\Omega$ ,  $T_A = T_C = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$  (Notes 3, 4)

Symbol	Parameter	Conditions	LH4118CG			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 5)	Design Limit (Note 6)	
$V_{OS}$	Non-Inverting Input Offset Voltage	$V_{IN} = 0\text{V}$	$\pm 2$	$\pm 5$	$\pm 5$	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage Drift		10			$\mu\text{V}/^\circ\text{C}$
$I_B$	Non-Inverting Input Bias Current		$\pm 5$	$\pm 25$	$\pm 30$	$\mu\text{A}$
$V_O$	Output Voltage Swing	$R_L = 500\Omega$	$\pm 13$	$\pm 11$	$\pm 10.5$	V
$V_O$	Output Voltage Swing	$R_L = \infty$	$\pm 14$	$\pm 12$	$\pm 11.5$	V (Min)
$I_O$	Output Current Swing	$R_L = 50\Omega$ (Note 7)		$\pm 100$	$\pm 100$	mA
CMRR	Common Mode Rejection Ratio	$V_{IN} = -11\text{V to } +11\text{V}$ , $V_S = \pm 18\text{V}$	54	50	<b>50</b>	dB
PSRR	Power Supply Rejection Ratio	$\pm V_S = 9\text{V to } 15\text{V}$ $\Delta V = 6\text{V}$	72	62	<b>62</b>	dB
$I_S$	Quiescent Supply Current	$V_{IN} = 0\text{V}$	20	25	<b>25</b>	mA
$P_D$	Quiescent Power Dissipation	(Note 7)	600	750	<b>750</b>	mW
$C_{IN}$	Input Capacitance		1.5			pF

## AC Electrical Characteristics

Unless otherwise noted,  $A_v = +2$ ,  $R_S = 50\Omega$ ,  $R_L = 100\Omega$ ,  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$

Symbol	Parameter	Conditions	LH4118CG, LH4118AG and LH4118G			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit	Design Limit	
SSBW -3 dB	Small Signal Bandwidth	$V_{OUT} = 0.2 V_{P-P}$	250	200		MHz (Min)
PBW -3 dB	Power Bandwidth	$V_{OUT} = 10 V_{P-P}$	68	55		MHz (Min)
GF	Gain Flatness	$V_{OUT} = 0.2 V_{P-P}$	0.5 MHz, -50 MHz	$\pm 0.3$		dB (Max)
			0.5 MHz, -100 MHz	-1.0		
SR	Slew Rate LH4118AG LH4118G LH4118CG	$V_{OUT} = 15 V_{P-P}$ 20%-80%		2400 2000 1800		V/ $\mu$ S (Min)
$t_r$	Rise Time	$V_{OUT} = 10 V_{P-P}$ 10%-90%	2.5			ns
$V_{GC}$	-1 dB Gain Compression	$f = 50$ MHz	23.5			dBm
$e_n$	Input Noise Voltage	$A_v = 5$ , $R_S = 50\Omega$ , $f = 10$ MHz	1.3			$nV/\sqrt{Hz}$
HD <sub>2</sub>	Second Harmonic Distortion	$V_{OC} = 1.27 V_{P-P}$ $F_C = 14$ MHz	-58			dBc
HD <sub>3</sub>	Third Harmonic Distortion	$V_{OC} = 1.27 V_{P-P}$ $F_C = 14$ MHz	-40			dBc
$t_s$	Settling Time	$A_v = -1$ $V_{IN} = +5 V_{P-P}$ to 0.1%	15			ns
LVBW -3 dB	Low Supply Voltage Bandwidth	$V_{OUT} = 0.2 V_{P-P}$ $V_S = \pm 5V$	230			MHz
LVSR	Low Supply Voltage Slew Rate	$V_S = \pm 5V$ , $V_{OUT} = 5 V_{P-P}$ 20%-80%	1400			V/ $\mu$ s
DG	Differential Gain	$V_{IN} = \pm 4 V_{DC}$ 0.4 $V_{P-P}$ AC $f = 4$ MHz	<0.01			dB
PL	Phase Linearity	$V_{IN} = \pm 4 V_{DC}$ 0.4 $V_{P-P}$ AC, $f = 4$ MHz	<0.1			DEG

**Note 1:** The input signal should be within the supply rails. Also, the input signal as well as the output signal should not be more than 30V from any supply voltage.

**Note 2:** The average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500 $\Omega$ .

**Note 3: Boldface** limits are guaranteed over full temperature range. Operating ambient temperature range of LH4118CG is  $-25^\circ C$  to  $+85^\circ C$ , for LH4118G and LH4118AG it is  $-55^\circ C$  to  $125^\circ C$ .

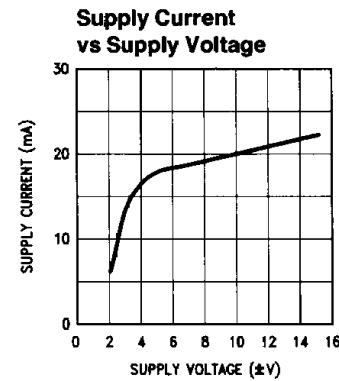
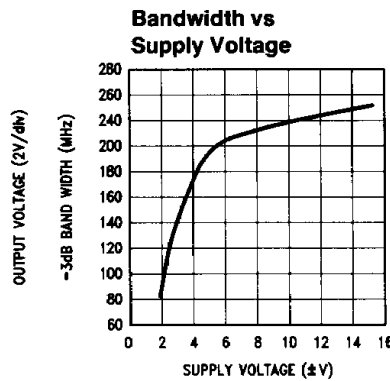
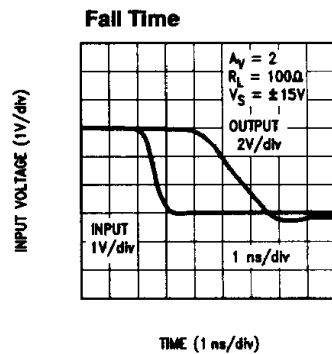
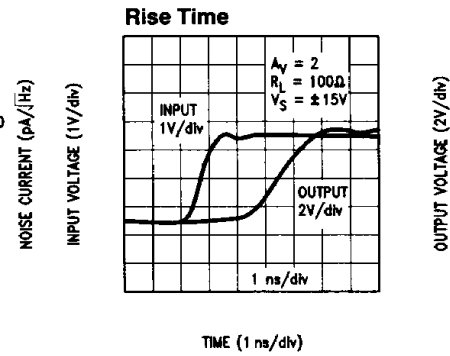
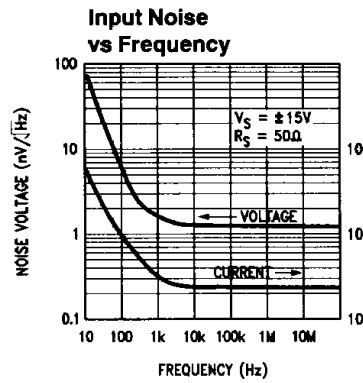
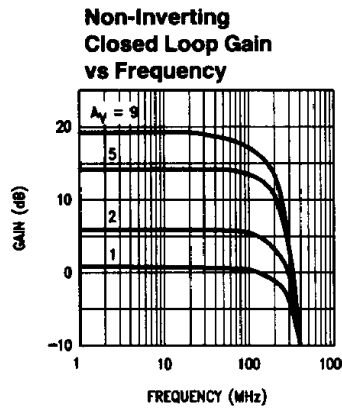
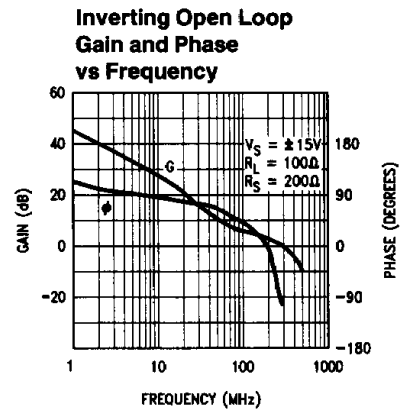
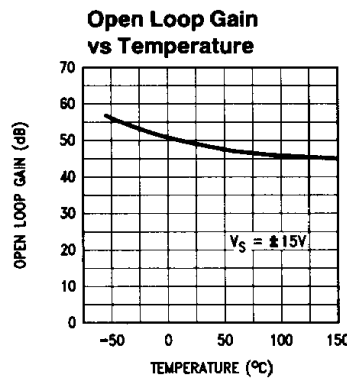
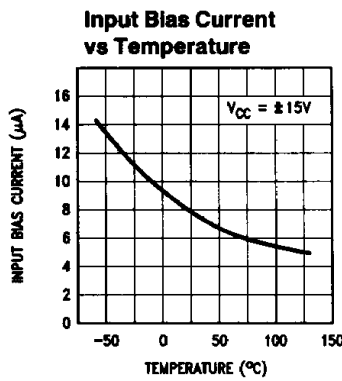
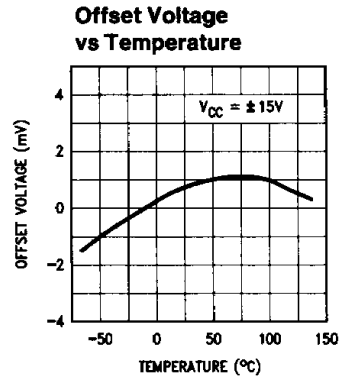
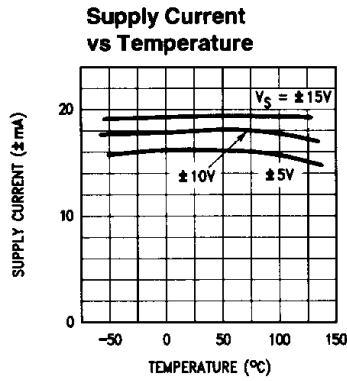
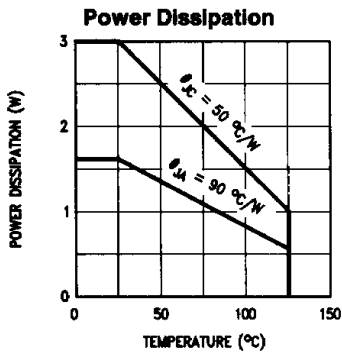
**Note 4:** Specifications are at  $25^\circ C$  junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at  $T_J = 25^\circ C$ .

**Note 5:** Tested limits are guaranteed and 100% production tested.

**Note 6:** Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

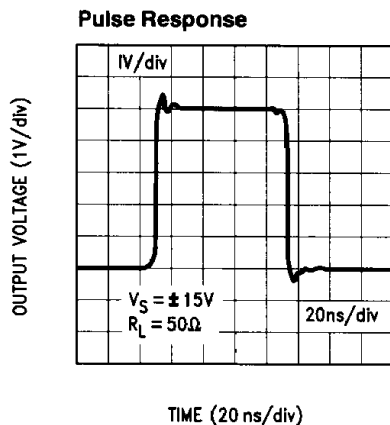
**Note 7:** When the LH4118 is operated at elevated temperature (such as  $125^\circ C$ ), some form of heat sinking or forced air cooling is required. The quiescent power with  $V_S = \pm 15V$  is 750 mW, whereas the package can only handle 550 mW without a heatsink at  $125^\circ C$ .

# Typical Performance Characteristics



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## Typical Performance Characteristics (Continued)



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## Applications Information

### LAYOUT

Breadboards should have a solid ground plane and short point-to-point wiring. Do not use wirewrap boards or techniques. PC boards should have short connections and as much ground plane as possible.

The inputs (Pins 4, 5 & 6) should have low capacitance and, therefore, the ground plane should be taken out around these pins. The body of  $R_G$  should be close to Pin 5 for the same reason.

It is best to have a layout without sockets, but sockets with short pins and receptacles do not degrade the performance much.

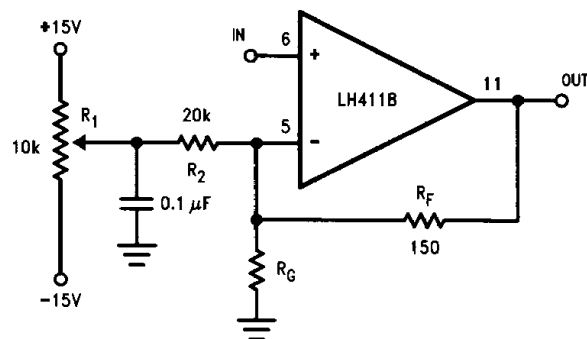
Input and output should be led by coax or microstrip if the distances are more than a few inches to avoid impedance shifts and resulting reflections.

Power supplies need to be bypassed with 0.01  $\mu F$  to 0.1  $\mu F$  as close as 0.15" to the pins and additional 1  $\mu F$  tantalum a maximum 1" distant. Please make sure that the return current from the ground end of  $R_L$  does not flow across the input: the grounding point of  $R_L$  should be close to the grounding points of the power supply bypass capacitors. On the LH4118, this comes almost natural because of the layout of the pins.

The direct non-inverting input on pin 4, if used, should not see impedances of less than 100 $\Omega$ .

The built-in feedback resistor (pin 8) is limited to a maximum dissipation of 150 mW. It can be used for unity gain and for higher gains at lower amplitudes.

### Input-to-Output Offset Zero Adjust



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This circuit lets the  $V_{OS}$  between non-inverting input (pin 6) and output (pin 11) be adjusted. For  $R_G = 15\Omega$  the range of adjustment is  $\pm 11$  mV, for higher  $R_G$  proportionately more. For higher  $R_G$  it is recommended to increase  $R_2$  to decrease the range and make trimming less sensitive.

There is also an offset between inverting and non-inverting input which cannot be trimmed out.

# Typical Applications

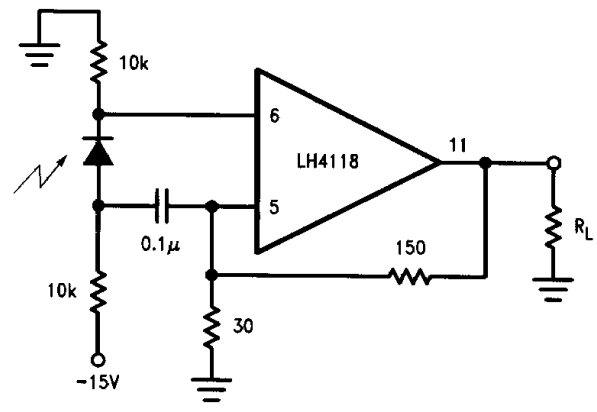
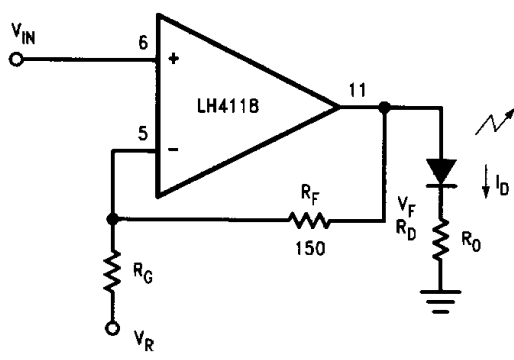


FIGURE 1. Bootstrapped Fiber Optic Receiver

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$$I_D = I_{BIAS} + I_{Signal}$$

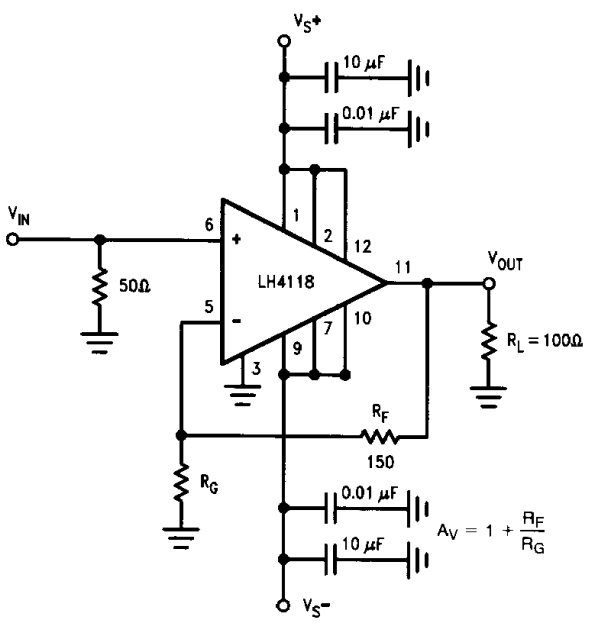
$$I_{BIAS} = \frac{V_R(-R_F/R_G) - V_F}{R_D}$$

$$I_{Signal} = \frac{V_{IN}(1 + R_F/R_G)}{R_D + R_O}$$

$$R_D \approx 26 \text{ mV}/I_{BIAS}$$

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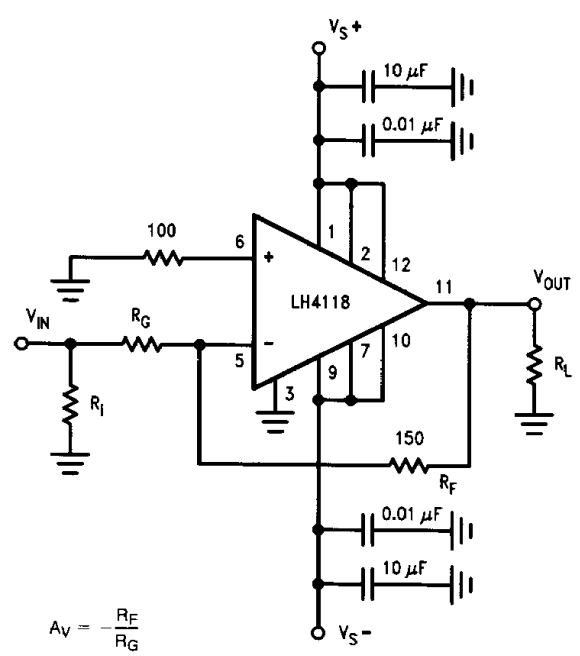
FIGURE 2. Fiber Optic Transmitter



$$A_v = 1 + \frac{R_F}{R_G}$$

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FIGURE 3. Non-Inverting Gain Circuit



$$A_v = -\frac{R_F}{R_G}$$

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FIGURE 4. Inverting Gain Circuit  
Ri is selected so that Ri || RG matches the line impedance (e.g., 50Ω)

### Typical Applications (Continued)

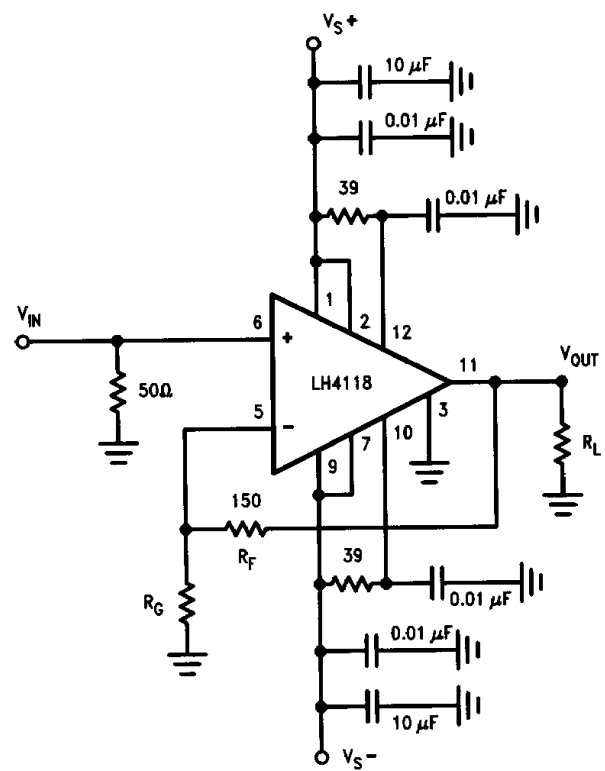
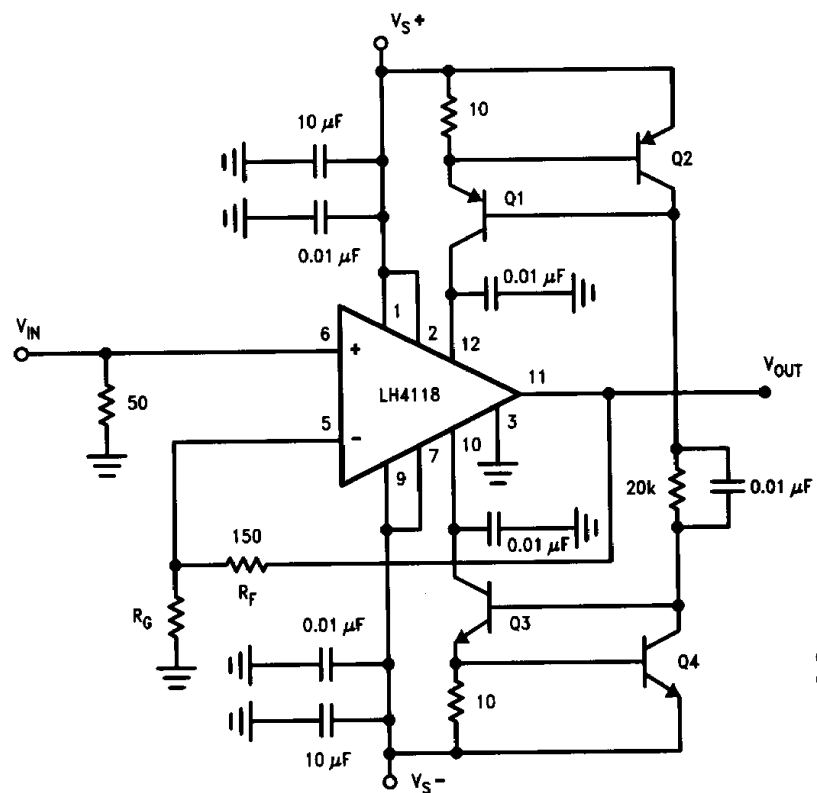


FIGURE 5. Current Limiting Using Resistor

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Q1 = Q2 = 2N2905  
Q3 = Q4 = 2N2219

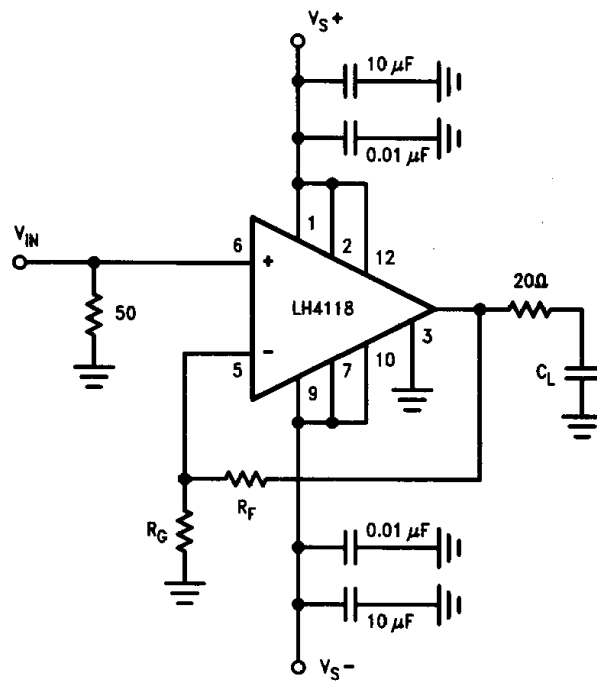
TL/K/9768-11

The current cutoff is set to  $I = \frac{V_{BE}}{R} = \frac{600 \text{ mV}}{10\Omega} = 60 \text{ mA}$ . Higher current peaks are sustained by the 0.01 μF Capacitors.

FIGURE 6. Current Limiting Using Transistor Current Source



## Typical Applications (Continued)

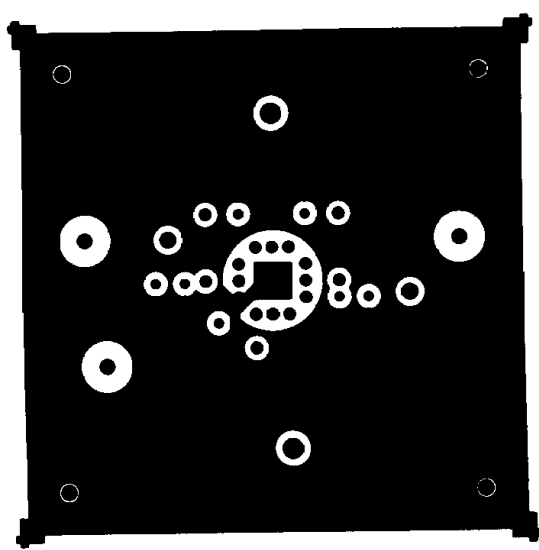


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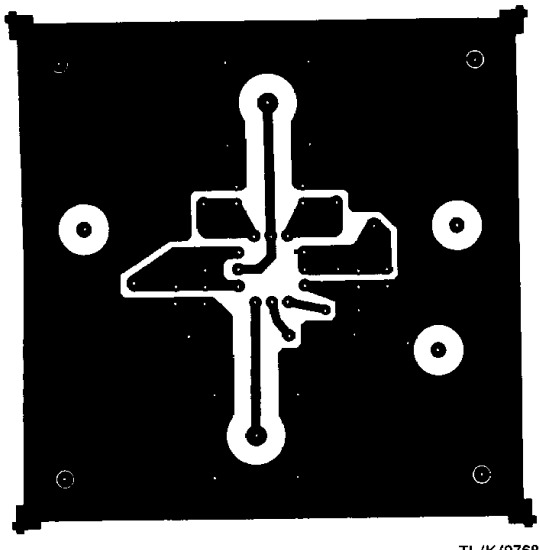
A series resistor between  $50\ \Omega$  and  $500\ \Omega$  helps to stabilize capacitive loads. There is, however, a corresponding drop in bandwidth.

### Evaluation Board

(3" x 3", not to scale)



TL/K/9768-13

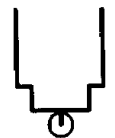


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Top

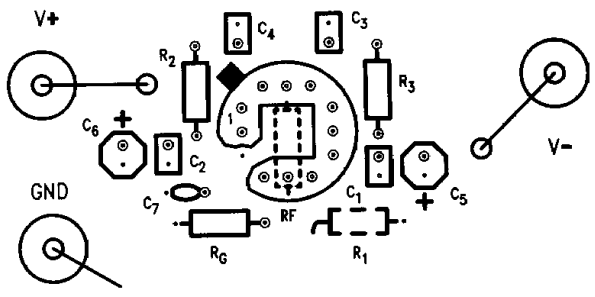
Bottom

#### Components

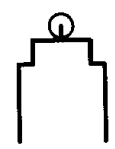


OUTPUT

#### LH4118 DEMO BOARD



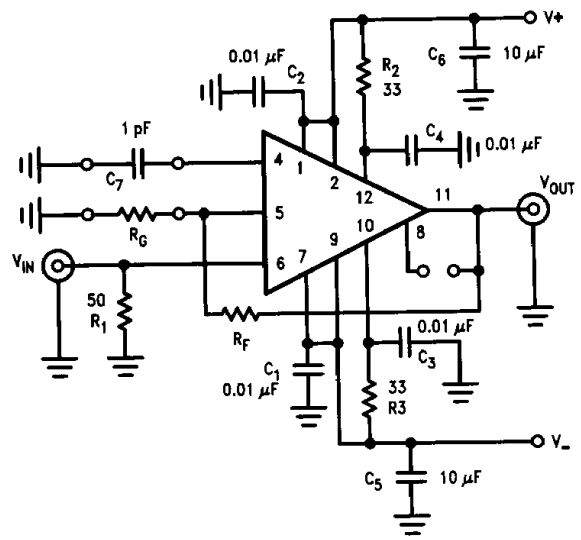
INPUT



Top View

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#### Schematic Diagram



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Input and output connections are made through BNC connectors. When the indicated cut-outs are made, the connectors can be placed in-line. As an alternative, Amphenol No. 31-4758 connectors can be used soldered upright into the board.

R1 is the termination resistor of the input line. It is mounted on the bottom of the board, with one side soldered flat to the center of the input strip-line.

The LH4118 can be soldered directly into the board or Hole-tight pins can be used (Augat part No. 8134-HC-5P2). These pins need plated through holes with a finished inner diameter of  $41 \pm 2$  Mil. For  $A_V = 1$  the built-in  $R_F$  (150Ω) can be utilized by bridging the trace between pins 8 and 11. In this case no external  $R_F$  should be used.