SHARP

TO: _____

REFERENCE

DEVICE SPECIFICATION FOR

64K bit STATIC RAM (8,192 X 8bit)

MODEL NO.

L H 5 1 6 0 H N - 1 0 L

(LH5160N8)

SPEC NO.: EL02Y011

ISSUE: Dec.13.1990

CUSTOMERS APPROVAL

DATE: _____

BY: _____

SHARP CORPORATION 1.17'91. MAIL DATE IC GROUP

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Integrated Circuit Group

SHARP CORPORATION

EL-02-2966

1. General Description

LH5160HN-10L is a static RAM organized as 8,192word×8bit fabricated with a CMOS silicon gate process.
It's main features include:

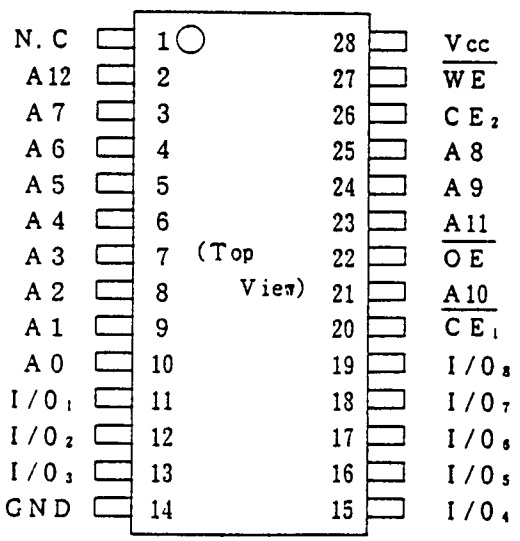
Features

○High speed — Access time ···· 100ns (MAX.)

○Current consumption — Operating ···· 40 mA (MAX.)
Standby ~70℃ ···· 1.0μA (MAX.)
~85℃ ···· 3.0μA (MAX.)
Data hold ···· 0.2μA (Vcc=3V, Ta=25℃)

○Single 5V power supply 5V±10%
○Fully static operation
○All input/output TTL compatible
○Three-state output
○Not designed or rated as radiation hardened
○28pin SOP plastic package
○P-type bulk silicon
○Operating temperature is −40~85℃
○Pin configuration is compatible with industry standard 64K EPROM

2. Pin Configuration



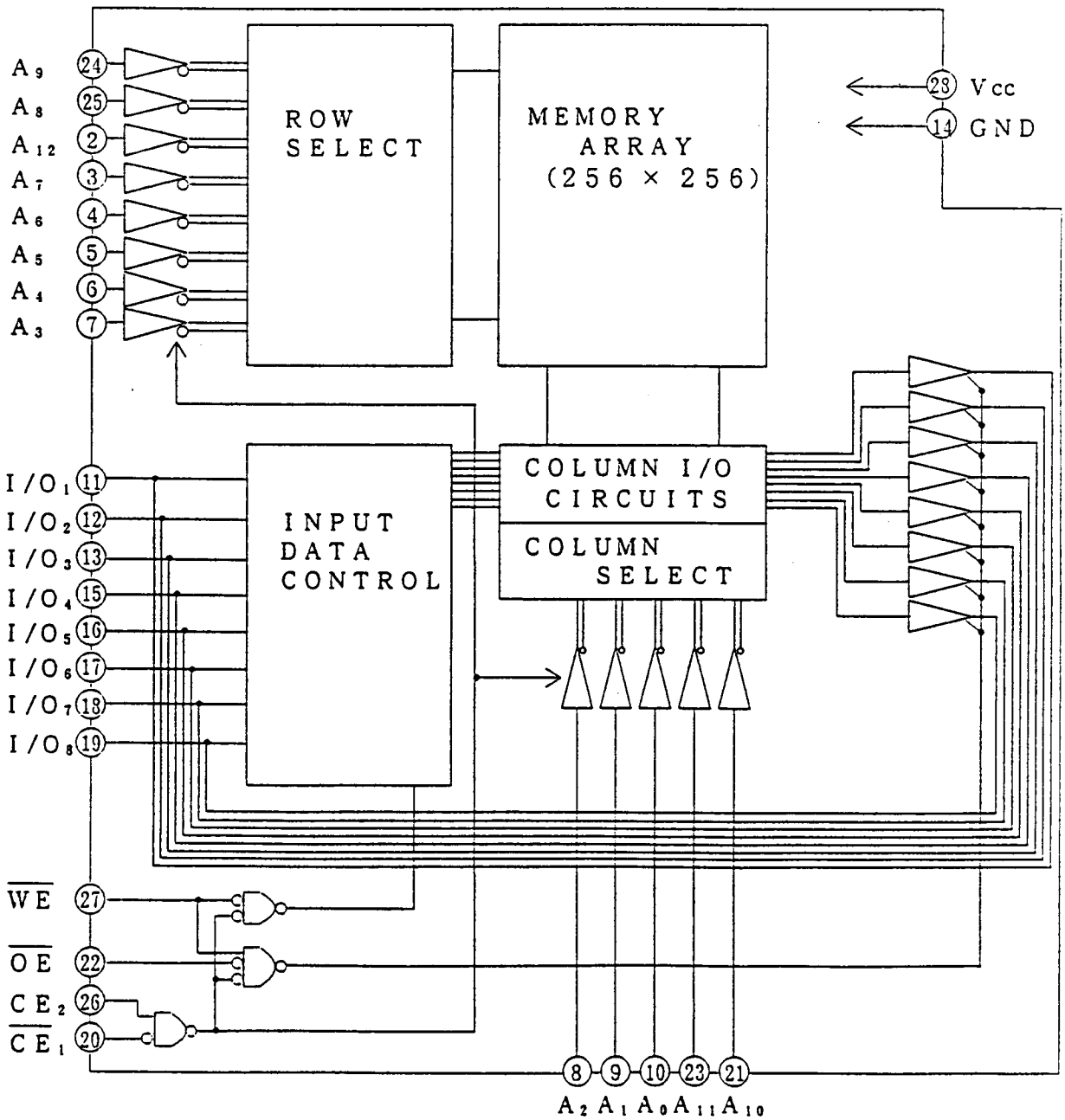
Pin Name	Signal
$A_0 \sim A_{12}$	Address input
$\overline{CE}_1/CE_2$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$I/O_1 \sim I/O_8$	Data input/output
Vcc	Power supply
GND	Ground
N.C.	Non connection

3. Operating Mode

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Mode	$I/O_1 \sim I/O_8$	Supply current
H	X	X	X	Deselect	High Z	Standby (Icc_L)
X	L	X	X			
L	H	L	X	Write	D_{IN}	Operating (Icc)
L	H	H	L	Read	D_{OUT}	Operating (Icc)
L	H	H	H	Output disable	High Z	Operating (Icc)

X : H or L

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage *	V_{CC}	−0.3～+7.0	V
Input voltage *	V_{IN}	−0.3～Vcc+0.3	V
Operating temperature	Topt	−40～+85	℃
Storage temperature	Tstg	−55～+150	℃

* Maximum applicable voltage on any pin with respect to GND

6. Recommended DC Operating Conditions

(Ta=−40～+85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		Vcc+0.3	V
	V_{IL}	−0.3		0.8	V

7. DC Electrical Characteristics

(Ta=−40～+85℃, Vcc=5 V±10%)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0～Vcc			1.0	μA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{I/O}$=0～Vcc			1.0	μA
Operating Supply current	I_{CC}	$\overline{CE_1}=V_{IL}$, $V_{IN}=V_{IL}$ or V_{IH} $CE_2=V_{IH}$, Output open			40	mA
Standby current	I_{CCL1}	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$			10	mA
	I_{CCL}	$CE_2 \leqq 0.2$V or	～+70℃		1.0	μA
		$\overline{CE_1} \geqq V_{CC}-0.2$V *	～+85℃		3.0	μA
Output voltage	V_{OL}	I_{OL}=2.1 mA			0.4	V
	V_{OH}	I_{OH}=−1 mA		2.4		V

* $CE_2 \geqq V_{CC}-0.2$V or $CE_2 \leqq 0.2$V

8. Test Condition of AC Characteristics

Input pulse level	0.6～2.4 V
Input rise/fall time	10 ns
Input/Output timing level	1.5 V
Output load	1TTL+C_L=100pF

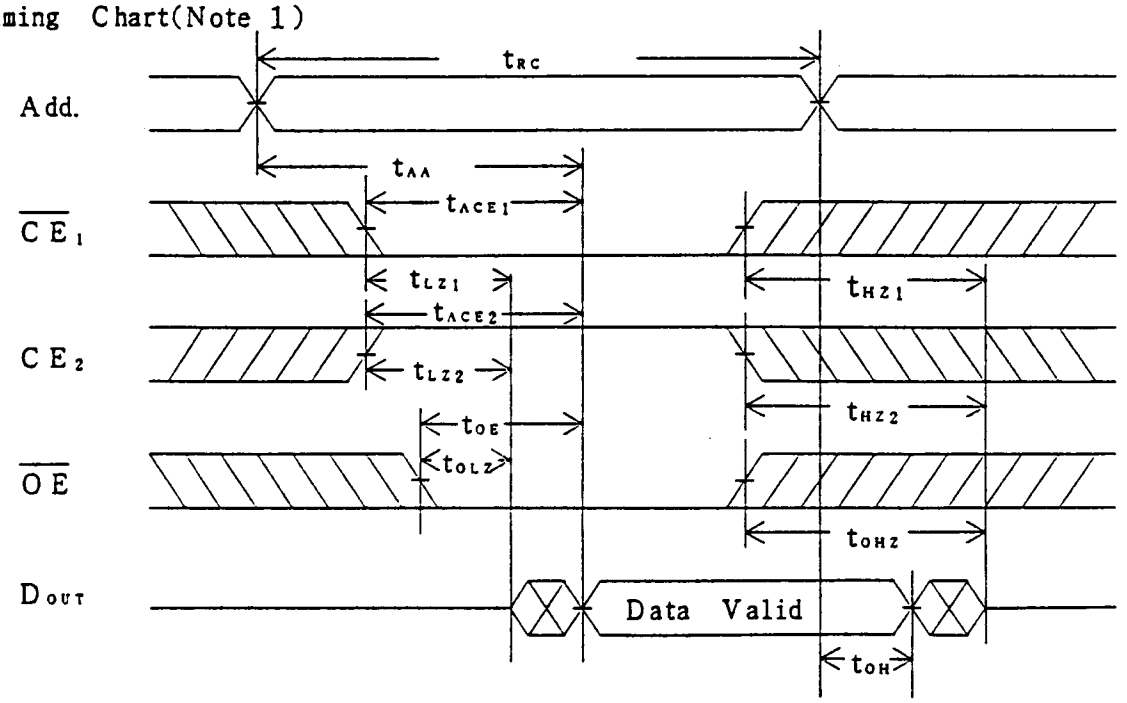
9. AC Characteristics

Read cycle

(Ta = −40~85℃, Vcc = 5 V ±10%)

Parameter	Symbol	Min.	Max.	Unit
Read cycle time	t_{RC}	100		ns
Address access time	t_{AA}		100	ns
Chip enable access time with respect to CE_1	t_{ACE1}		100	ns
Chip enable access time with respect to CE_2	t_{ACE2}		100	ns
Output enable access time	t_{OE}		40	ns
Output hold time	t_{OH}	10		ns
Output floating hold time with respect to $\overline{CE_1}$	t_{LZ1}	10		ns
Output floating hold time with respect to CE_2	t_{LZ2}	10		ns
Output floating time with respect to $\overline{OE}$	t_{OLZ}	5		ns
Output floating time with respect to $\overline{CE_1}$	t_{HZ1}	0	30	ns
Output floating time with respect to CE_2	t_{HZ2}	0	30	ns
Output floating time with respect to $\overline{OE}$	t_{OHZ}	0	20	ns

Timing Chart(Note 1)

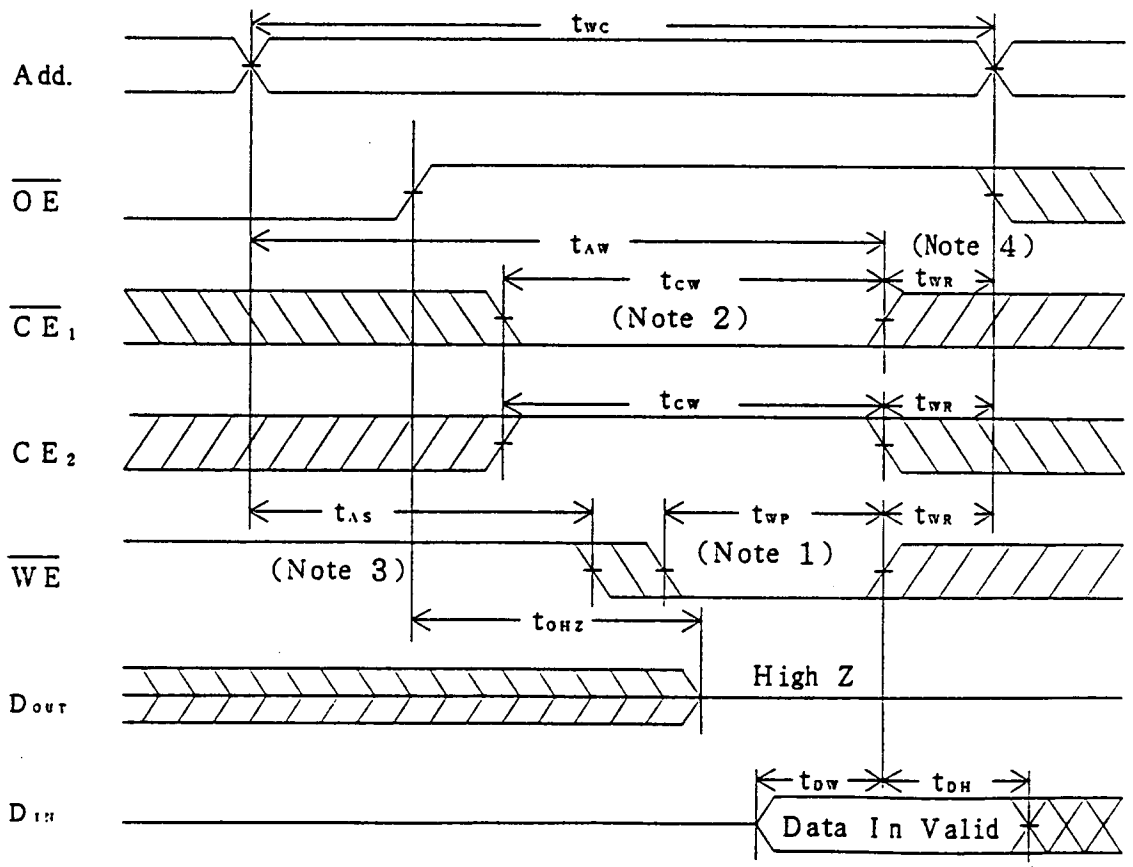


Note1) $\overline{WE}$ is "High"level during the read cycle

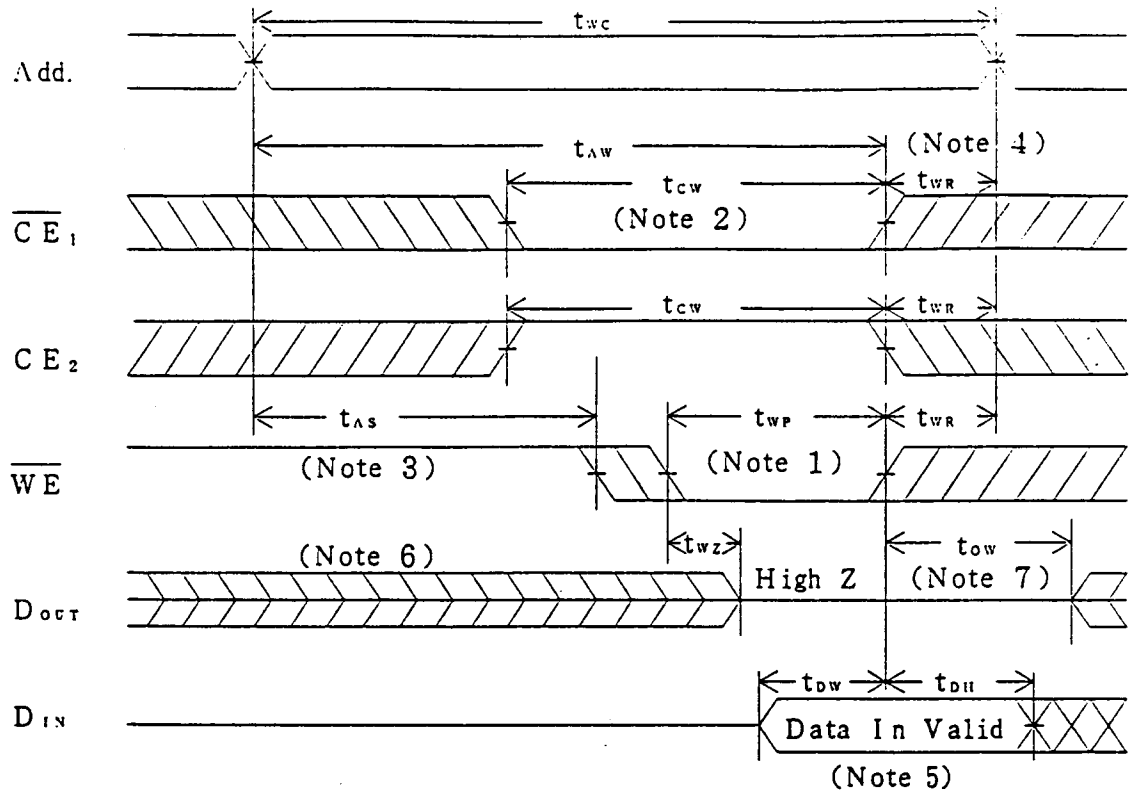
Write cycle

(Ta = −40~85℃, Vcc = 5 V ±10%)

Parameter	Symbol	Min.	Max.	Unit.
Write cycle time	t_{WC}	100		ns
Chip enable time to write	t_{CW}	90		ns
Address valid time	t_{AW}	90		ns
Address setup time	t_{AS}	20		ns
Write pulse width	t_{WP}	60		ns
Write recovery time	t_{WR}	10		ns
Input data set time	t_{DW}	50		ns
Input data hold time	t_{DH}	0		ns
Output floating hold time with respect to $\overline{WE}$	t_{OW}	10		ns
Output floating time with respect to $\overline{WE}$	t_{WZ}	0	30	ns
Output folating time with respect to $\overline{OE}$	t_{OHZ}	0	20	ns



Timing Chart – ($\overline{OE}$ Low fixed)



Note) 1. The writing ocurrs during a overlapping period of $\overline{CE_1}$='Low', CE_2='High' and $\overline{WE}$='Low' (t_{WP}).

2. t_{CW} is defined as the time from the last occuring transit, either $\overline{CE_1}$ Low transit or CE_2 High transit, to the time when the writing is finished.

3. t_{AS} is defined as the time from address change to writing start.

4. t_{WR} is defined as the time from writing finish to address change.

5. Since during this period, I/O pins assume output state, no input signal 180° out of phase with an output signal admitted.

6. If $\overline{CE_1}$ Low transit or CE_2 High transit occurs at the same time or after $\overline{WE}$ Low transit the output will remain High Z.

7. If CE_1 High transit or CE_2 Low transit occurs at the same time or before $\overline{WE}$ High transit, the output remain High Z.

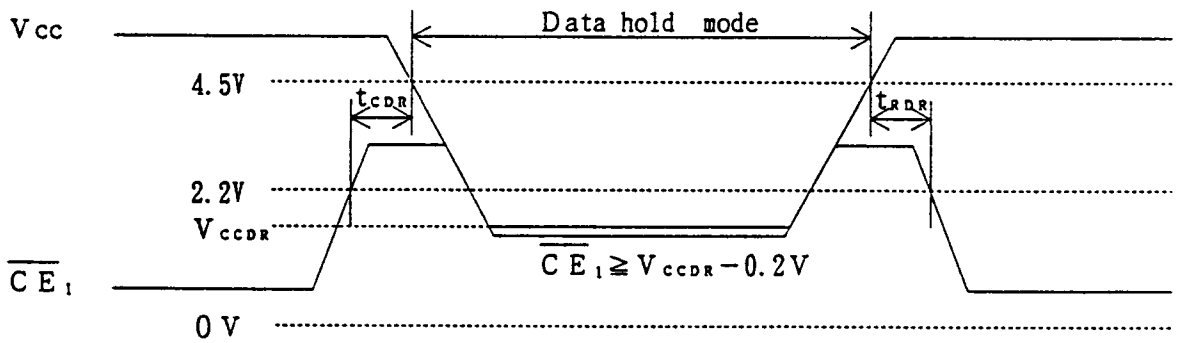
10. Low Voltage Data Hold Characteristics

(Ta = −40 ~ +85℃)

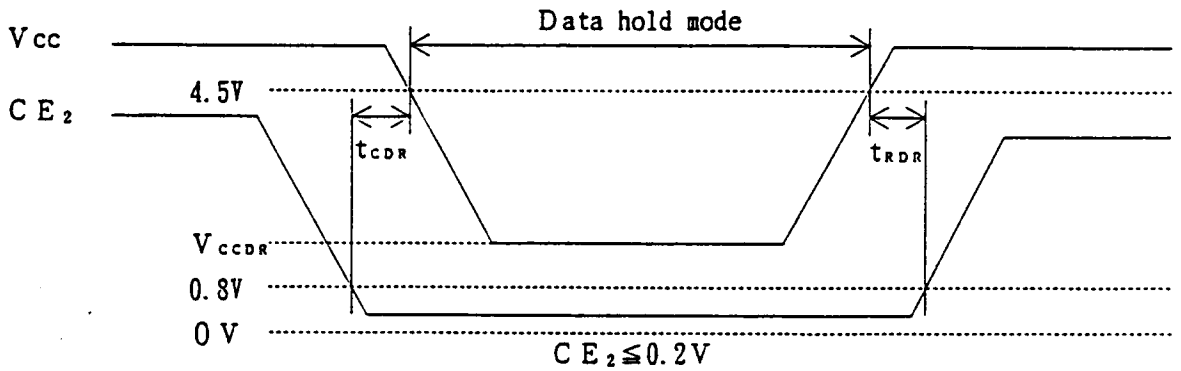
Parameter	Symbol	Condition		Min.	Max.	Unit
Data hold supply voltage	V_{CCDR}	$CE_2 \leqq 0.2V$ or $\overline{CE}_1 \geqq V_{CCDR} - 0.2V$ *		2.0		V
Data hold supply current	I_{CCDR}	$V_{CCDR} = 3V$ $CE_2 \leqq 0.2V$ or $\overline{CE}_1 \geqq V_{CCDR} - 0.2V$ *	Ta = 25℃		0.2	μA
			Ta = 40℃		0.4	
					0.6	
Chip enable setup time	t_{CDR}			0		ns
Chip enable hold time	t_{RDR}			** t_{RC}		ns

* $CE_2 \geqq V_{CCDR} - 0.2V$ or $CE_2 \leqq 0.2V$ ** Read cycle time

Timing Chart−($\overline{CE}_1$ Control) Note)1



Timing Chart−(CE_2 Contorol)



Note)1 To control the data hold mode at $\overline{CE}_1$, fix the input level of CE_2 between $V_{CCDR} \sim V_{CCDR} - 0.2V$ or $0.0V \sim 0.2V$ during the data hold mode.

11. Pin Capacitance

(Ta = 25℃, f = 1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V			7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V			10	pF

Note) Parameter is sample value, not all tested.

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PACKAGE AND PACKING SPECIFICATION

1. Package Outline Specification

Refer to drawing No. AA931

2. Markings

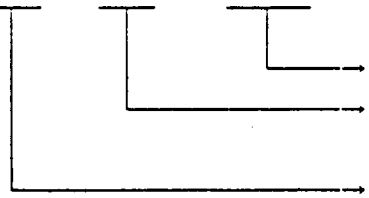
2－1. Marking contents

(1) Product name : LH5160HN－10L

(2) Company name : SHARP

(3) Date code

(Example) YY WW ××× Indicates the product was manufactured in the WWth week of 19YY.



Denotes the production ref.code (1~3)

Denotes the production week. (01,02,03,・・・・・52,53)

Denotes the production year. (Lower two digit of the year.)

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer drawing No. AA931

(This layout do not define the dimensions of marking character and marking position.)

3. Surface Mount Conditions

The conditions below are recommended when mounting ICs not to deteriorate IC quality.

3－1. Soldering conditions

Mounting Method	Temperature and Duration	Measurement Point
Infrared reflow soldering	Peak temperature of 240℃, duration less than 15 seconds above 230℃, temperature increase rate of 1~4℃/second	IC surface
Solder dipping	245℃ or less, duration less than 3 seconds/dip, total of 5 seconds	Solder bath
Vapor phase solderring	215℃ or less, duration less than 40 seconds above 200℃	Steam
Manual soldering (soldering iron)	260℃ or less, duration less than 10 seconds	IC outer lead surface

3－2. Conditions for removal of residual flux

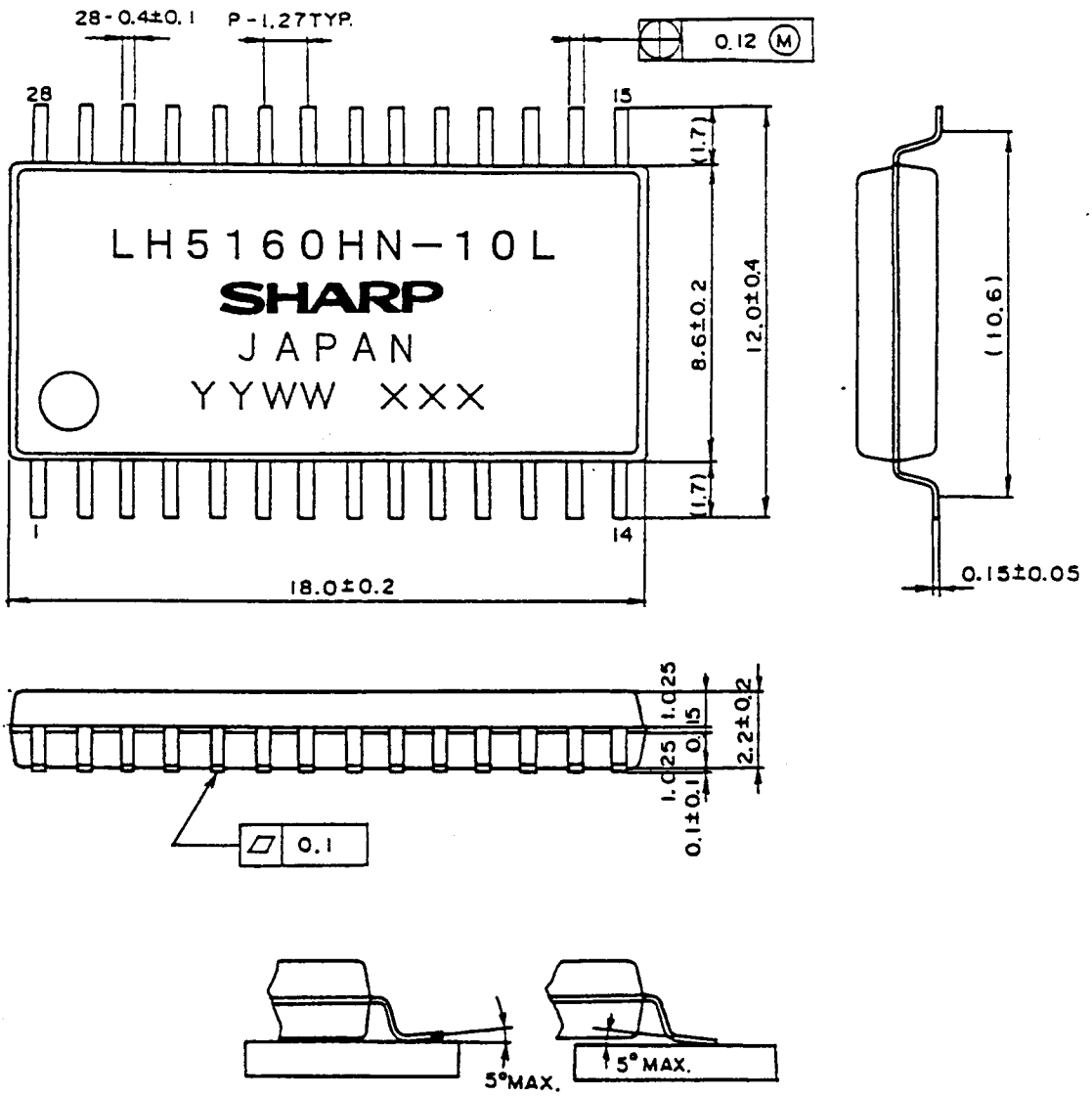
(1) Ultrasonic washing power : 25 Watts/liter or less

(2) Washing time : Total 1 minute maximum

(3) Solvent temperature : 15~40℃

ISSUE DATE	'90.12.03	APPROVE	CHECK	DESIGN	DESIGN	(NOTE)
ISSUE NUMBER	H01203-03	T. Tsuda	T. Kurosaki	T. Kimura	T. Awano	
S/C NUMBER	LH5160N8					

SHARP



名称 NAME	SOP28-P-450	リード仕上 LEAD FINISH	TIN-LEAD PLATING	単位 UNIT	mm	備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。 NOTE Plastic body dimensions do not include burr of resin.
シャープ株式会社 SHARP CORP.	IC事業本部 IC GROUP		DRAWING NO.	AA931		

4. Packing Specification (Embossed Carrier Taping Specification)

This standard apply to the embossed carrier taping specification for ICs to be delivered from SHARP CORPORATION. SHARP's embossed carrier taping specification are, in principle, based on those set forth by the EIAJ (Electronic Industries Association of Japan (RC-1009B)) and the EIA (Electronic Industries Association (EIA481A)).

4 − 1. Tape Structure

- Embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and covered with a top covering tape to enclose them.

4 − 2. Taping Reel and Embossed Carrier Tape Size

- For the taping reel and embossed carrier tape sizes, refer to the attached drawings (NO.CV524 and CV521)

4 − 3. IC Package Enclosure in Embossed Carrier Tape

- The IC package enclosure direction in the embossed portion as it compares to the direction in which the tape is pulled is indicated by an index mark on package (Index mark indicate the NO.1 pin on package) in the attached drawing (NO. CV522).

4 − 4. Missing IC Packages inside Embossed Carrier Tape

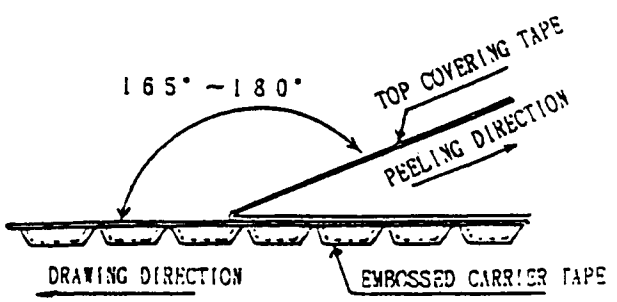
- The number of missing IC packages inside the embossed carrier tape should not exceed 0.1% of the total enclosed in the tape per reel, or 1, Whichever may be larger. There should never be more than two consecutive missing IC package.

4 − 5. Tape Joints

- The embossed carrier tape should not have more than one joint per reel.

4 − 6. Peeling Strength of the Top Covering Tape

- Peeling strength must meet the following conditions.
  1) Peeling angle
     at 165° to 180°
  2) Peeling speed
     at 300mm/min.
  3) Peeling strength
     at 0.2 to 0.7N (20 to 70gf)



4 − 7. Packing

- The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, shall be held in place with paper adhesive tape exceeding 30mm in length.
- The leading and trailing edges of the embossed carrier tape shall be left empty (with embossed portions not filled with IC packages), in the attached drawing (NO. CV522).
- The number of IC packages enclosed in the embossed carrier tape per reel shall, in principle, be as listed below.

Package Type	Number of IC Packages/Reel
SOP14PIN, SOP16PIN	3,000 pcs
SOP24PIN	1,500 pcs
SOP28PIN	1,000 pcs

4 − 8. Indications

- The following shall be indicated on the taping reel and the packing case.
  1) Part Number (Product Name)
  2) Storage Quantity
  3) Production Date
  4) Manufacture's Name (SHARP)

Note : The IC taping direction shall be indicated by "E1" or "E2" suffixed to the part number.

E1 : Eqiuvalent to "f" of the EIAJ (RC-1009B) standard.
E2 : Equivalent to "B" of the EIAJ (RC-1009B) standard.

4 − 9. Protection While in Transit

Embossed carrier tape should be free from deformed IC leads and deterioration in electrical characteristics.

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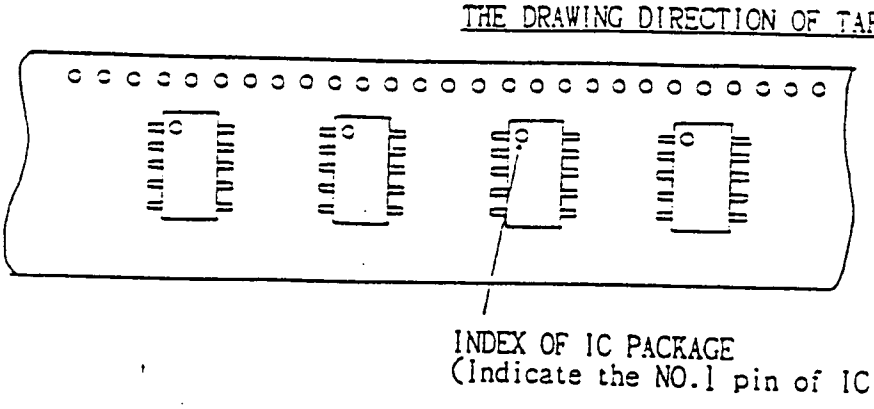
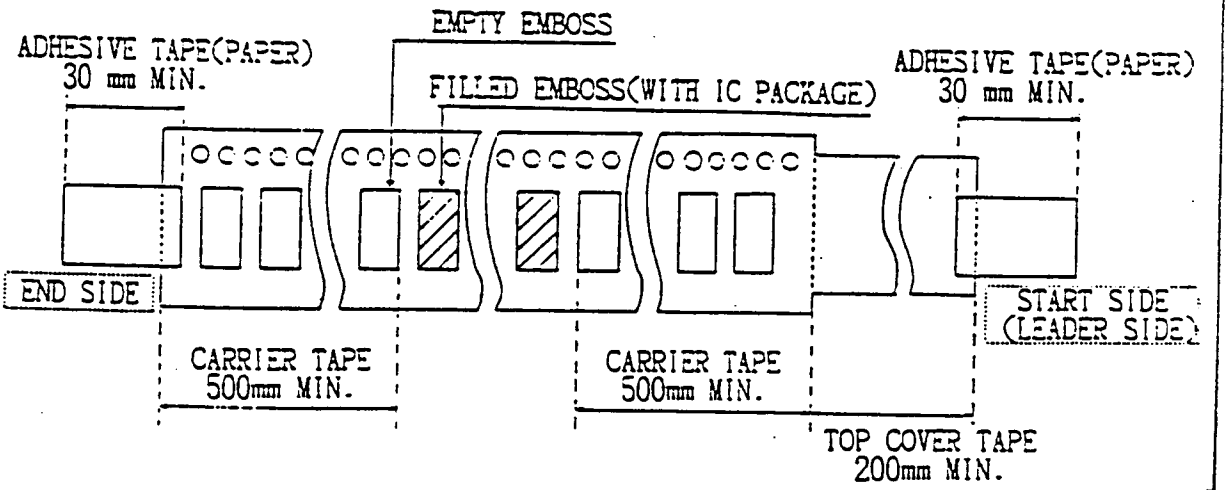
EMBOSS TAPING TYPE (E2)

IC TAPING DIRECTION

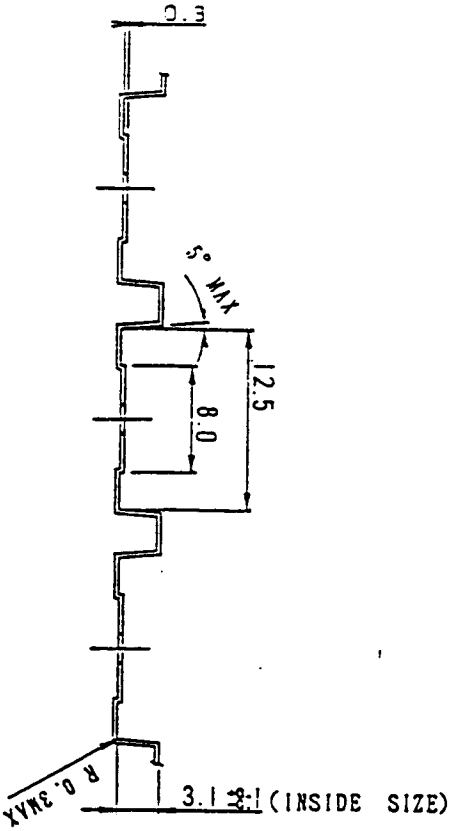


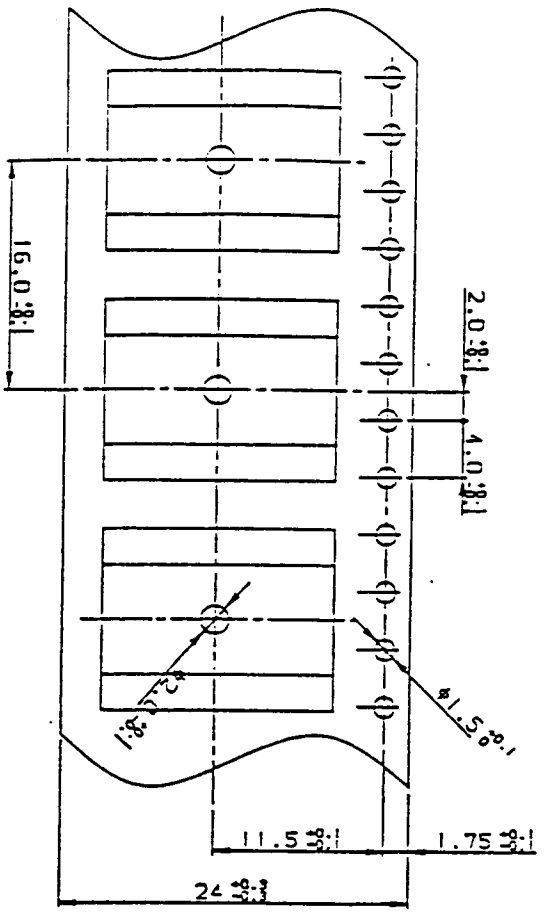
LEADER SIDE AND END SIDE OF TAPE

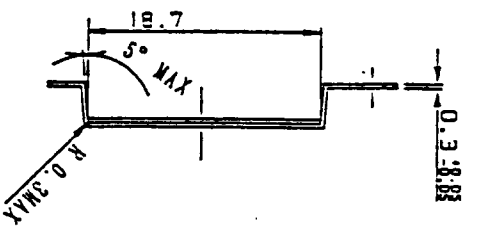


尺度 SCALE	単位 UNIT		
/	1 = /		
		改訂DATE	改訂記事 REVISE 担当 CHARGE
材質MATERIAL	仕上 FINISH	名称 NAME	EMBOSS TAPING TYPE (E2)
		コード CODE	
シャープ株式会社 IC事業本部			
SHARP CORPORATION		図番 DRAWING No	CV522

SHARP







尺度 SCALE	単位 UNIT	⚠ . .		
1/2	1 = m/m	⚠ . .		
		改訂日 DATE	改訂記事 REVISE	担当 CHARGE
材質 MATERIAL	仕上 FINISH	名称 NAME	EC28SPS	
CONDUCTIVE PVC		コード CODE		
シャープ株式会社 IC事業本部		図番 DRAWING No.	CV524	
SHARP CORPORATION				

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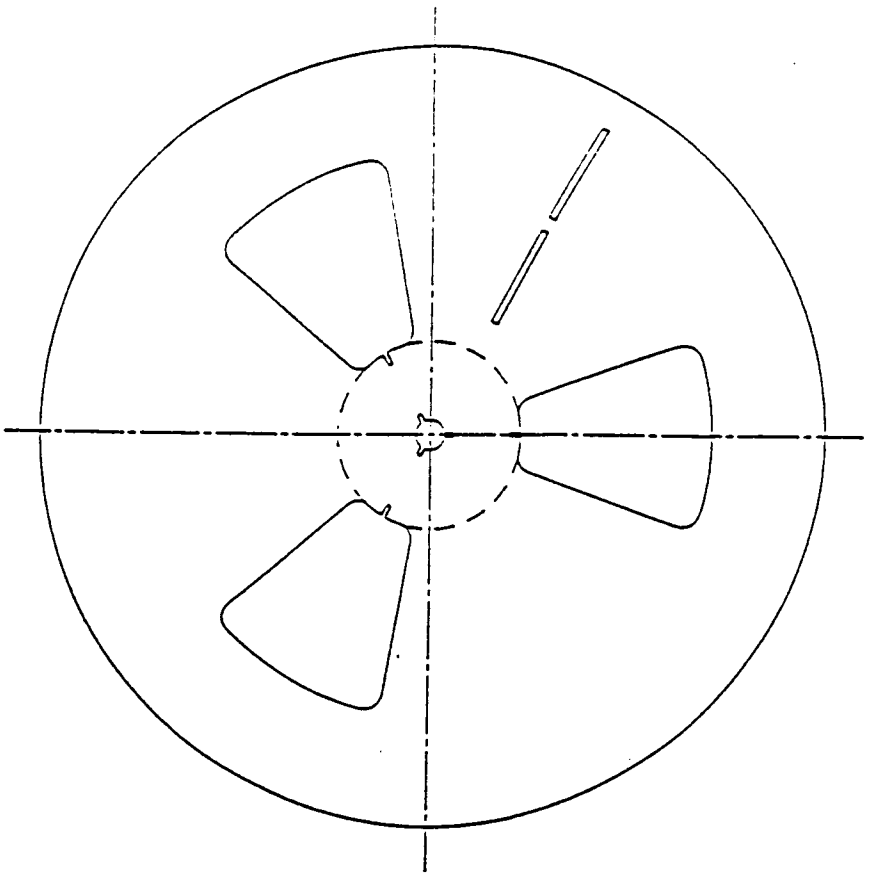

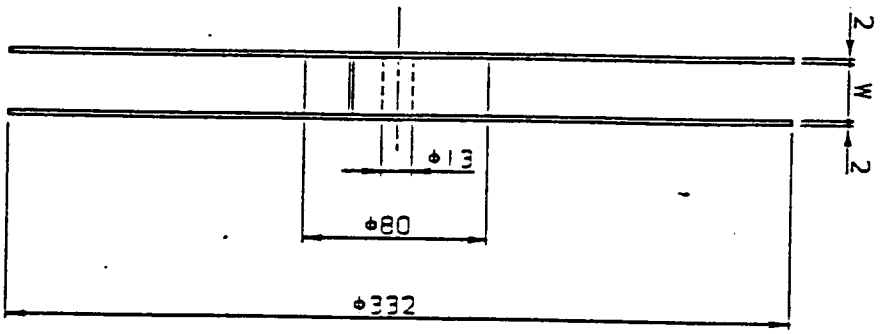

PKG	W (mm)	TAPE NUMBER
SOP14-P-225	16.4	ECR16
SOP16-P-225	〃	〃
SOP24-P-450	24.4	ECR24
SOP28-P-450	〃	〃

尺度 SCALE	単位 UNIT	△ . .	
/	1 = m/m	△ . .	
		改訂日 DATE	改訂記事 REVISE 担当 CHARG
材質 MATERIAL	仕上 FINISH	名称 NAME	REEL FOR EMBOSS CARRIER TAPING
CONDUCTIVE PS		コード CODE	
シャープ株式会社 IC事業本部			
SHARP CORPORATION		図番 DRAWING No.	CV521

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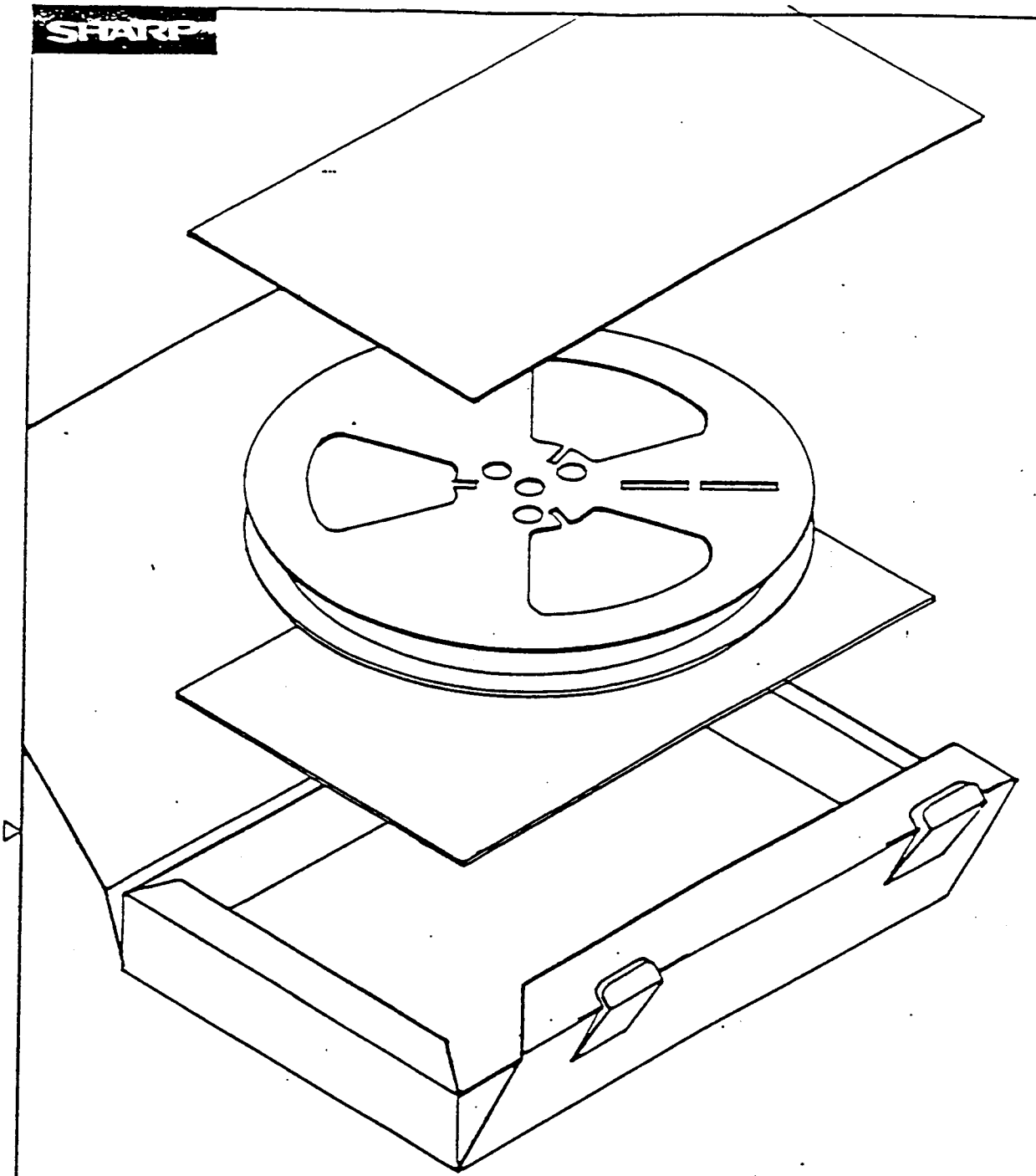

CASE. SIZE : 350×342×56 (mm)

尺度 SCALE	単位 UNIT	⚠			
/	1 = /	⚠			
		改訂日 DATE	改訂記事 REVISE	担当 CHARGE
材質 MATERIAL	仕上 FINISH	名称 NAME	EXTERNAL APPEARANCE OF PACKING CASE FOR EMBOSS CARRIER TAPING		
		コード CODE			
ｼｬｰﾌﾟ株式会社 IC事業本部					
SHARP CORPORATION		図番 DRAWING No	BJ246		