

# LH5164AV

CMOS 64K (8K × 8) Static RAM

## FEATURES

- 8,192 × 8 bit organization
- Access time: 200 ns (MAX.)
- Supply current (MAX.):
  - Operating: 248 mW
  - 55 mW ( $t_{RC}$ ,  $t_{WC} = 1 \mu s$ )
  - Standby: 5.5  $\mu W$
  - Data retention: 0.6  $\mu W$  ( $V_{CC} = 3 V$ ,  $t_A = 25^\circ C$ )
- Wide operating voltage range: 2.7 V to 5.5 V
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Packages:
  - 28-pin, 450-mil SOP
  - 28-pin, 8 × 13 mm<sup>2</sup> TSOP (Type I)

## DESCRIPTION

The LH5164AV is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

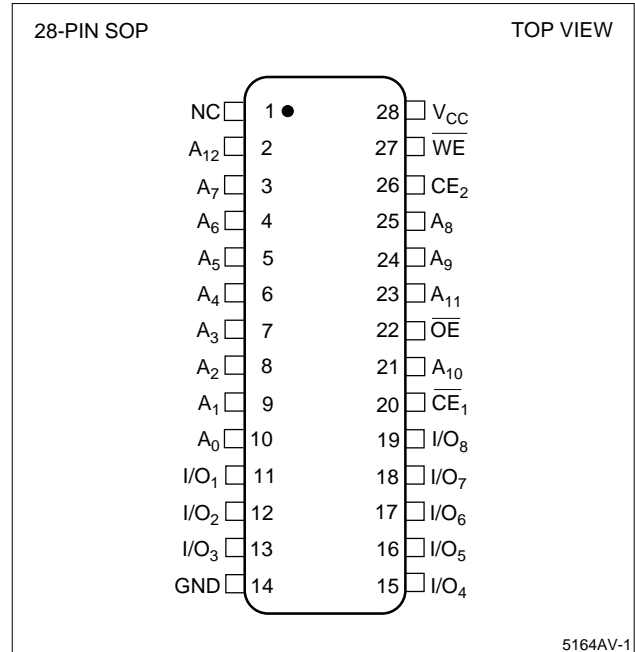


Figure 1. Pin Connections for SOP Package

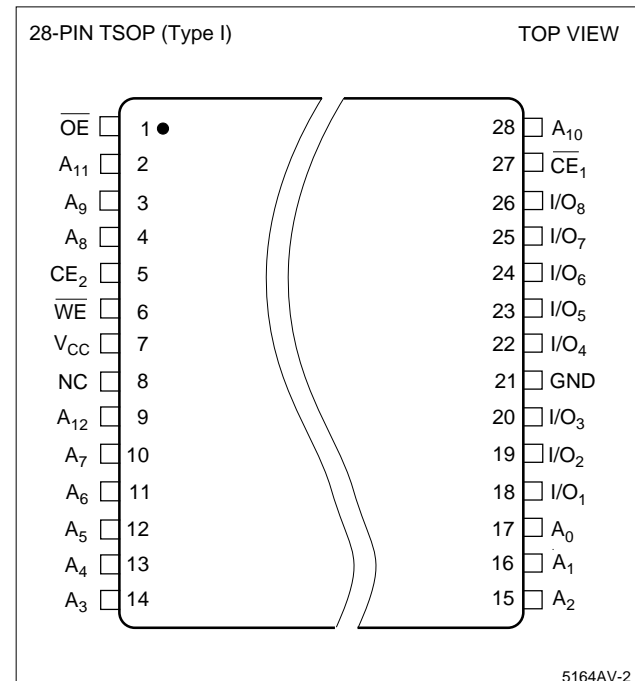


Figure 2. Pin Connections for TSOP Package

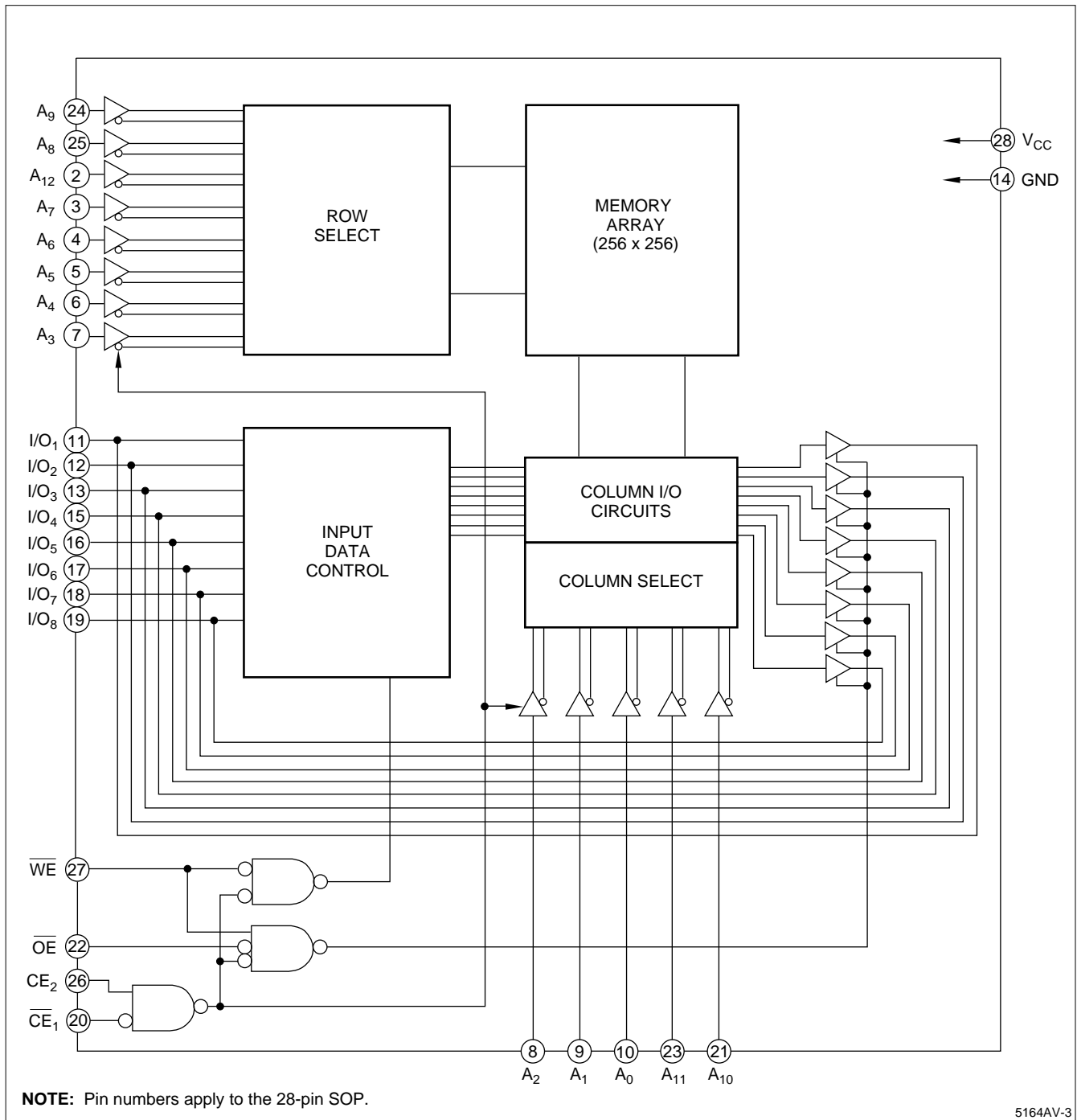


Figure 3. LH5164AV Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>12</sub>	Address inputs
CE <sub>1</sub> /CE <sub>2</sub>	Chip Enable input
WE	Write Enable input
OE	Output Enable input

SIGNAL	PIN NAME
I/O <sub>1</sub> - I/O <sub>8</sub>	Data inputs and outputs
V <sub>CC</sub>	Power supply
GND	Ground
NC	No connection

## TRUTH TABLE

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	MODE	I/O <sub>1</sub> - I/O <sub>8</sub>	SUPPLY CURRENT	NOTE
H	X	X	X	Standby	High-Z	Standby (I <sub>SB</sub> )	1
X	L	X	X				
L	H	L	X	Write	Data input	Operating (I <sub>CC</sub> )	1
L	H	H	L	Read	Data output	Operating (I <sub>CC</sub> )	
L	H	H	H	Output disable	High-Z	Operating (I <sub>CC</sub> )	

## NOTE:

1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V	1
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> + 0.3	V	1, 2
Operating temperature	T <sub>opr</sub>	-10 to +70	°C	
Storage temperature	T <sub>stg</sub>	-65 to +150	°C	

## NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. V<sub>IN</sub> (MIN.) = -3.0 V for pulse width ≤ 50 ns.

RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = -10°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	2.7		5.5	V	
Input voltage (V <sub>CC</sub> = 2.7 V to 3.6 V)	V <sub>IH</sub>	V <sub>CC</sub> - 0.5		V <sub>CC</sub> + 0.3	V	
	V <sub>IL</sub>	-0.3		0.2	V	1
Input voltage (V <sub>CC</sub> = 4.5 V to 5.5 V)	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3	V	
	V <sub>IL</sub>	-0.3		0.8	V	1

## NOTE:

1. V<sub>IL</sub> (MIN.) = -3.0 V for pulse width ≤ 50 ns.

DC CHARACTERISTICS <sup>1</sup> ( $T_A = -10^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input leakage current	$I_{LI}$	$V_{IN} = 0\text{ V}$ to $V_{CC}$	-1.0	1.0	$\mu\text{A}$	
Output leakage current	$I_{LO}$	$CE_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$ $V_{I/O} = 0$ to $V_{CC}$	-1.0	1.0	$\mu\text{A}$	
Operating supply current	$I_{CC}$	$CE_1 = 0.2\text{ V}$ , $V_{IN} = 0.2\text{ V}$ , or $V_{CC} - 0.2\text{ V}$ $CE_2 = V_{CC} - 0.2\text{ V}$ , Outputs open, $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	$t_{CYCLE} = 200\text{ ns}$	20	mA	
			$t_{CYCLE} = 1.0\ \mu\text{s}$	8		
		$CE_1 = V_{IL}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ $CE_2 = V_{IH}$ , Outputs open, $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	$t_{CYCLE} = 200\text{ ns}$	45		
			$t_{CYCLE} = 1.0\ \mu\text{s}$	10		
Standby current	$I_{SB}$	$CE_2 \leq 0.2\text{ V}$ or $CE_1 \geq V_{CC} - 0.2\text{ V}$	$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	0.6	$\mu\text{A}$	1
			$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	1.0		
Output voltage	$V_{OL}$	$I_{OL} = 500\ \mu\text{A}$ , $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ $I_{OL} = 2.1\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$		0.4	V	
				0.4		
	$V_{OH}$	$I_{OH} = -500\ \mu\text{A}$ , $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ $I_{OH} = -1.0\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	$V_{CC} - 0.5$		V	
			2.4			
	$I_{SB1}$	$CE_1 = V_{IH}$ or $CE_2 = V_{IL}$		5	mA	

**NOTE:**

- $CE_2$  should be  $\geq V_{CC} - 0.2\text{ V}$  or  $\leq 0.2\text{ V}$  when  $CE_1 \geq V_{CC} - 0.2\text{ V}$ .

**READ CYCLE ( $T_A = -10^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$ )**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read cycle time	$t_{RC}$	200		ns
Address access time	$t_{AA}$		200	ns
CE <sub>1</sub> access time	$t_{ACE1}$		200	ns
CE <sub>2</sub> access time	$t_{ACE2}$		200	ns
Output enable access time	$t_{OE}$		150	ns
Output hold time	$t_{OH}$	10		ns
CE <sub>1</sub> Low to output in Low-Z	$t_{LZ1}$	20		ns
CE <sub>2</sub> High to output in Low-Z	$t_{LZ2}$	20		ns
OE Low to output in Low-Z	$t_{OLZ}$	10		ns
CE <sub>1</sub> High to output in High-Z	$t_{HZ1}$	0	60	ns
CE <sub>2</sub> Low to output in High-Z	$t_{HZ2}$	0	60	ns
OE High to output in High-Z	$t_{OHZ}$	0	40	ns

**WRITE CYCLE ( $T_A = -10^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$ )**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	$t_{WC}$	200		ns
CE Low to end of write	$t_{CW}$	180		ns
Address valid to end of write	$t_{AW}$	180		ns
Address setup time	$t_{AS}$	0		ns
Write pulse width	$t_{WP}$	150		ns
Write recovery time	$t_{WR}$	0		ns
Input data setup time	$t_{DW}$	100		ns
Input data hold time	$t_{DH}$	0		ns
WE High to output in Low-Z	$t_{OW}$	20		ns
WE Low to output in High-Z	$t_{WZ}$	0	60	ns
OE High to output in High-Z	$t_{OHZ}$	0	40	ns

**TEST CONDITIONS**

PARAMETER	MODE	NOTE
Input pulse level	0.2 V to $V_{CC} - 0.2\text{ V}$	
Input rise/fall time	10 ns	
Input/output timing level	1.5 V	
Output load	$C_L$ (100 pF)	1

**NOTE:**

1. Includes scope and jig capacitance.

**CAPACITANCE <sup>1</sup> ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$			7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF

**NOTE:**

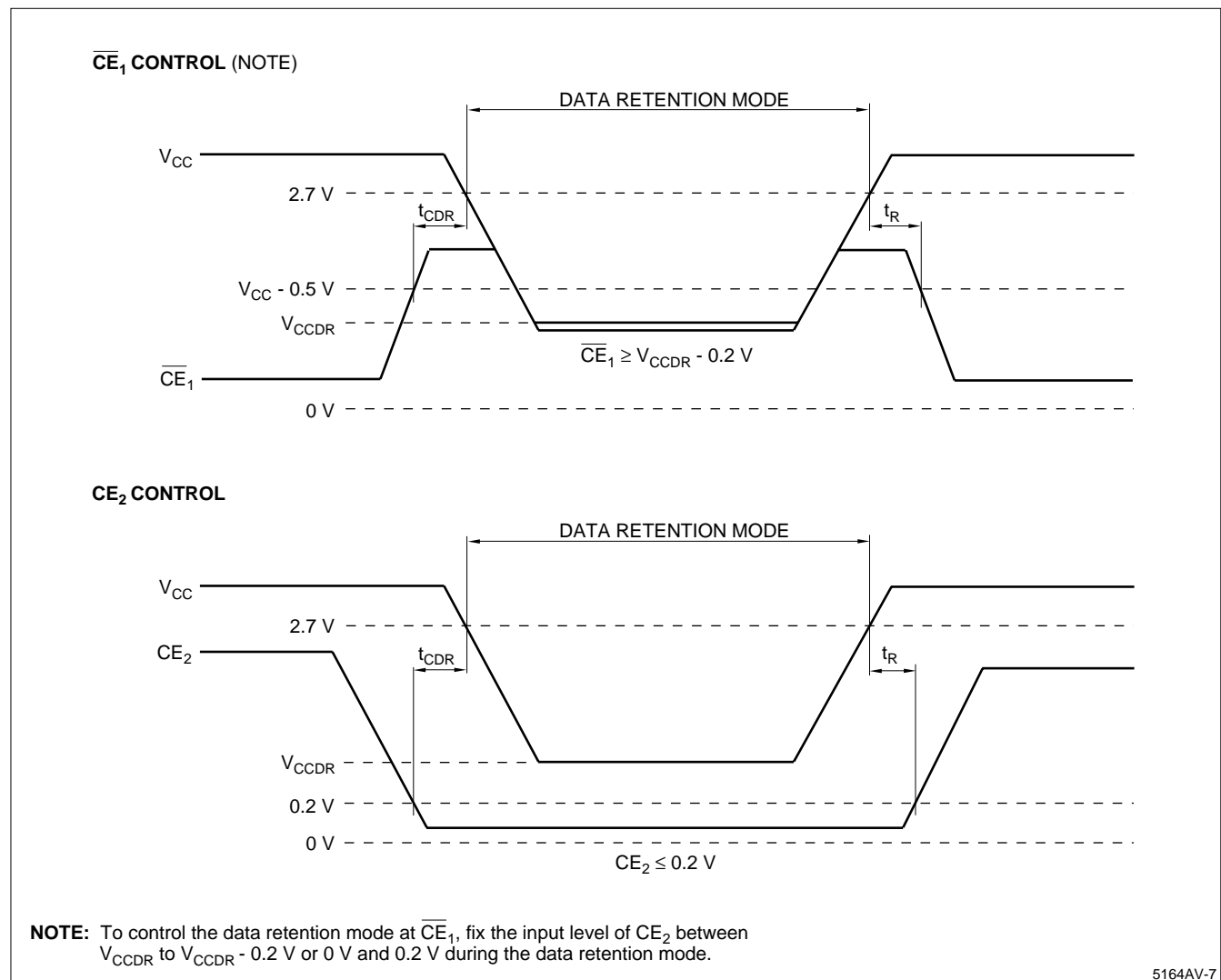
1. This parameter is sampled and not production tested.

**DATA RETENTION CHARACTERISTICS (T<sub>A</sub> = -10°C to +70°C)**

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V <sub>CCDR</sub>	CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> ≥ V <sub>CCDR</sub> - 0.2 V	2.0	5.5	V	1
Data retention supply current	I <sub>CCDR</sub>	V <sub>CCDR</sub> = 3 V, CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> ≥ V <sub>CCDR</sub> - 0.2 V		0.2	μA	1
		T <sub>A</sub> = 25°C		0.4	μA	
		T <sub>A</sub> = 40°C		0.6	μA	
Chip disable to data retention	t <sub>CDR</sub>		0		ns	
Recovery time	t <sub>R</sub>		t <sub>RC</sub>		ns	2

**NOTES:**

1. CE<sub>2</sub> should be ≥ V<sub>CCDR</sub> - 0.2 V or ≤ 0.2 V when CE<sub>1</sub> ≥ V<sub>CCDR</sub> - 0.2 V.
2. t<sub>RC</sub> = Read cycle time.



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**Figure 4. Data Retention Characteristics**

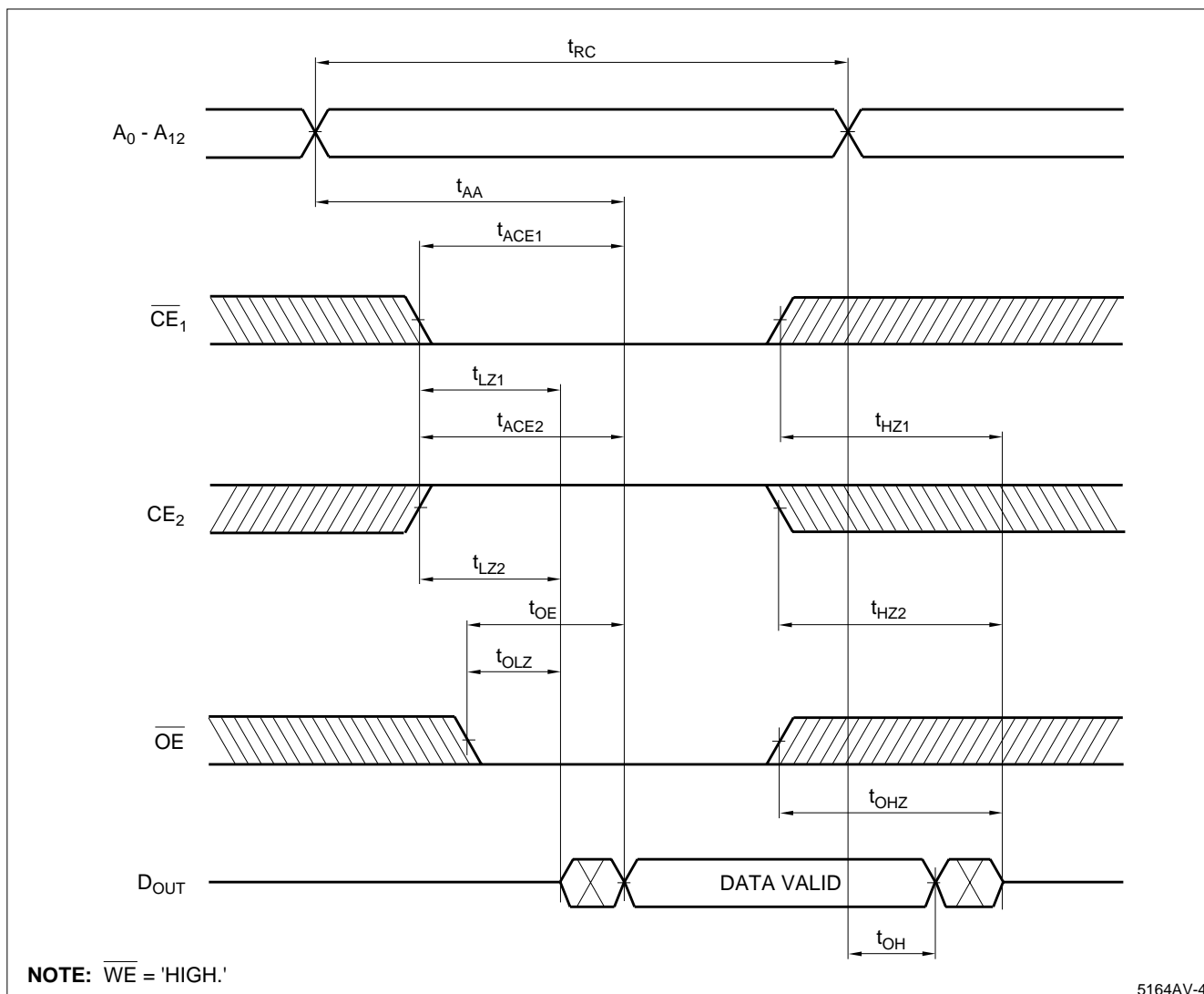
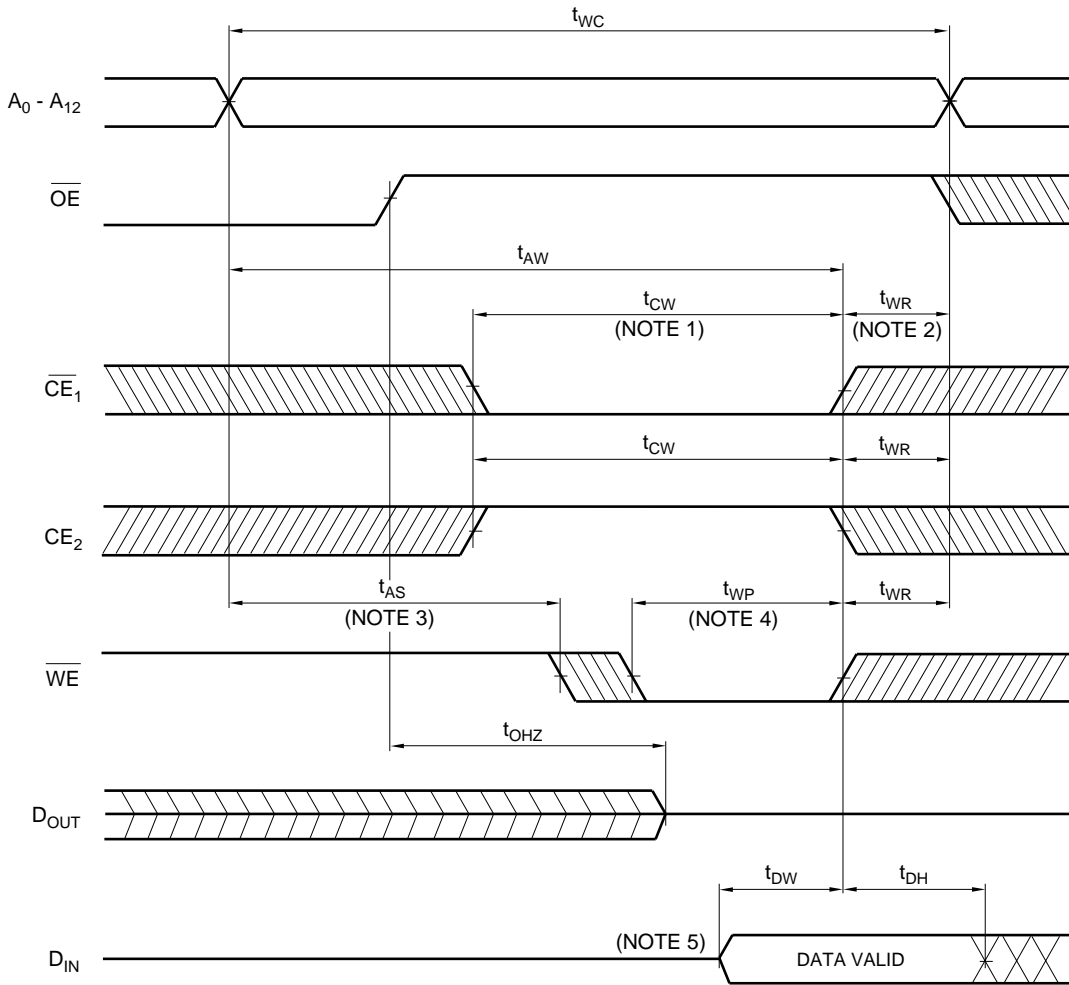


Figure 5. Read Cycle



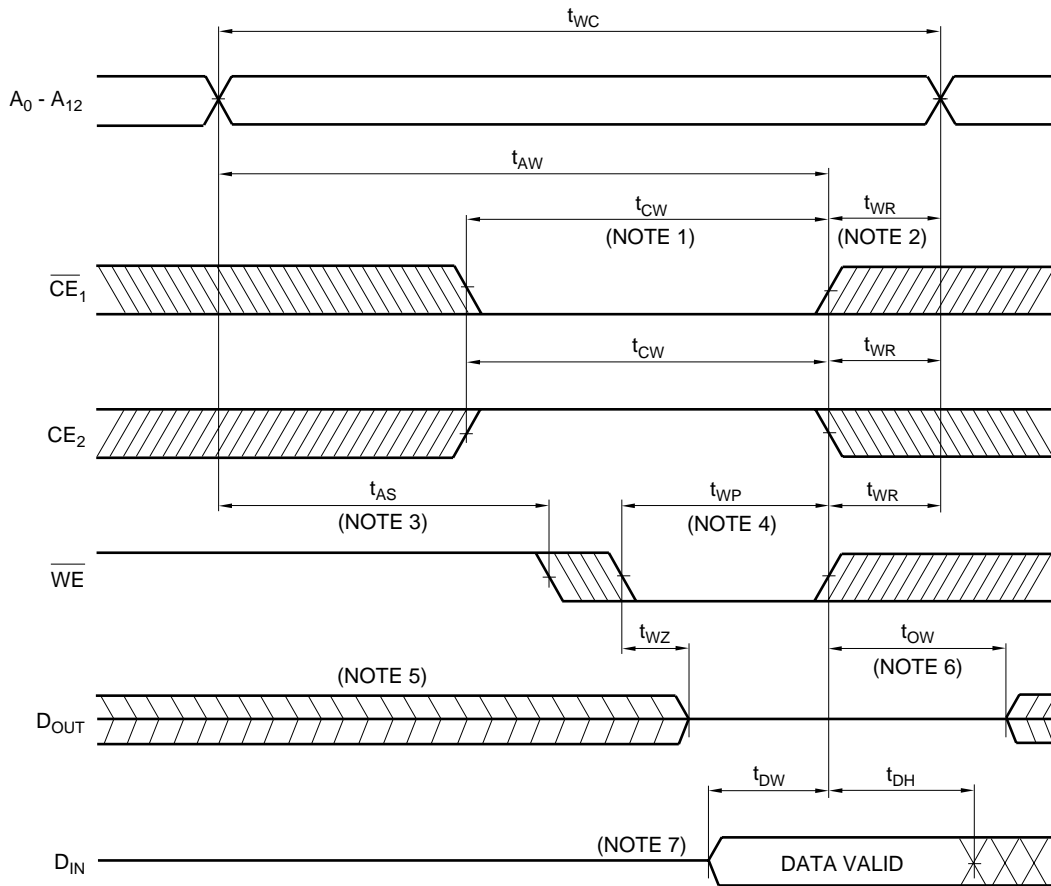
**NOTES:**

1.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition, to the time when the writing is finished.
2.  $t_{WR}$  is defined as the time from writing finish to address change.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4. The writing occurs during an overlapping period of  $\overline{CE}_1 = \text{'LOW'}$ ,  $CE_2 = \text{'HIGH'}$ , and  $\overline{WE} = \text{'LOW'}$  ( $t_{WP}$ ).
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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**Figure 6. Write Cycle (OE Controlled)**





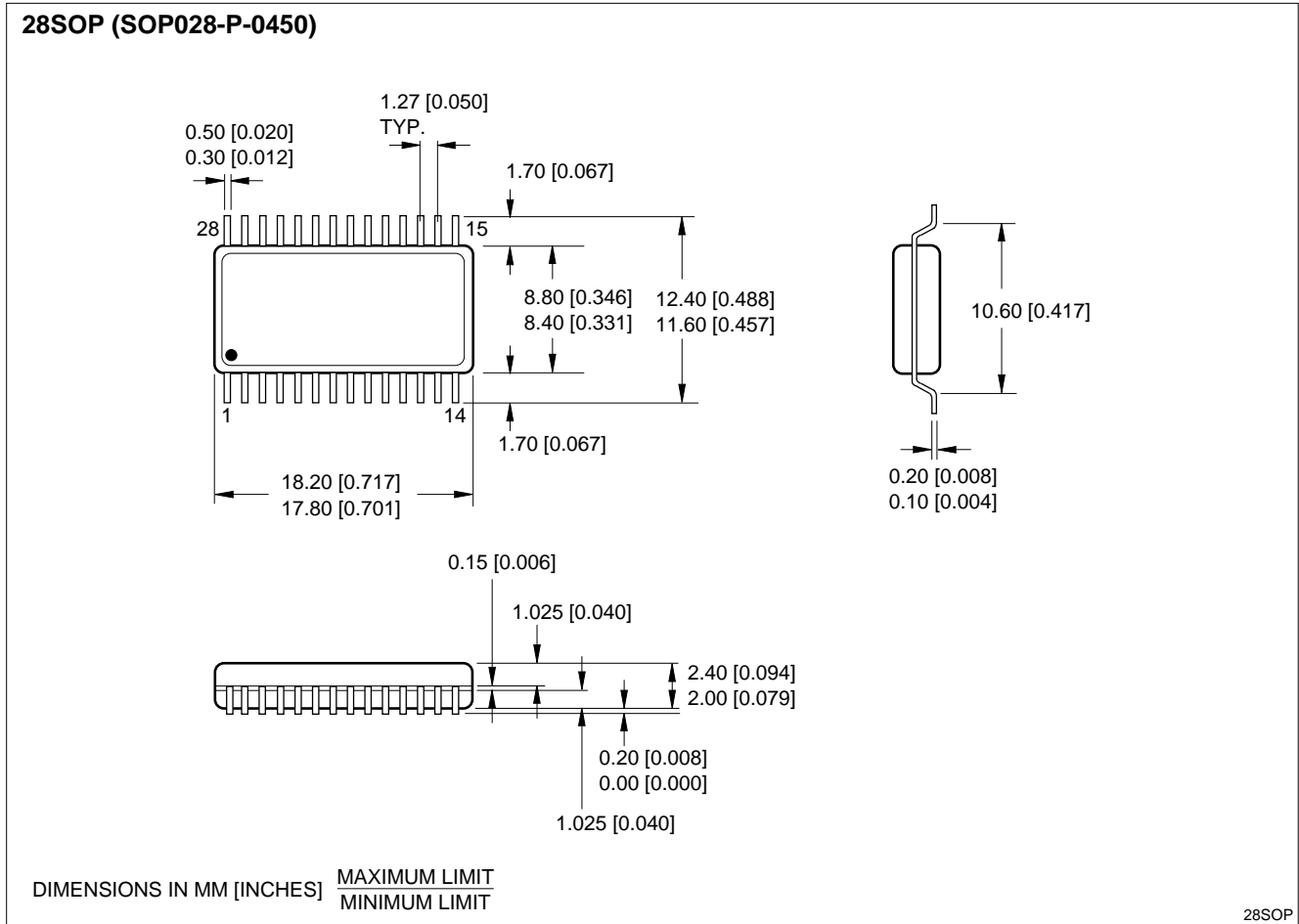
**NOTES:**

1.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition, to the time when the writing is finished.
2.  $t_{WR}$  is defined as the time from writing finish to address change.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4. The writing occurs during an overlapping period of  $\overline{CE}_1 = \text{'LOW'}$ ,  $CE_2 = \text{'HIGH'}$ , and  $\overline{WE} = \text{'LOW'}$  ( $t_{WP}$ ).
5. If  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition occurs at the same time or after  $\overline{WE}$  LOW transition, the outputs will remain high-impedance.
6. If  $\overline{CE}_1$  HIGH transition or  $CE_2$  LOW transition occurs at the same time or before  $\overline{WE}$  HIGH transition, the outputs will remain high-impedance.
7. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

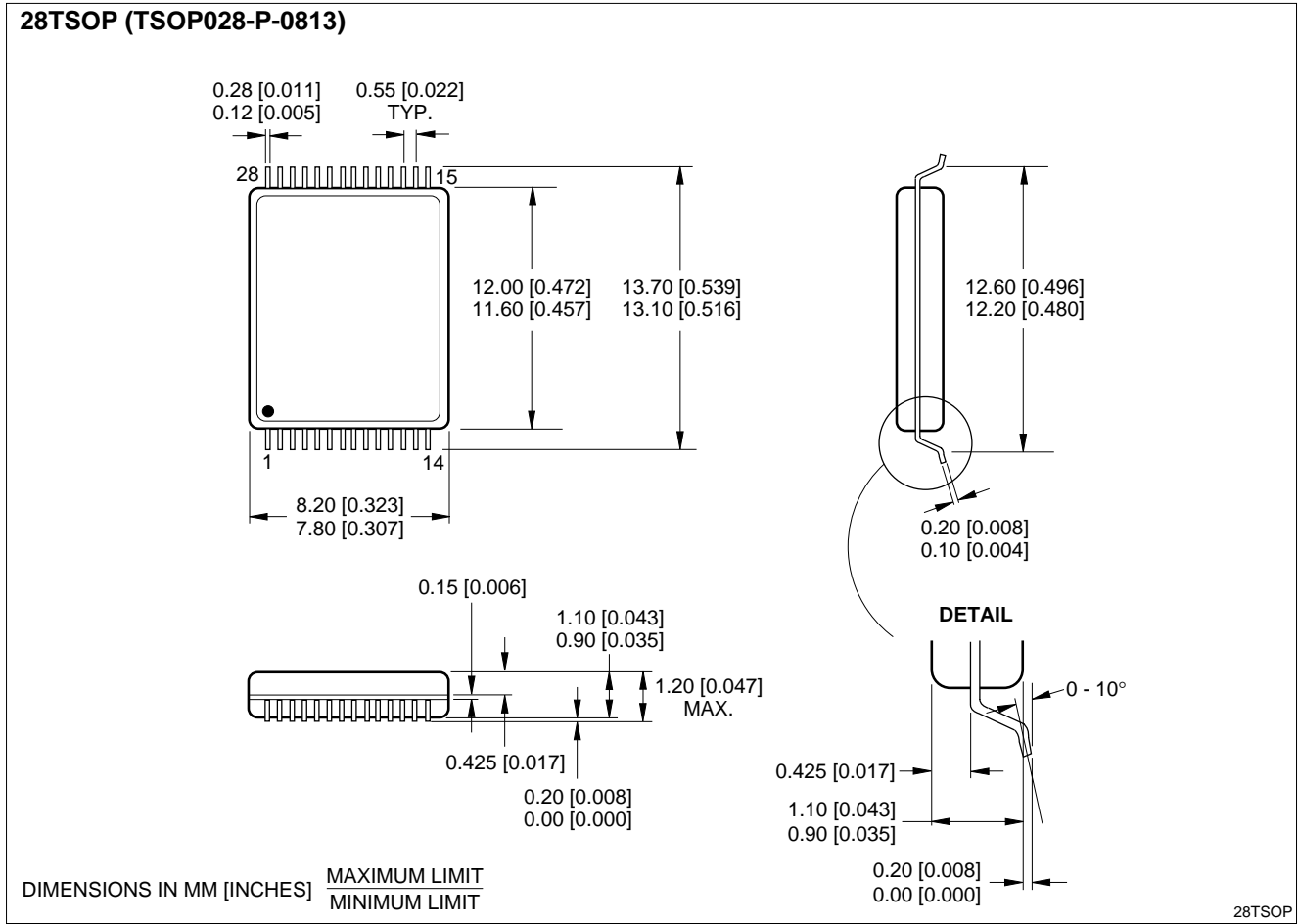
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**Figure 7. Write Cycle ( $\overline{OE}$  Low Fixed)**

PACKAGE DIAGRAMS



28-pin, 450-mil SOP



**28-pin, 8 × 13 mm<sup>2</sup> TSOP (Type I)**

**ORDERING INFORMATION**

