LH51BV1000J

CMOS 1M (128K × 8) Static Ram

FEATURES

- Access time: 70 ns (MAX.)
- Current consumption:
  Operating: 30 mA (MAX.)
  5 mA (MAX.) (t_{RC}, t_{WC} = 1 µs)
  Standby: 60 µA (MAX.)
- Data Retention:
  1.0 µA (MAX.) (V_{CCDR} = 3 V, T_A = 25°C)
- Single power supply: 2.7 V to 3.6 V
- Operating temperature: -25°C to +85°C
- Fully-static operation
- Three-state output
- Not designed or rated as radiation hardened
- Package: 32-pin 6 × 10 mm CSP
- N-type bulk silicon

DESCRIPTION

The LH51BV1000JY is a static RAM organized as 131,072 × 8 bits which provides low power standby mode. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

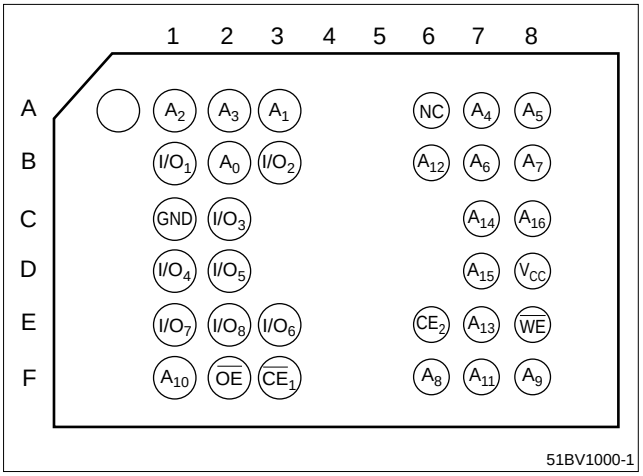


Figure 1. Pin Connections for CSP Package

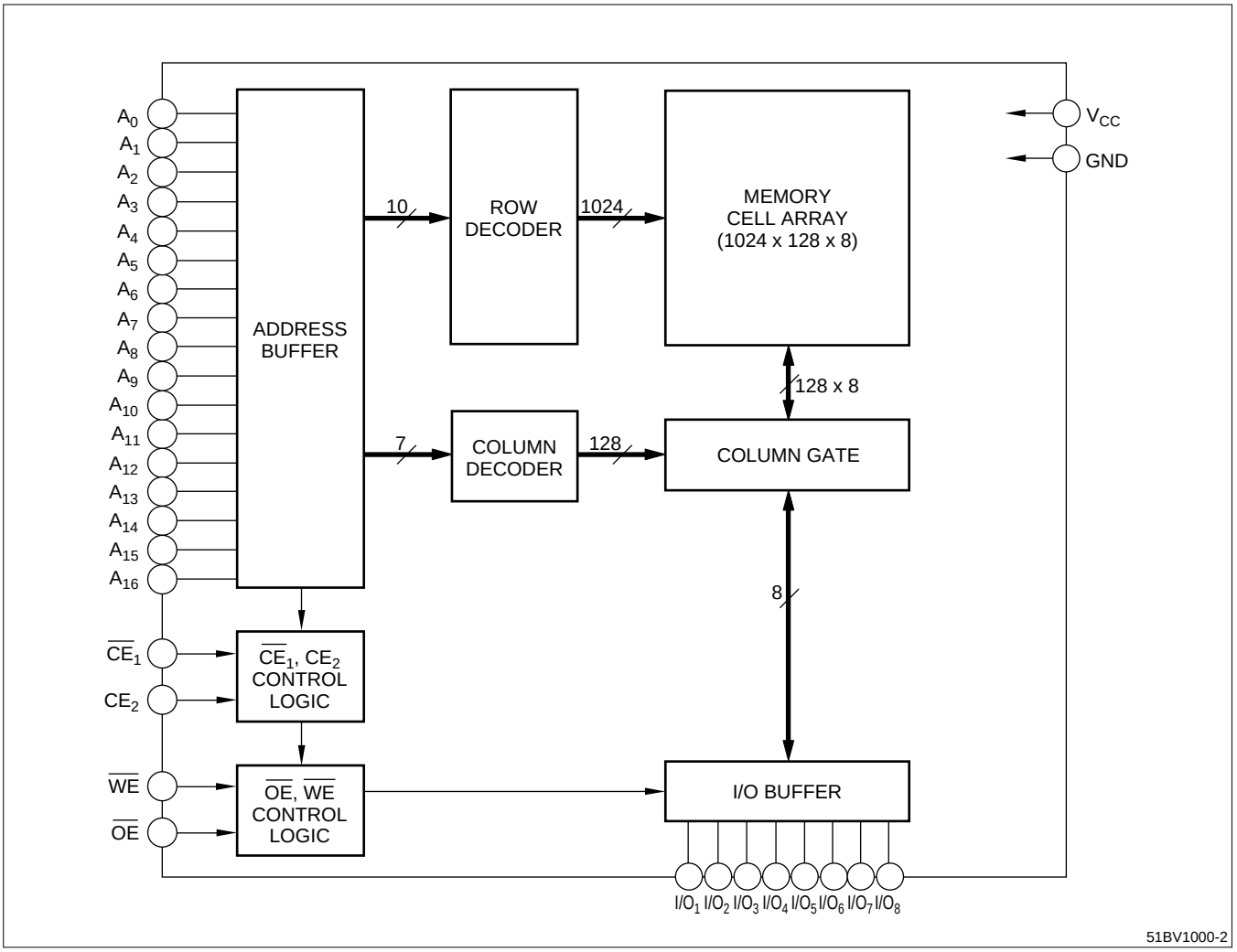


Figure 2. LH51BV1000JY Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
$A_0 - A_{16}$	Address inputs
$\overline{CE_1}$	Chip enable 1
CE_2	Chip enable 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable

SIGNAL	PIN NAME
$I/O_1 - I/O_8$	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	No connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	$I/O_1 - I/O_8$	SUPPLY CURRENT
H	—	—	—	Standby	High impedance	Standby (I_{SB})
—	L	—	—	Standby	High impedance	Standyby (I_{SB})
L	H	L	—	Write	Data input	Active (I_{CC})
L	H	H	L	Read	Data output	Active (I_{CC})
L	H	H	H	Output disable	High impedance	Active (I_{CC})

NOTE:

1. — = Don't care, L = Low, H = High

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	–0.5 to +4.6	V	1
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.3	V	1, 2
Operating temperature	T_{OPR}	–25 to +85	°C	—
Storage temperature	T_{STG}	–65 to +150	°C	—

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.
2. Undershoot of –3.0 V is allowed width of pulse below 50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = -25°C to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	2.7	3.0	3.6	V	—
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	—
	V_{IL}	–0.3	—	0.4	V	1

NOTE:
1. Undershoot of –3.0 V is allowed width of pulse below 50 ns.

DC ELECTRICALCHARACTERISTICS (T_A = -25°C to +85°C, V_{CC} = 2.7 V to 3.6 V)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.[1]	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0	—	1.0	µA
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 V to V_{CC}		–1.0	—	1.0	µA
Operating supply current	I_{CC1}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH} CE_2 = V_{IH}, $I_{I/O}$ = 0 mA	t_{CYCLE} = MIN.	—	—	30	mA
	I_{CC2}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH} CE_2 = V_{IH}, $I_{I/O}$ = 0 mA	t_{CYCLE} = 1.0 µs	—	—	5	
Standby current	I_{SB}	$\overline{CE_1}$, $CE_2 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V		—	0.6	60	µA
	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}		—	—	1.0	mA
Output voltage	V_{OL}	I_{OL} = 2.0 mA, $V_{CC} \geq$ 3 V				0.4	V
		I_{OL} = –0.1 mA		—	—	0.2	
	V_{OH}	I_{OH} = –2.0 mA, $V_{CC} \geq$ 3 V		2.4	—	—	
		I_{OH} = –0.1 mA		V_{CC} – 0.2	—	—	

NOTE:
1 Typical values at V_{CC} = 5.0 V, T_A = 25°C

AC ELECTRICAL CHARACTERISTICS
AC Test Conditions

PARAMETER	MODE	NOTE
Input pulse level	0.4 V to 2.4 V	—
Input rise and fall time	5 ns	—
Input and output timing ref. level	1.5 V	—
Output load	1 TTL + C_L (100 pF)	1

NOTE:
1. Including scope and jig capacitance.

READ CYCLE (T_A = -25°C to +85°C, V_{CC} = 2.7 V to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	70	—	ns	—
Address access time	t_{AA}	—	70	ns	—
$\overline{CE}_1$ access time	t_{ACE1}	—	70	ns	—
CE_2 access time	t_{ACE2}	—	70	ns	—
Output enable to output valid	t_{OE}	—	40	ns	—
Output hold from address change	t_{OH}	10	—	ns	—
$\overline{CE}_1$ Low to output active	t_{LZ1}	5	—	ns	1
CE_2 High to output active	t_{LZ2}	5	—	ns	1
$\overline{OE}$ Low to output active	t_{OLZ}	0	—	ns	1
$\overline{CE}_1$ High to output in High impedance	t_{HZ1}	—	30	ns	1
CE_2 Low to output in High impedance	t_{HZ2}	—	30	ns	1
$\overline{OE}$ High to output in High impedance	t_{OHZ}	—	30	ns	1

NOTE:
1. Active output to High impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

WRITE CYCLE (T_A = -25°C to +85°C, V_{CC} = 2.7 V to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	70	—	ns	—
Chip enable to end of write	t_{CW}	60	—	ns	—
Address valid to end of write	t_{AW}	60	—	ns	—
Address setup time	t_{AS}	0	—	ns	—
Write pulse width	t_{WP}	55	—	ns	—
Write recovery time	t_{WR}	0	—	ns	—
Input data setup time	t_{DW}	30	—	ns	—
Input data hold time	t_{DH}	0	—	ns	—
$\overline{WE}$ High to output active	t_{OW}	5	—	ns	1
$\overline{WE}$ Low to output in High impedance	t_{WZ}	—	30	ns	1
$\overline{OE}$ High to output in High impedance	t_{OHZ}	—	30	ns	1

NOTE:
1. Active output to High impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

DATA RETENTION CHARACTERISTICS (T_A = -25°C to +850°C)

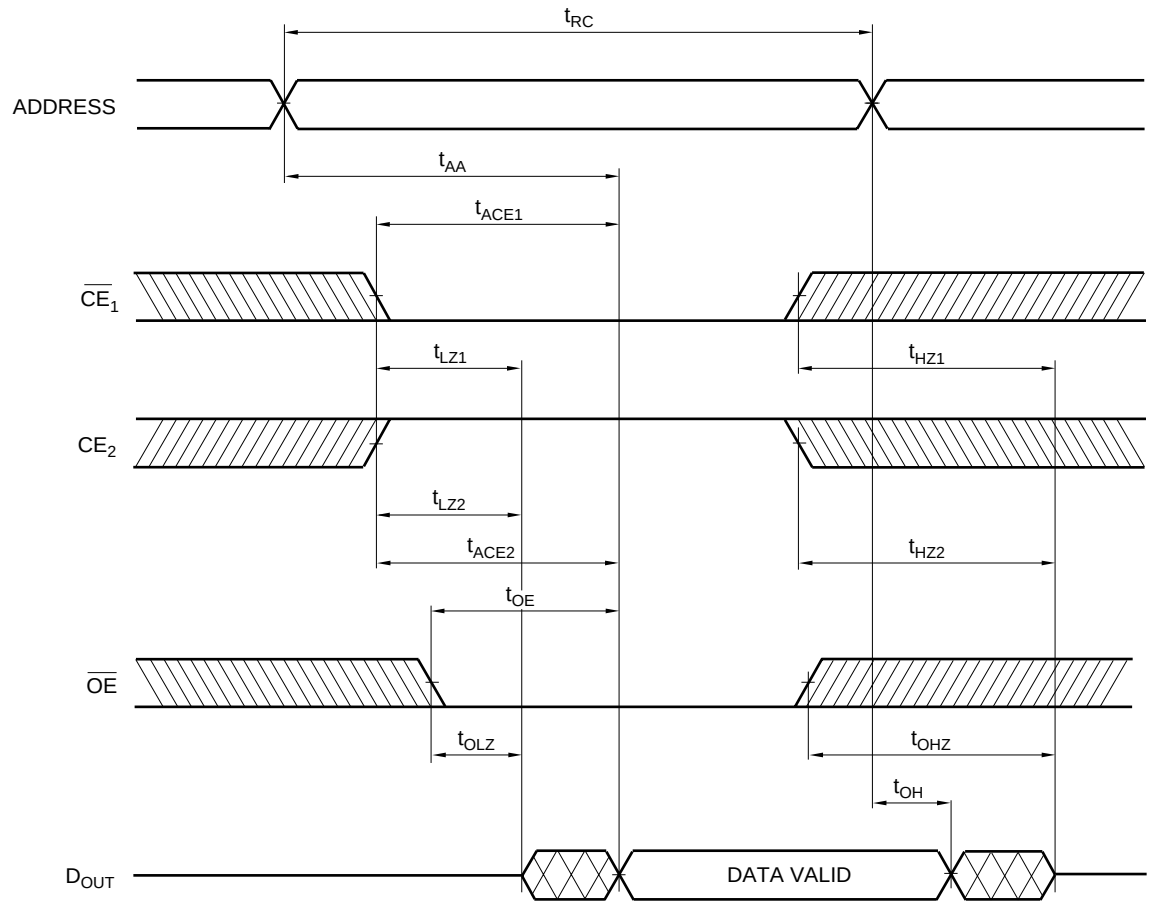
PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.[1]	MAX.	UNIT	NOTES
Data retention supply voltage	V_{CCDR}	$\overline{CE_2} \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V		2.0	—	3.6	V	2
Data retention supply current	I_{CCDR}	V_{CCDR} = 3 V $\overline{CE_2} \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V	T_A = 25°C	—	0.5	1.0	µA	—
			T_A = 40°C	—	—	3.0	—	—
				—	—	50	µA	2
Chip enable setup time	t_{CDR}	—		0	—	—	ms	—
Chip enable hold time	t_R	—		5	—	—	ms	—

NOTES:
1. Typical value at T_A = 25°C
2. $\overline{CE_2} \ge V_{CCDR}$ - 0.2 V or $\overline{CE_2} \le 0.2$ V

PIN CAPACITANCE (T_A = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	V_{IN} = 0 V	—	—	8	pF	1
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	—	10	pF	1

NOTE:
1. This parameter is sampled and not production tested.



NOTE: $\overline{WE}$ is HIGH for Read cycle.

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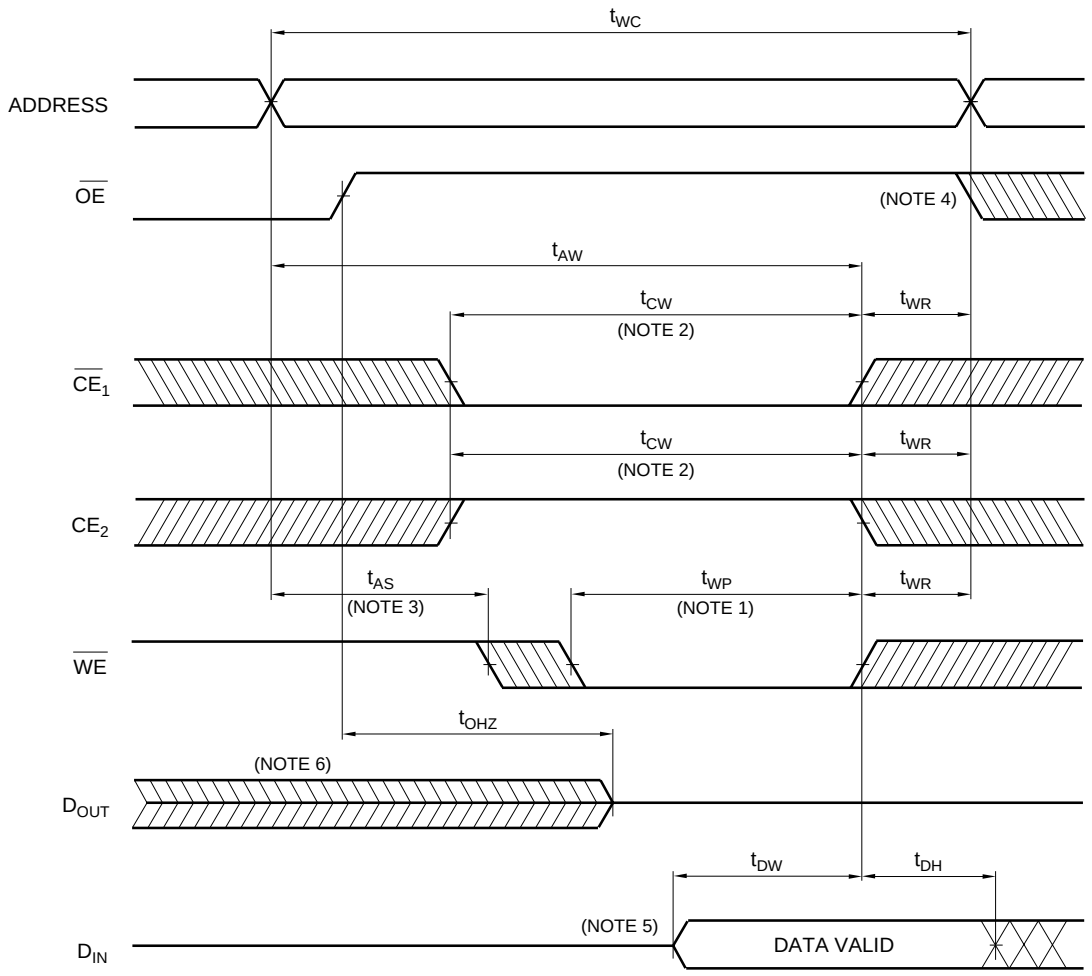
Figure 3. Read Cycle



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CE_1}$, a HIGH CE_2 and a LOW $\overline{WE}$, A write begins at the latest transition among $\overline{CE_1}$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW. A write ends at the earliest transition among $\overline{CE_1}$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the latter of $\overline{CE_1}$ going LOW or CE_2 going HIGH to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CE_1}$ or $\overline{WE}$ going HIGH. t_{WR2} applies in case a write ends at CE_2 going LOW.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CE_1}$ goes LOW simultaneously with $\overline{WE}$ going LOW or after $\overline{WE}$ going LOW, the outputs remain in high impedance state.
7. If $\overline{CE_1}$ goes HIGH simulaneously with $\overline{WE}$ going HIGH or before $\overline{WE}$ going HIGH, the outputs remain in high impedance state.

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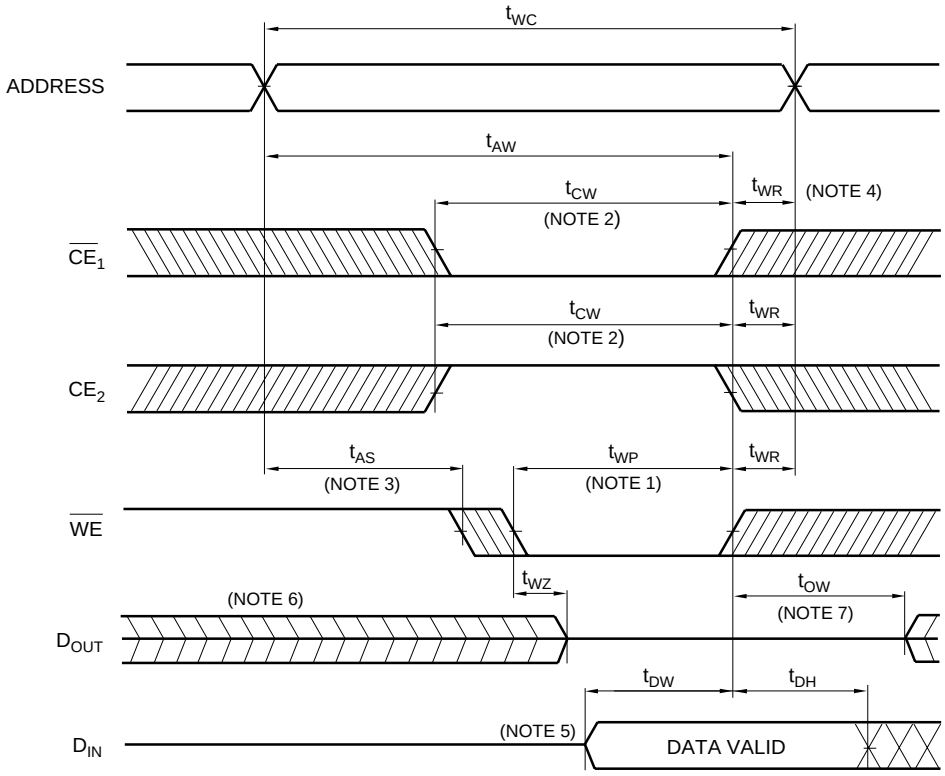
Figure 4. Write Cycle ($\overline{OE}$ Controlled)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CE_1}$, a HIGH CE_2 and a LOW $\overline{WE}$, A write begins at the latest transition among $\overline{CE_1}$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW. A write ends at the earliest transition among $\overline{CE_1}$ going HIGH. CE_2 going LOW and $\overline{WE}$ going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the latter of $\overline{CE_1}$ going LOW or CE_2 going HIGH to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CE_1}$ or $\overline{WE}$ going HIGH. t_{WR2} applies in case a write ends at CE_2 going LOW.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CE_1}$ goes LOW simultaneously with $\overline{WE}$ going LOW or after $\overline{WE}$ going LOW, the outputs remain in high impedance state.
7. If $\overline{CE_1}$ goes HIGH simulaneously with $\overline{WE}$ going HIGH or before $\overline{WE}$ going HIGH, the outputs remain in high impedance state.

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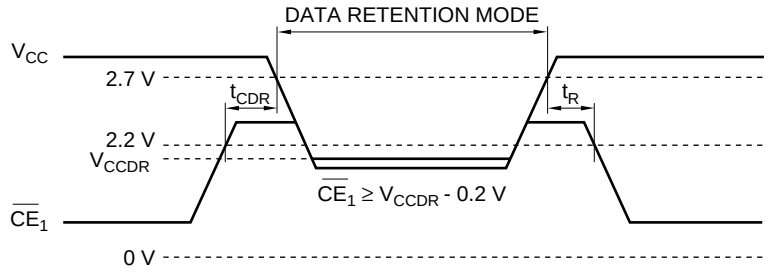
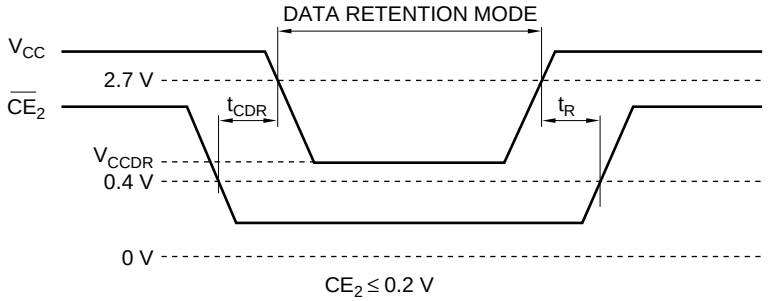
Figure 5. Write Cycle ($\overline{OE}$ Low Fixed)

$\overline{CE_1}$ CONTROL (NOTE)



CE_2 CONTROL



NOTE: To control the data retention mode at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} and V_{CCDR} - 0.2 V or 0 V and 0.2 V during the data retention mode.

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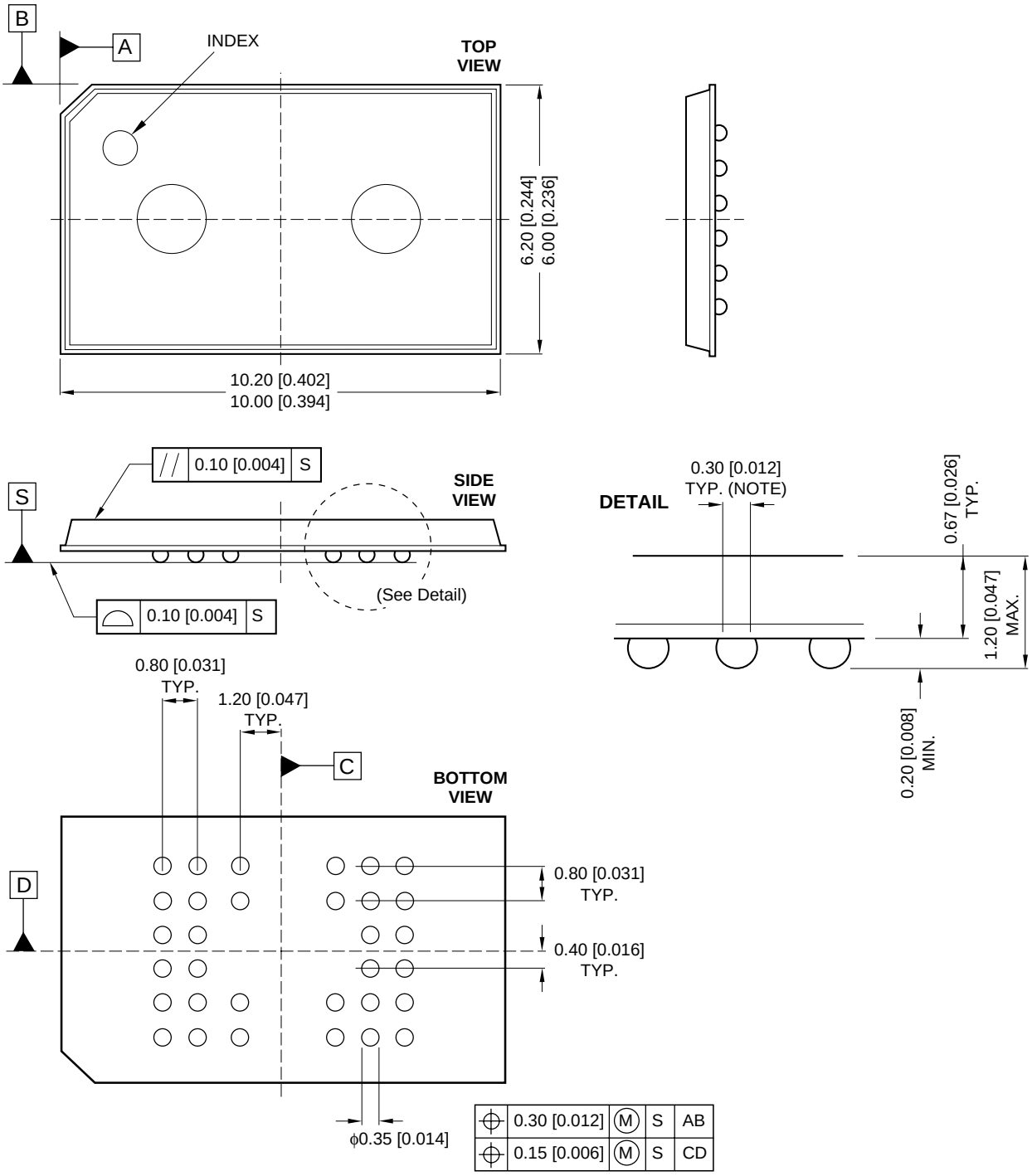
Figure 6. Data Retention Chart ($\overline{CE_1}$ Controlled)

PACKAGE DIAGRAM

32CSP (FBGA032-P-0610)

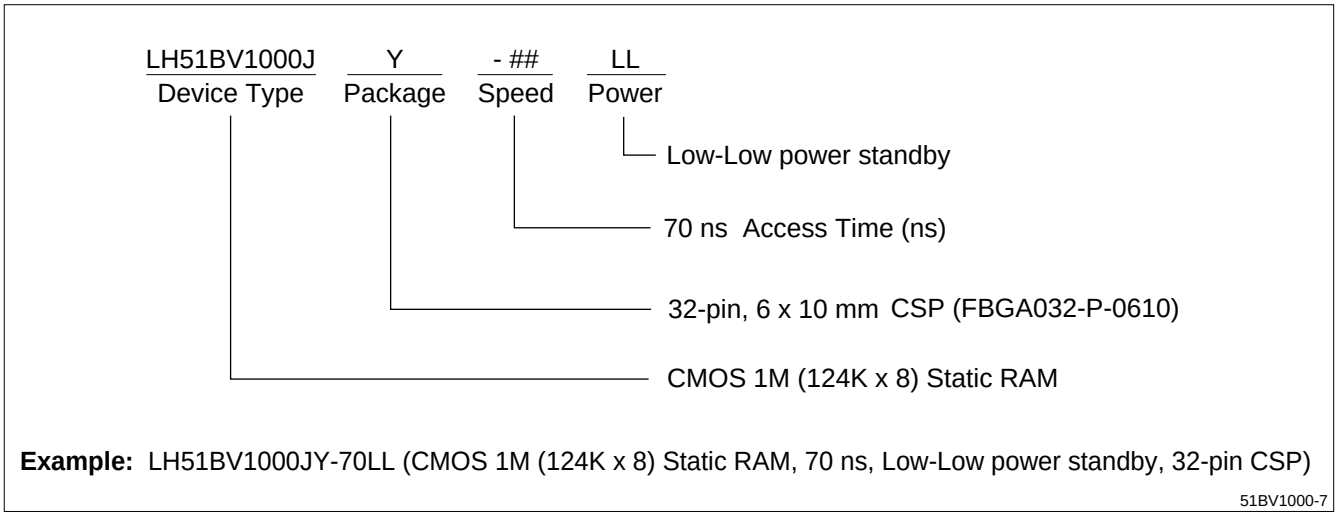


NOTE: Land hole diameter for ball mounting.

DIMENSIONS IN MM [INCHES] $\frac{\text{MAXIMUM LIMIT}}{\text{MINIMUM LIMIT}}$

32CSP

ORDERING INFORMATION



Example: LH51BV1000JY-70LL (CMOS 1M (124K x 8) Static RAM, 70 ns, Low-Low power standby, 32-pin CSP)

51BV1000-7