LH52256AS

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time: 500 ns (MAX.)
- Supply current:
  Operating: 36 mW (MAX.)
  18 mW (t_{RC}, t_{WC} = 1 µs (TYP.))
  Standby: 72 µW (MAX.)
- Low voltage operation: 2.5 V to 3.6 V
- Fully-static operation
- Three-state outputs
- Packages:
  28-pin, 450-mil SOP
  28-pin, 8 × 13 mm^2 TSOP (Type I)

DESCRIPTION

The LH52256AS is a static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

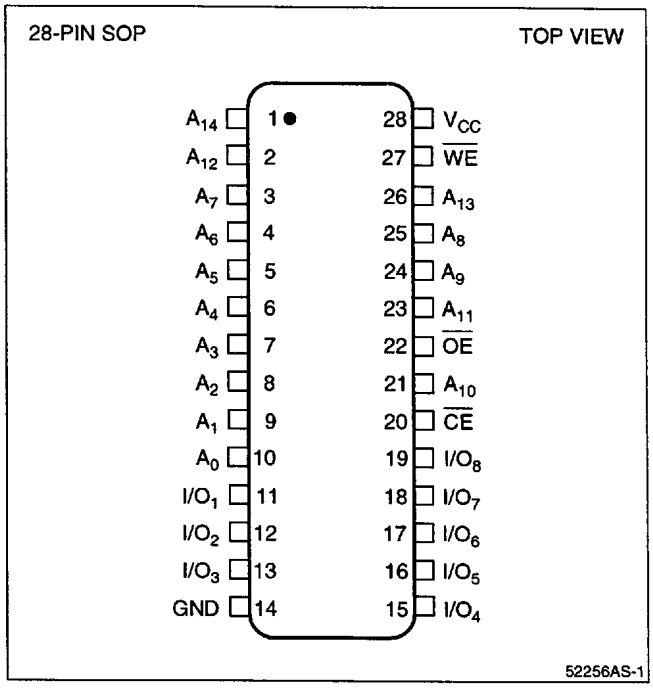


Figure 1. Pin Connections for SOP Package

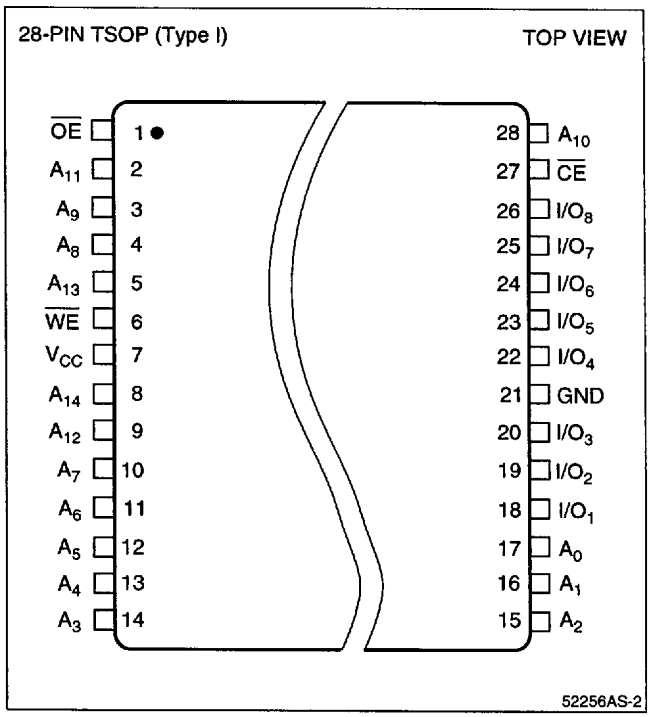


Figure 2. Pin Connections for TSOP Package

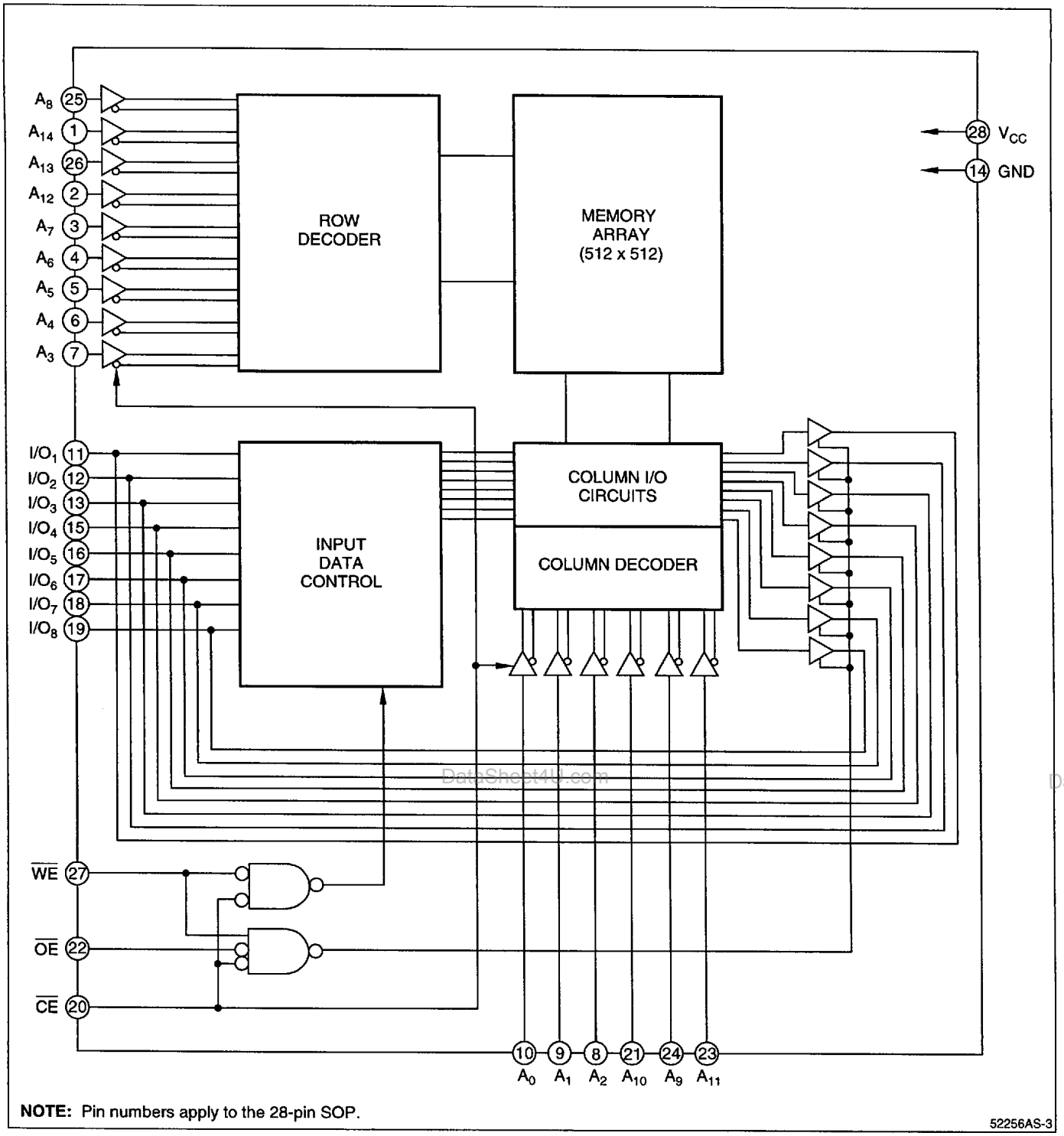


Figure 3. LH52256AS Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address inputs
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Standby	High-Z	Standby (I_{SB})	1
L	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	−0.3 to +7.0	V	1
Input voltage	V_{IN}	−0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	Topr	−10 to +70	°C	
Storage temperature	Tstg	−65 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. V_{IN} (MIN.) = −3.0 V for pulse width ≤50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = −10°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	2.5		3.6	V	
Input voltage	V_{IH}	V_{CC} − 0.5		V_{CC} + 0.3	V	
	V_{IL}	−0.3		0.2	V	1

NOTE:
1. V_{IN} (MIN.) = −3.0 V for pulse width ≤50 ns.

DC CHARACTERISTICS (T_A = –10°C to +70°C, V_{CC} = 2.5 V to 3.6 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0	1.0	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 V to V_{CC}	–1.0	1.0	µA
Operating supply current	I_{CC}	Minimum cycle, V_{IN} = V_{IL} or V_{IH} $I_{I/O}$ = 0 mA, $\overline{CE}$ = V_{IL}		10	mA
		t_{RC}, t_{WC} = 1 µs, V_{IN} = V_{IL} or V_{IH}, $I_{I/O}$ = 0 mA, $\overline{CE}$ = V_{IL}		5	
Standby supply current	I_{SB}	$\overline{CE}$ ≥ V_{CC} – 0.2 V		20	µA
	I_{SB1}	$\overline{CE}$ = V_{IH}		0.4	mA
Output voltage	V_{OL}	I_{OL} = 0.5 mA		0.5	V
	V_{OH}	I_{OH} = –0.5 mA	V_{CC} – 0.5		

READ CYCLE (T_A = –10°C to +70°C, V_{CC} = 2.5 V to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	500		ns	
Address access time	t_{AA}		500	ns	
Chip enable access time	t_{ACE}		500	ns	
Output enable access time	t_{OE}		250	ns	
Output hold time	t_{OH}	20		ns	
$\overline{CE}$ Low to output in Low-Z	t_{LZ}	10		ns	1
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	10		ns	1
$\overline{CE}$ High to output in High-Z	t_{HZ}	0	60	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	60	ns	1

NOTES:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

WRITE CYCLE (T_A = –10°C to +70°C, V_{CC} = 2.5 V to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	500		ns	
$\overline{CE}$ Low to end of write	t_{CW}	350		ns	
Address valid to end of write	t_{AW}	350		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	250		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	150		ns	
Input data hold time	t_{DH}	0		ns	
$\overline{WE}$ High to output in Low-Z	t_{OW}	10		ns	1
$\overline{WE}$ Low to output in High-Z	t_{WZ}	0	60	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	60	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

TEST CONDITIONS

PARAMETER	MODE	NOTE
Input pulse levels	0 V to V_{CC}	
Input rise/fall times	10 ns	
Input/output timing levels	1.5 V	
Output load	C_L (100 pF)	1

NOTE:
1. Includes scope and jig capacitance.

CAPACITANCE (T_A = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF	1
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF	1

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = –10°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR} - 0.2$ V	2.0	3.6	V	
Data retention supply current	I_{CCDR}	V_{CCDR} = 3.0 V $\overline{CE} \geq V_{CCDR} - 0.2$ V		20	µA	
Chip enable setup time	t_{CDR}		0		ns	
Chip enable hold time	t_R		t_{RC}		ns	1

NOTE:
1. t_{RC} = Read cycle time.

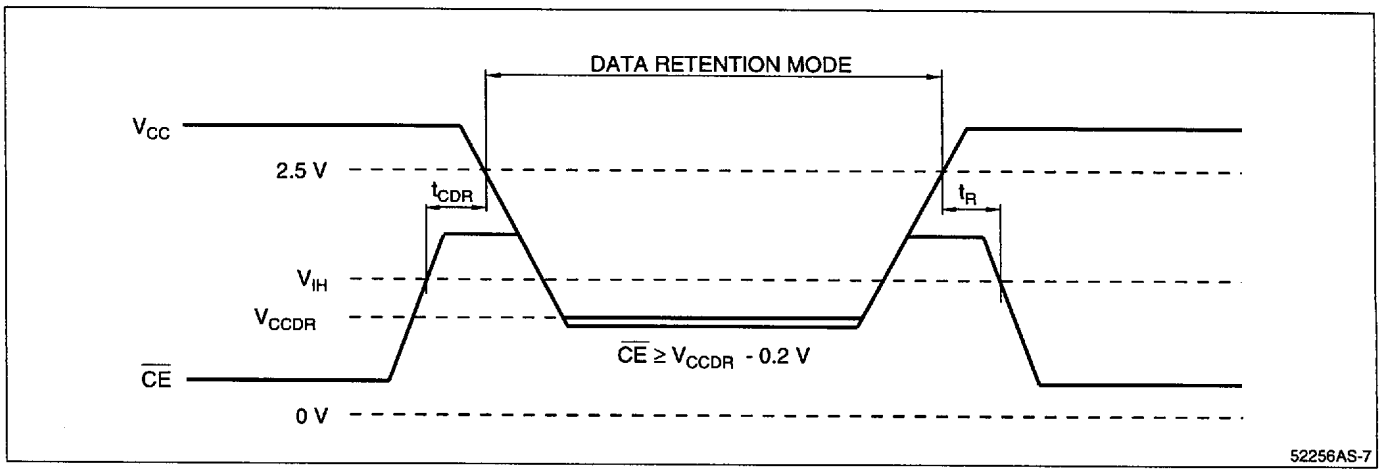


Figure 4. Low Voltage Data Retention

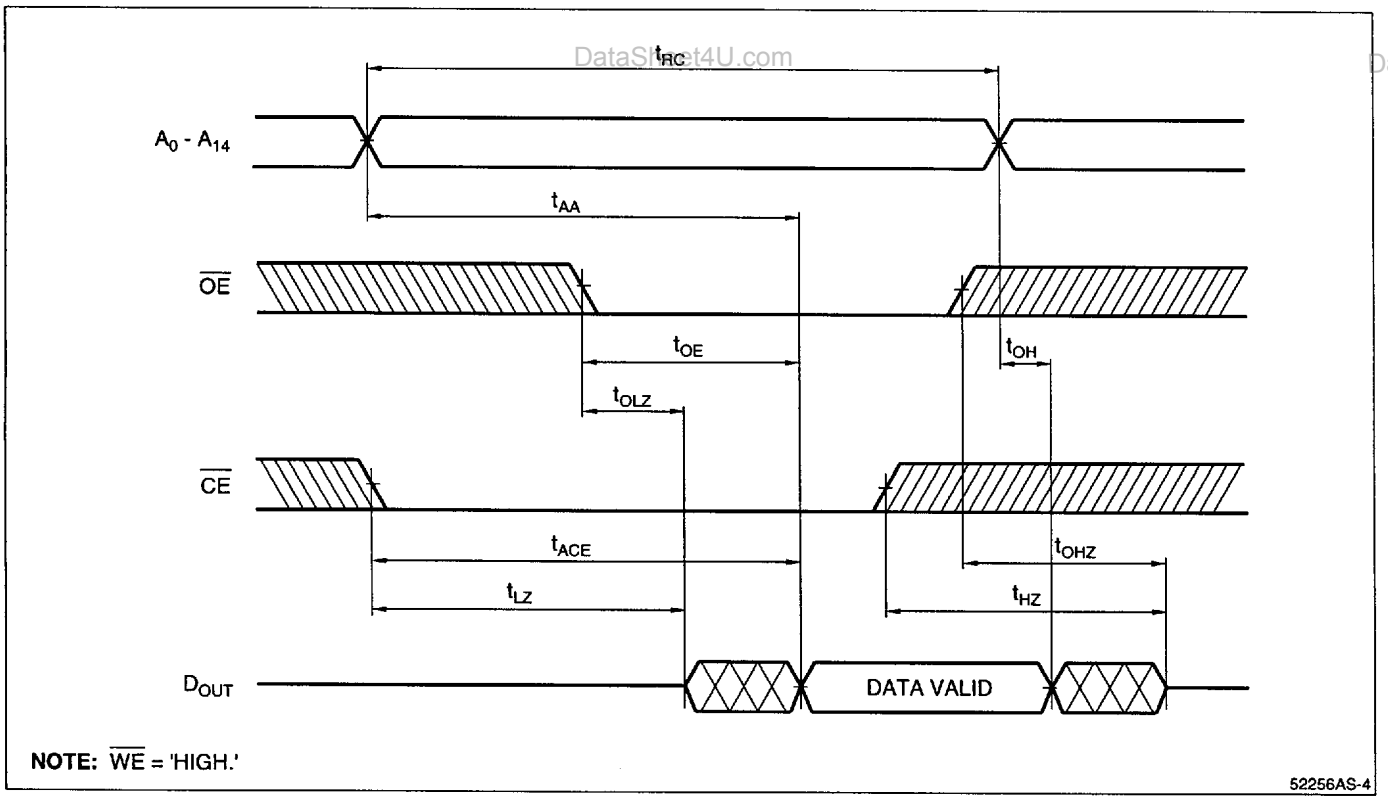
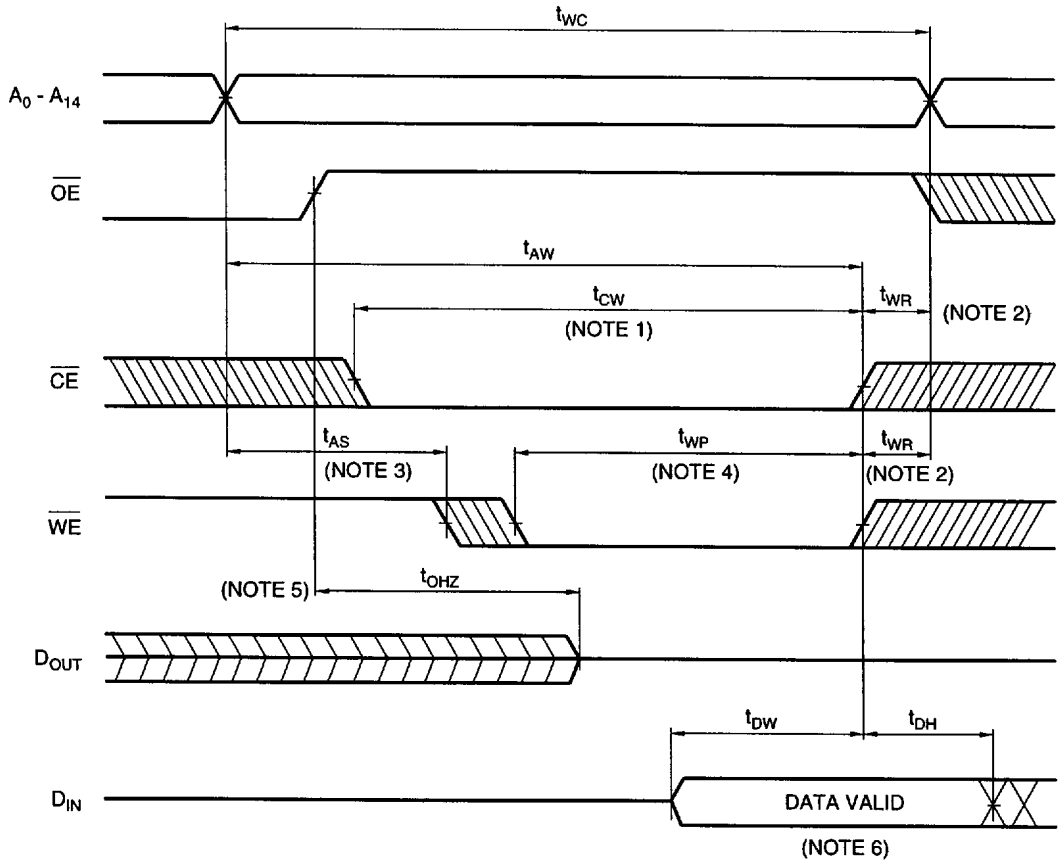


Figure 5. Read Cycle



NOTES:

1. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
2. t_{WR} is defined as the time from the end of writing to address change.
3. t_{AS} is defined as the time from address change to the start of writing.
4. The writing occurs during an overlapping period of $\overline{CE}$ = 'LOW,' and $\overline{WE}$ = 'LOW' (t_{WP}).
5. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
6. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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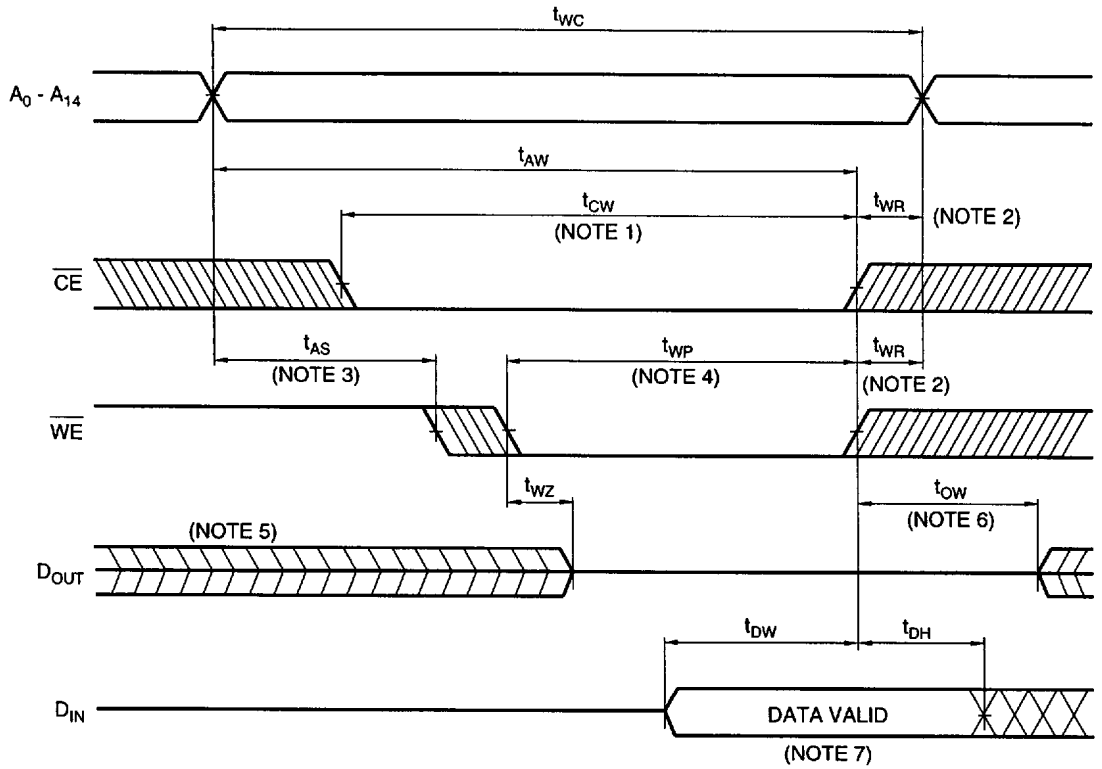
Figure 6. Write Cycle ($\overline{OE}$ Controlled)



NOTES:

1. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
2. t_{WR} is defined as the time from the end of writing to address change.
3. t_{AS} is defined as the time from address change to the start of writing.
4. The writing occurs during an overlapping period of $\overline{CE}$ = 'LOW,' and $\overline{WE}$ = 'LOW' (t_{WP}).
5. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
6. If $\overline{CE}$ HIGH transition occurs at the same time or before $\overline{WE}$ HIGH transition, the outputs will remain high-impedance.
7. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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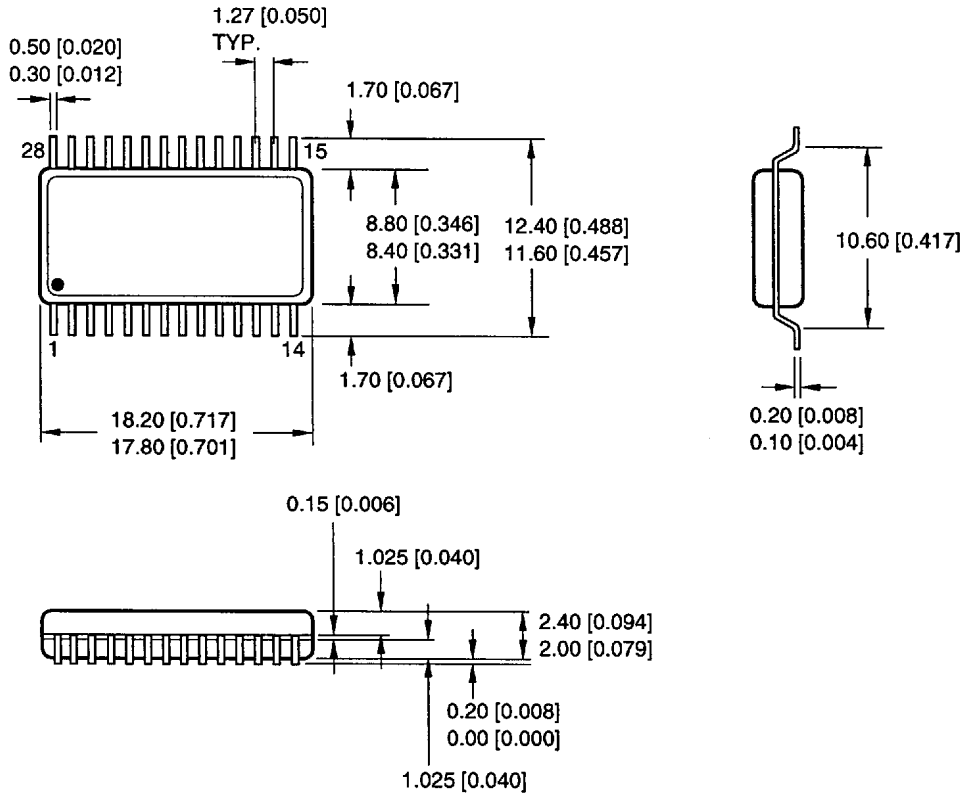
Figure 7. Write Cycle ($\overline{OE}$ Low Fixed)

PACKAGE DIAGRAMS

28SOP (SOP028-P-0450)

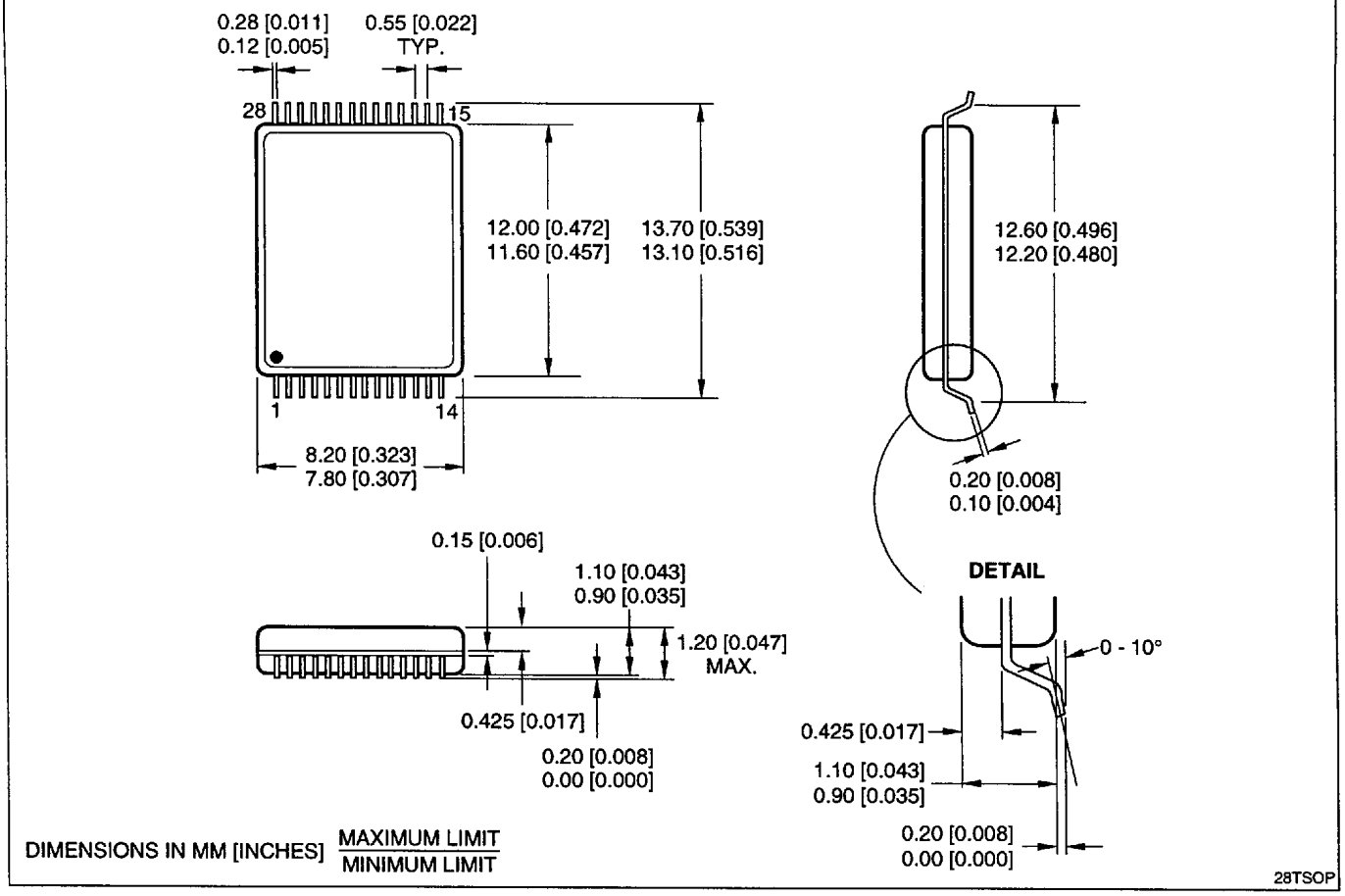


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOP

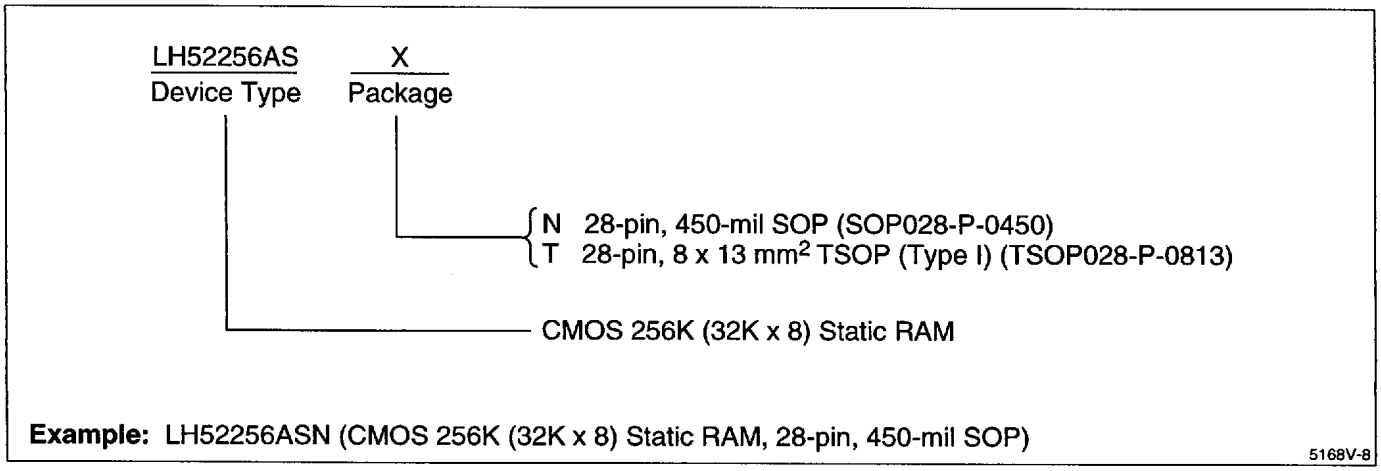
28-pin, 450-mil SOP

28TSOP (TSOP028-P-0813)



28-pin, 8 × 13 mm² TSOP (Type I)

ORDERING INFORMATION



Example: LH52256ASN (CMOS 256K (32K x 8) Static RAM, 28-pin, 450-mil SOP)

5168V-8