LH531000B-S

CMOS 1M (128K × 8) 3 V-Drive MROM

FEATURES

- 131,072 words × 8 bit organization
- Access time: 500 ns (MAX.)
- Power consumption:
  Operating: 64.8 mW (MAX.)
  Standby: 108 µW (MAX.)
- Mask-programmable control pin:
  Pin 20 = $\overline{CE}/OE/\overline{OE}$
- Static operation
- Three-state outputs
- Low power supply: 2.6 V to 3.6 V
- Package: 28-pin, 450-mil SOP

DESCRIPTION

The LH531000B-S is a mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

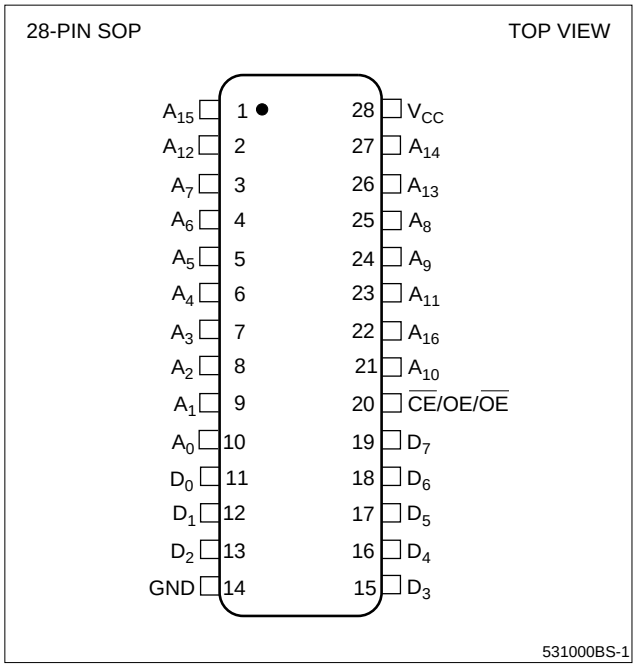


Figure 1. Pin Connections for DIP Package

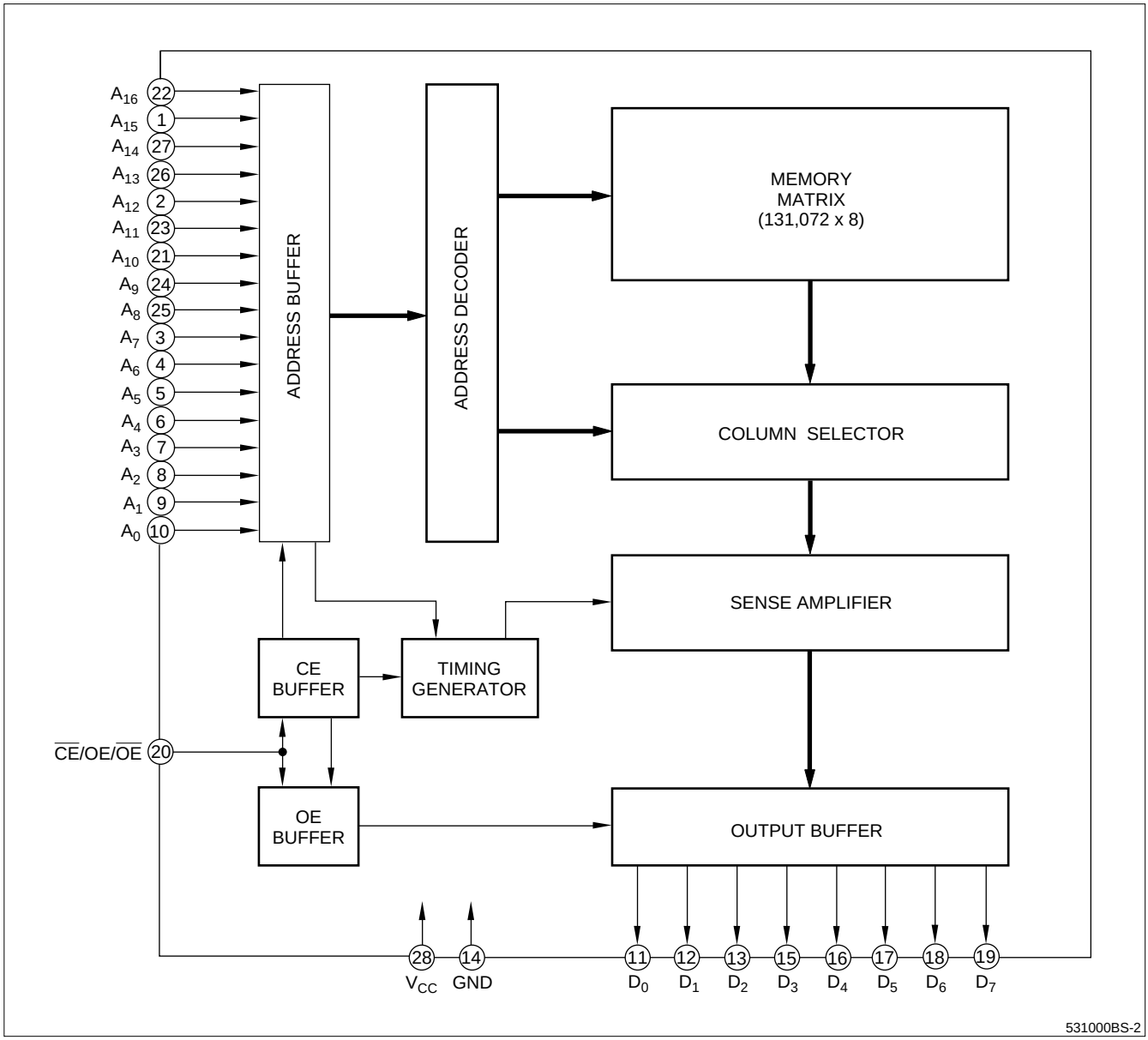


Figure 2. LH531000B-S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
$A_0 – A_{16}$	Address input	
$D_0 – D_7$	Data output	
$\overline{CE}/OE/\overline{OE}$	Chip Enable input or Output Enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (2.6 V to 3.6 V)	
GND	Ground	

NOTE:
1. Active level of $\overline{CE}/OE/\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	SUPPLY CURRENT
H	–	High-Z	Standby
L	–	Output	Operating
–	L/H	High-Z	Operating
–	H/L	Output	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		3.6	V

DC CHARACTERISTICS (V_{CC} = 2.6 V to 3.6 V, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		–0.3		0.4	V	
Input 'High' voltage	V_{IH}		0.8 × V_{CC}		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = –100 µA	0.8 × V_{CC}			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC}	t_{RC} = 500 ns			18	mA	2
Standby current	I_{SB}	$\overline{CE}$ = V_{CC} – 0.2 V			30	µA	
Input capacitance	C_{IN}	f = 1 MHz T_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTE:
1. $\overline{CE}$/$\overline{OE}$ = V_{IH}, OE = V_{IL}
2. Outputs open

AC CHARACTERISTICS (V_{CC} = 2.6 V to 3.6 V, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	500		ns	
Address access time	t_{AA}		500	ns	
Chip enable access time	t_{ACE}		500	ns	
Output enable delay time	t_{OE}		200	ns	
Output hold time	t_{OH}	10		ns	
CE to output in High-Z	t_{CHZ}		150	ns	1
OE to output in High-Z	t_{OHZ}			ns	

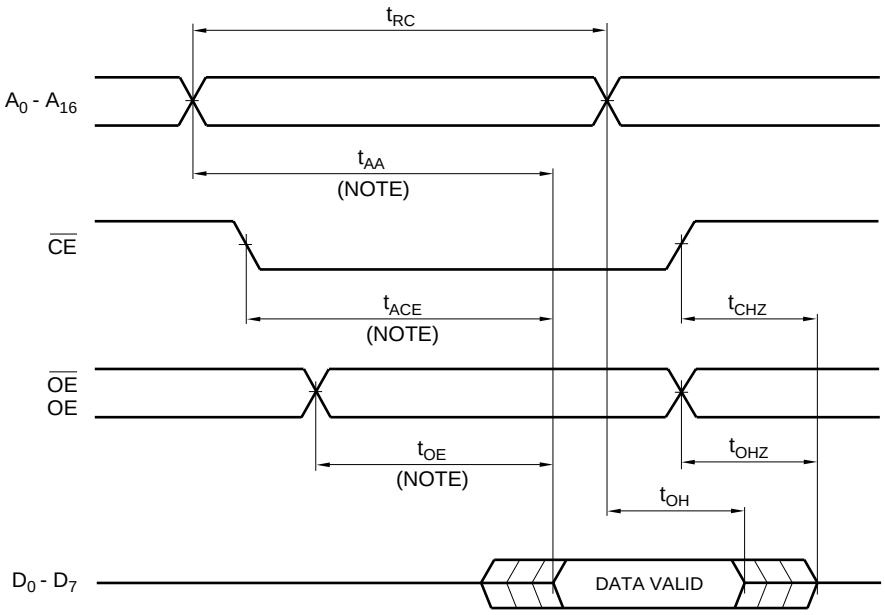
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to (0.8 × V_{CC}) V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



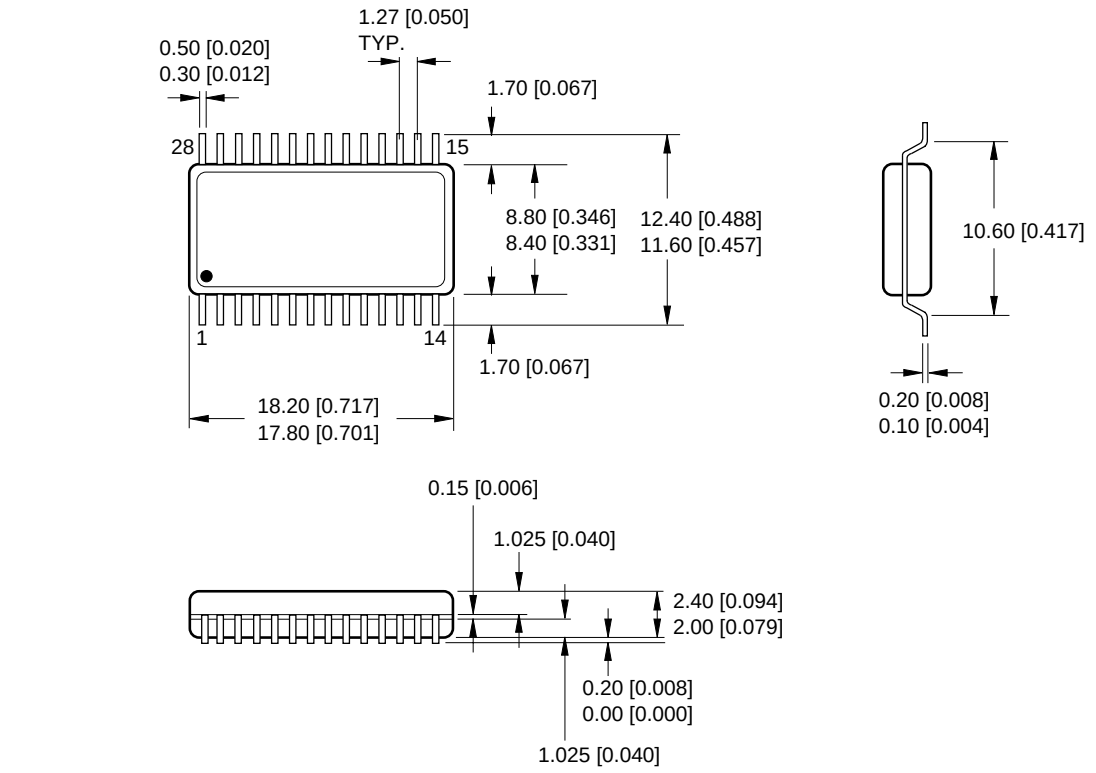
NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

531000BS-3

Figure 3. Timing Diagram

PACKAGE DIAGRAM

28SOP (SOP028-P-0450)



28-pin, 450-mil SOP

ORDERING INFORMATION