

# LH531V00

CMOS 1M (128K × 8) MROM

## FEATURES

- 131,072 words × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
  - Operating: 275 mW (MAX.)
  - Standby: 550 μW (MAX.)
- Mask-programmable OE<sub>1</sub>/OE<sub>1</sub>/DC
- Fully-static operation
- TTL-compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  - 32-pin, 600-mil DIP
  - 32-pin, 525-mil SOP
  - 32-pin, 8 × 20 mm<sup>2</sup> TSOP (Type I)

## DESCRIPTION

The LH531V00 is a 1M-bit mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

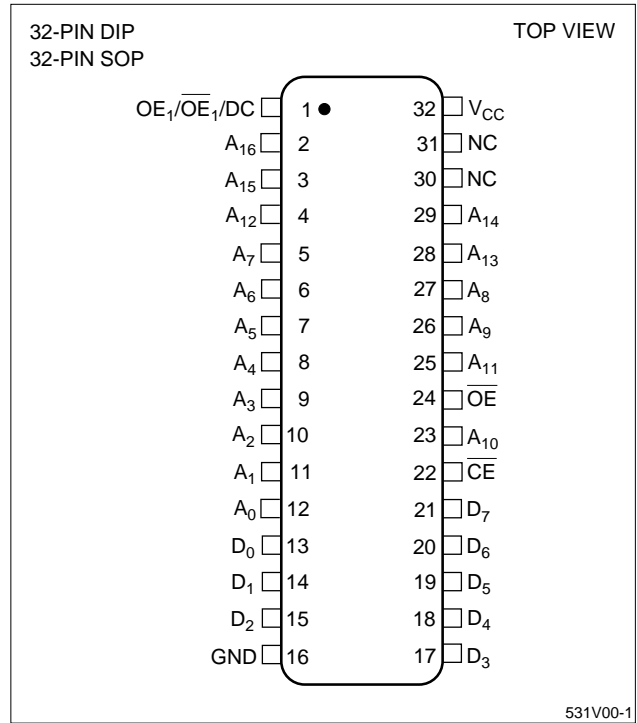


Figure 1. Pin Connections for DIP and SOP Packages

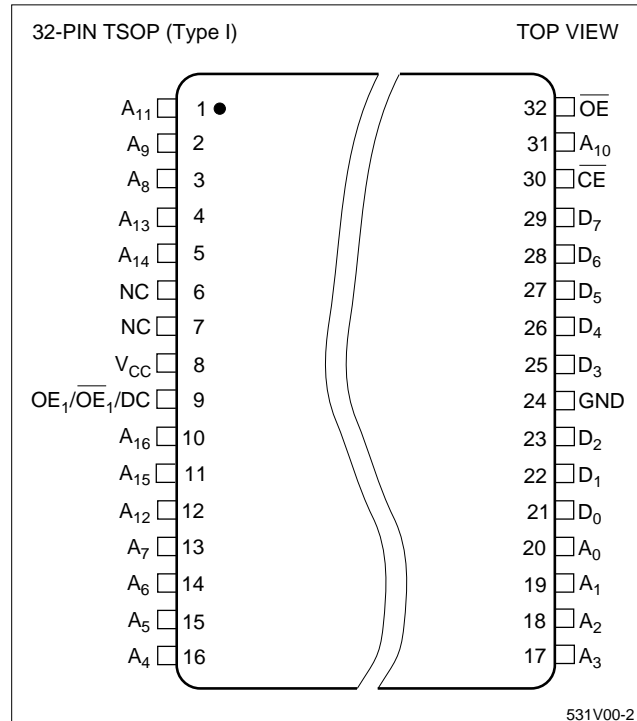


Figure 2. Pin Connections for TSOP Package

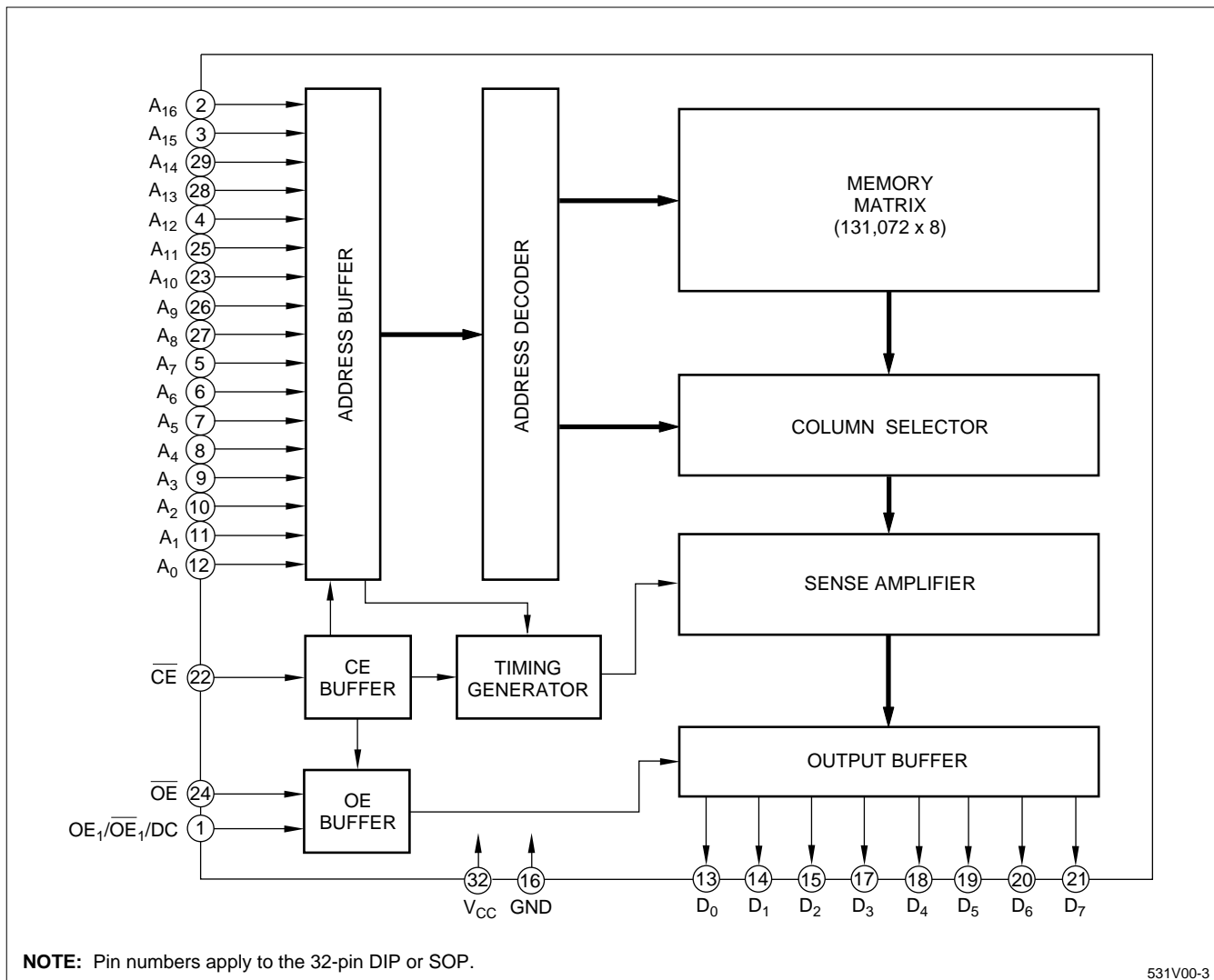


Figure 3. LH531V00 Block Diagram

## PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A <sub>0</sub> – A <sub>16</sub>	Address input	
D <sub>0</sub> – D <sub>7</sub>	Data output	
CE	Chip Enable input	
OE	Output Enable input	

SIGNAL	PIN NAME	NOTE
OE <sub>1</sub> /OE <sub>1</sub> /DC	Output Enable input	1
V <sub>CC</sub>	Power supply (+5 V)	
GND	Ground	

**NOTE:**

- Active level of OE<sub>1</sub>/OE<sub>1</sub>/DC is mask-programmable. When DC is selected out of OE<sub>1</sub>/OE<sub>1</sub>/DC, it is fixed to an active level. Then it is recommended to apply either HIGH or LOW to the DC pin.

## TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$OE_1/\overline{OE}_1$	D <sub>0</sub> – D <sub>7</sub>	SUPPLY CURRENT	NOTE
H	X	X	High-Z	Standby (I <sub>SB</sub> )	1
L	H	X	High-Z	Operating (I <sub>CC</sub> )	1
L	X	L/H	High-Z	Operating (I <sub>CC</sub> )	1
L	L	H/L	D <sub>0</sub> – D <sub>7</sub>	Operating (I <sub>CC</sub> )	

## NOTE:

1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V <sub>CC</sub>	–0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	–0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>OUT</sub>	–0.3 to V <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V

DC CHARACTERISTICS (V<sub>CC</sub> = 5 V ±10%, T<sub>A</sub> = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V <sub>IL</sub>		–0.3		0.8	V	
Input 'High' voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> + 0.3	V	
Output 'Low' voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA			0.4	V	
Output 'High' voltage	V <sub>OH</sub>	I <sub>OH</sub> = –400 μA	2.4			V	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>			10	μA	
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>			10	μA	1
Operating current	I <sub>CC1</sub>	t <sub>RC</sub> = 100 ns			50	mA	2
	I <sub>CC2</sub>	t <sub>RC</sub> = 1 μs			45	mA	
	I <sub>CC3</sub>	t <sub>RC</sub> = 100 ns			45	mA	3
	I <sub>CC4</sub>	t <sub>RC</sub> = 1 μs			40	mA	
Standby current	I <sub>SB1</sub>	CE = V <sub>IH</sub>			3	mA	
	I <sub>SB2</sub>	CE = V <sub>CC</sub> – 0.2 V			100	μA	
Input capacitance	C <sub>IN</sub>	f = 1 MHz			10	pF	
Output capacitance	C <sub>OUT</sub>	T <sub>A</sub> = 25°C			10	pF	

## NOTES:

1.  $\overline{CE}/\overline{OE} = V_{IH}$
2. V<sub>IN</sub> = V<sub>IH</sub> or V<sub>IL</sub>, CE = V<sub>IL</sub>, outputs open
3. V<sub>IN</sub> = (V<sub>CC</sub> – 0.2 V) or 0.2 V, CE = 0.2 V, outputs open

**AC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	100			ns	
Address access time	$t_{AA}$			100	ns	
Chip enable access time	$t_{ACE}$			100	ns	
Output enable delay time	$t_{OE}$			50	ns	
Output hold time	$t_{OH}$	0			ns	
CE to output in High-Z	$t_{CHZ}$			50	ns	1
OE to output in High-Z	$t_{OHZ}$			50	ns	

**NOTE:**

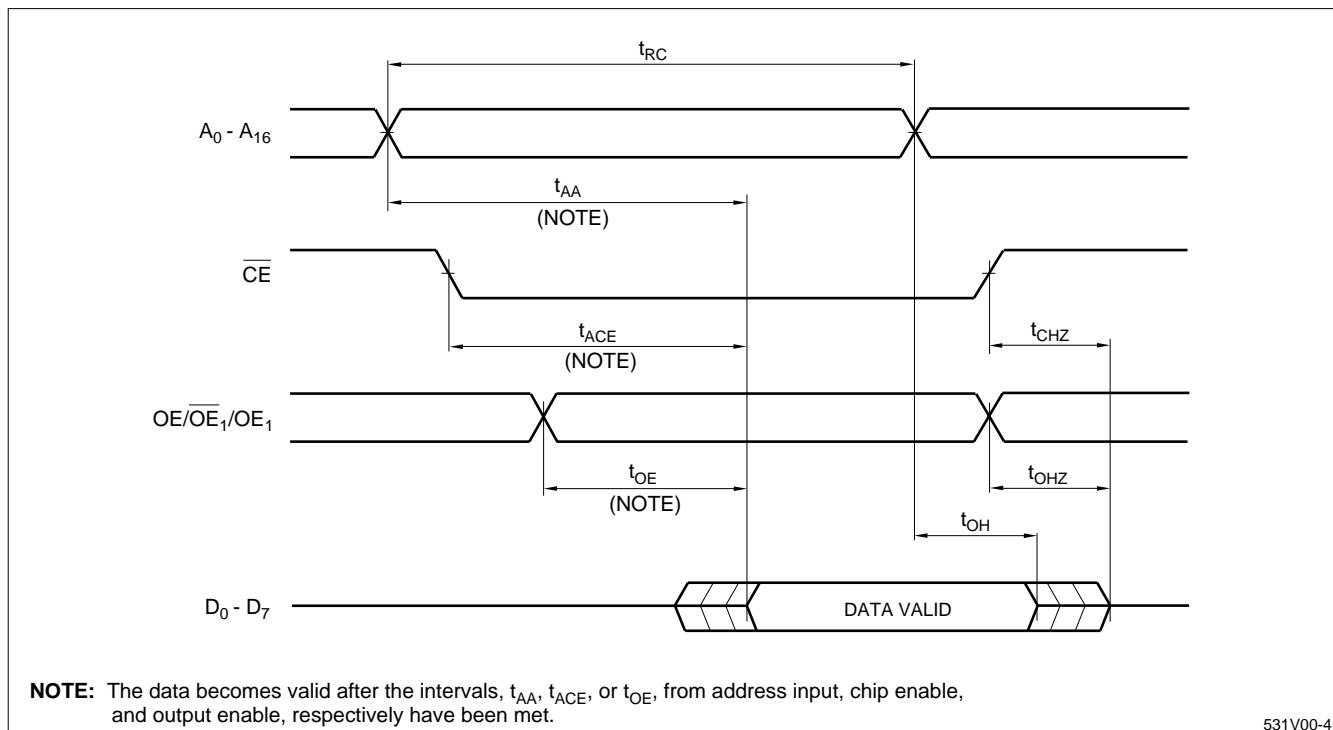
1. This is the time required for the outputs to become high-impedance.

**AC TEST CONDITIONS**

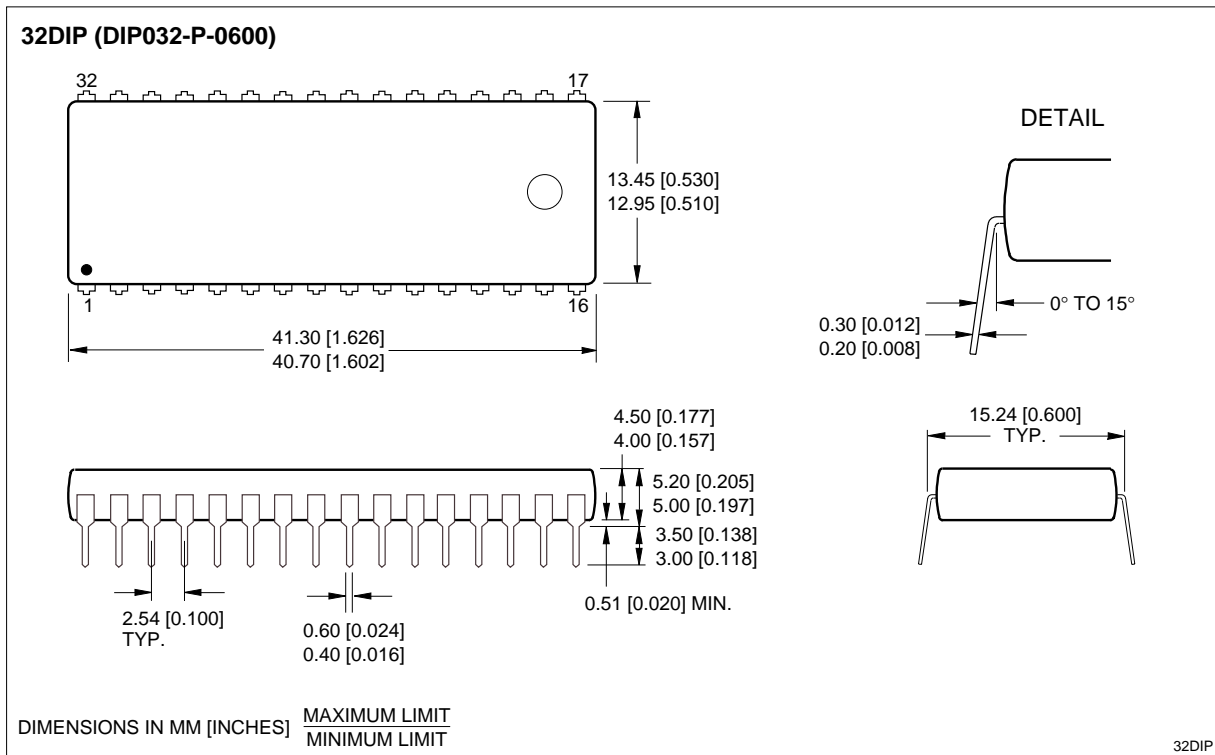
PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

**CAUTION**

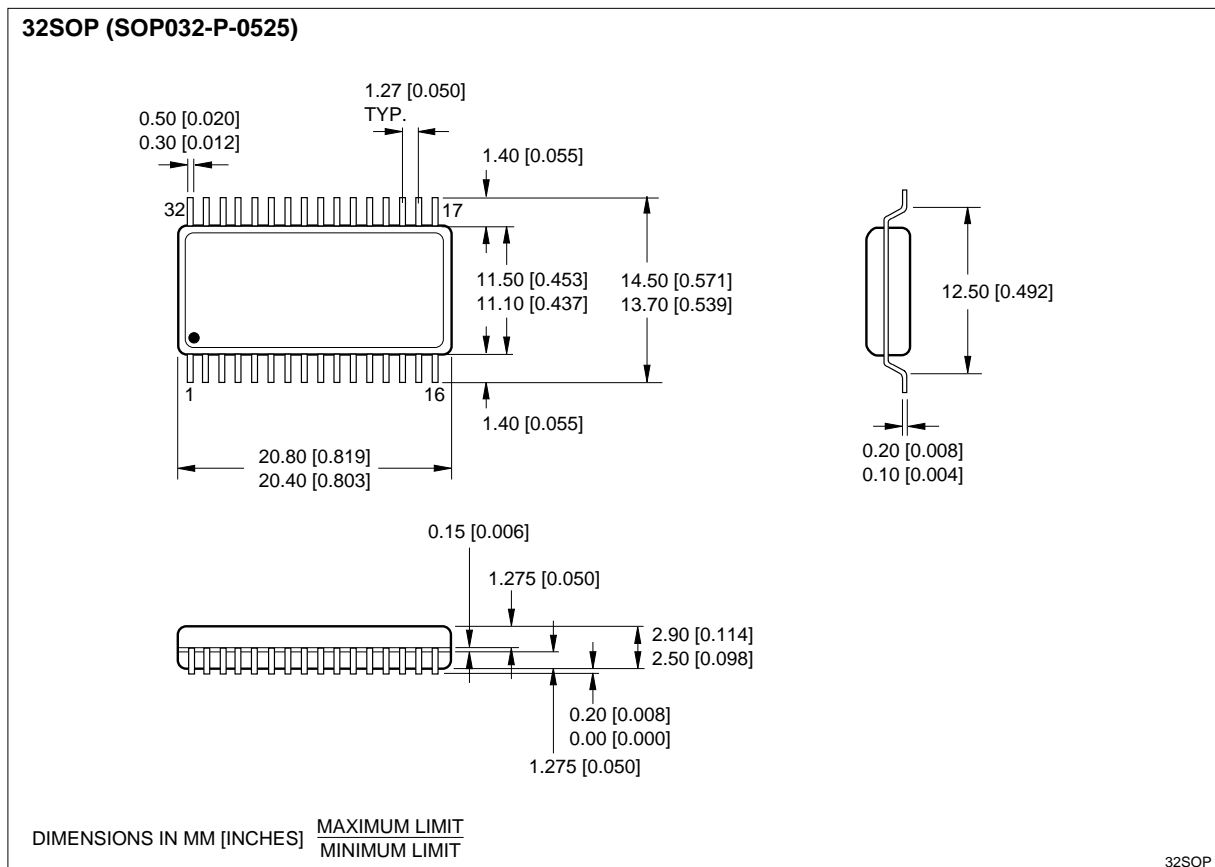
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the  $V_{CC}$  pin and the GND pin.

**Figure 4. Timing Diagram**

PACKAGE DIAGRAMS

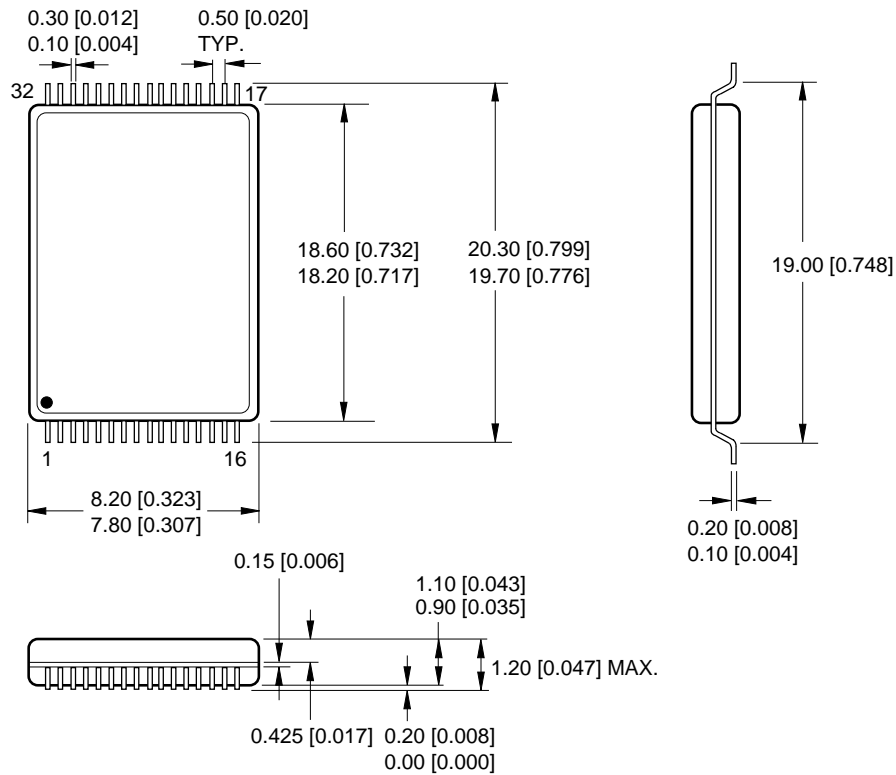


32-pin, 600-mil DIP



32-pin, 525-mil SOP

**32TSOP (Type I) (TSOP032-P-0820)**



DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

32TSOP

**32-pin, 8 × 20 mm<sup>2</sup> TSOP (Type I)**

**ORDERING INFORMATION**

LH531V00  
Device Type

X  
Package

- { D 32-pin, 600-mil DIP (DIP032-P-0600)
- { N 32-pin, 525-mil SOP (SOP032-P-0525)
- { T 32-pin, 8 x 20 mm<sup>2</sup> TSOP (Type I) (TSOP032-P-0820)

CMOS 1M (128K x 8) Mask-Programmable ROM

**Example:** LH531V00D (CMOS 1M (128K x 8) Mask-Programmable ROM, 32-pin, 600-mil DIP)

531V00-5