

LH532000B-1

CMOS 2M (256K × 8/128K × 16) MROM

FEATURES

- 262,144 words × 8 bit organization (Byte mode)
131,072 words × 16 bit organization (Word mode)
- Access time: 120 ns (MAX.)
- Power consumption:
Operating: 275 mW (MAX.)
Standby: 550 μW (MAX.)
- Mask-programmable control pin (for 40-pin DIP/40-pin SOP):
Pin 1 = OE₁/OE₁/DC
Pin 12 = OE/OE
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
 - 40-pin, 600-mil DIP
 - 40-pin, 525-mil SOP
 - 48-pin, 12 × 18 mm² TSOP (Type I)

DESCRIPTION

The LH532000B-1 is a CMOS 2M-bit mask-programmable ROM organized as 262,144 × 8 bits (Byte mode) or 131,072 × 16 bits (Word mode) that can be selected by BYTE input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

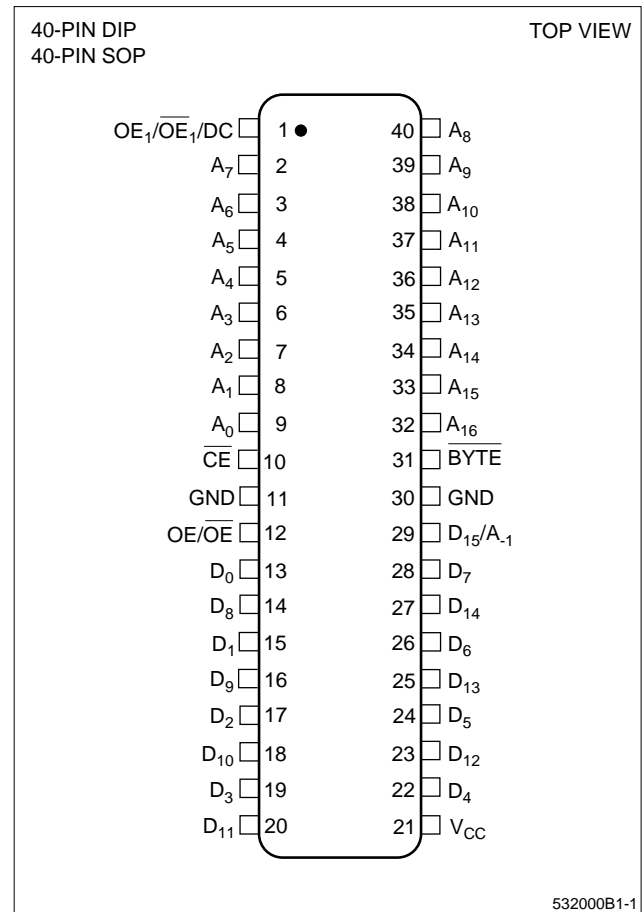


Figure 1. Pin Connections for DIP and SOP Packages

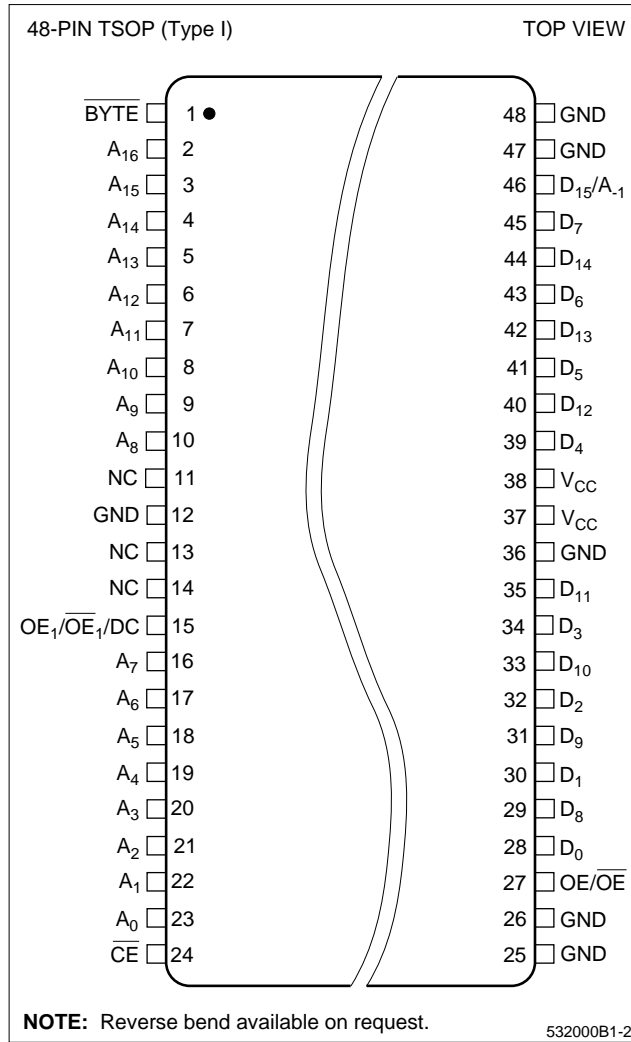


Figure 2. Pin Connections for TSOP Package

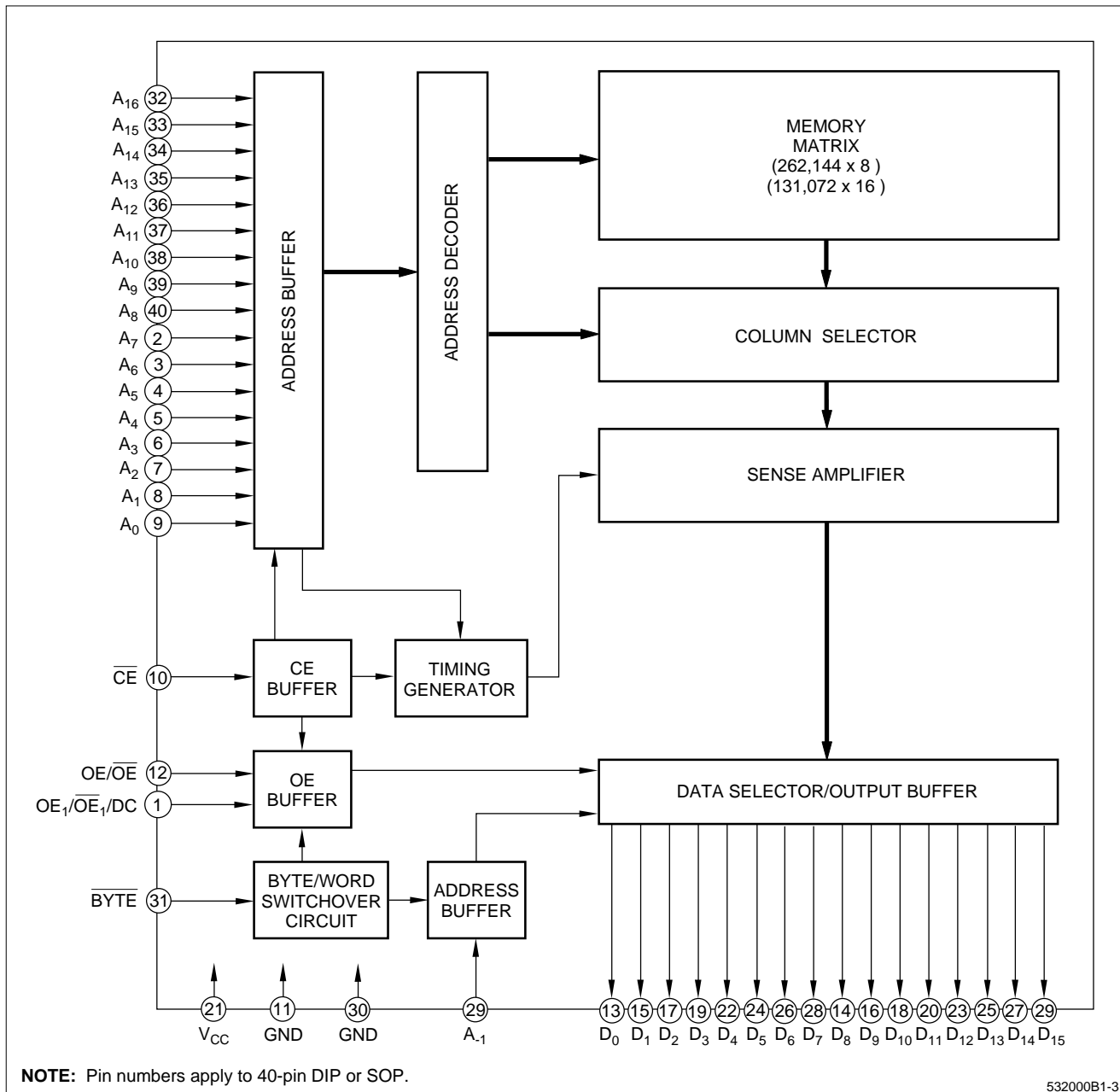


Figure 3. LH532000B-1 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₋₁ – A ₁₆	Address input	1
D ₀ – D ₁₅	Data output	1
BYTE	Byte/word mode switch	1
CE	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/OE	Output enable input	2
OE ₁ /OE ₁ /DC	Output enable input	2
V _{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D₁₅/A₋₁ pin becomes LSB address input (A₋₁) when the BYTE pin is set to be LOW in byte mode, and data output (D₁₅) when set to be HIGH in word mode.
2. The active levels of OE/OE and OE₁/OE₁/DC are mask-programmable.

TRUTH TABLE

\overline{CE}	OE/ \overline{OE}	OE ₁ / \overline{OE} ₁	\overline{BYTE}	A ₋₁ (D ₁₅)	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					D ₀ – D ₇	D ₈ – D ₁₅	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	Standby (I _{SB})
L	L/H	X	X	X	High-Z	High-Z	–	–	Operating (I _{CC})
L	X	L/H	X	X	High-Z	High-Z	–	–	Operating (I _{CC})
L	H/L	H/L	H	–	D ₀ – D ₇	D ₈ – D ₁₅	A ₀	A ₁₆	Operating (I _{CC})
L	H/L	H/L	L	L	D ₀ – D ₇	High-Z	A ₋₁	A ₁₆	Operating (I _{CC})
L	H/L	H/L	L	H	D ₈ – D ₁₅	High-Z	A ₋₁	A ₁₆	Operating (I _{CC})

NOTE:

1. X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	–0.3 to +7.0	V
Input voltage	V _{IN}	–0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	–0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V _{IL}		–0.3		0.8	V	
Input 'High' voltage	V _{IH}		2.2		V _{CC} + 0.3	V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V _{OH}	I _{OH} = –400 μA	2.4			V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}			10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}			10	μA	1
Operating current	I _{CC1}	t _{RC} = 120 ns			50	mA	2
	I _{CC2}	t _{RC} = 1 μs			45	mA	2
	I _{CC3}	t _{RC} = 120 ns			45	mA	3
	I _{CC4}	t _{RC} = 1 μs			40	mA	3
Standby current	I _{SB1}	CE = V _{IH}			3	mA	
	I _{SB2}	CE = V _{CC} – 0.2 V			100	μA	
Input capacitance	C _{IN}	f = 1 MHz			10	pF	
Output capacitance	C _{OUT}	T _A = 25°C			10	pF	

NOTES:

1. CE/OE/OE₁ = V_{IH}, OE/OE₁ = V_{IL}
2. V_{IN} = V_{IH} or V_{IL}, CE = V_{IL}, outputs open
3. V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, CE = 0.2 V, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		ns	
Address access time	t_{AA}		120	ns	
Chip enable access time	t_{ACE}		120	ns	
Output enable delay time	t_{OE}		55	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		55	ns	1
OE to output in High-Z	t_{OHZ}		55	ns	

NOTE:

1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1 TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

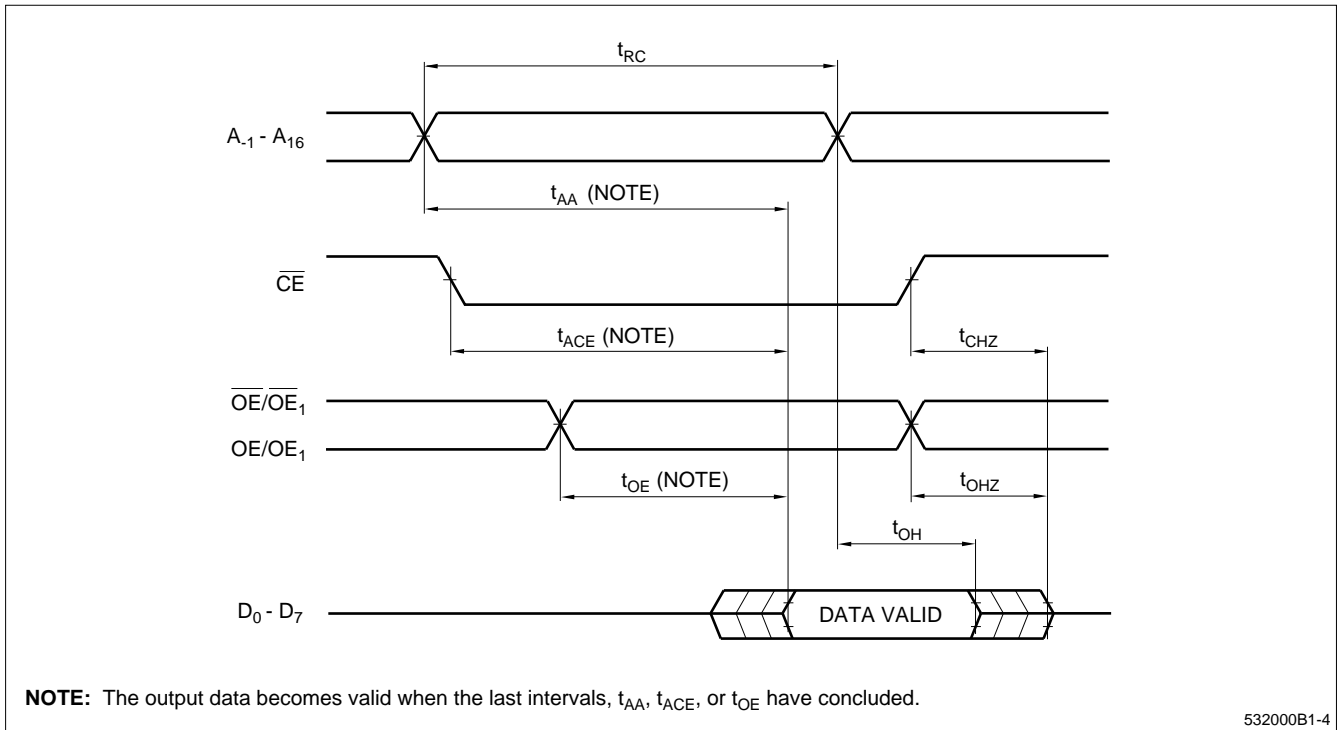


Figure 4. Byte Mode (BYTE = VIL)

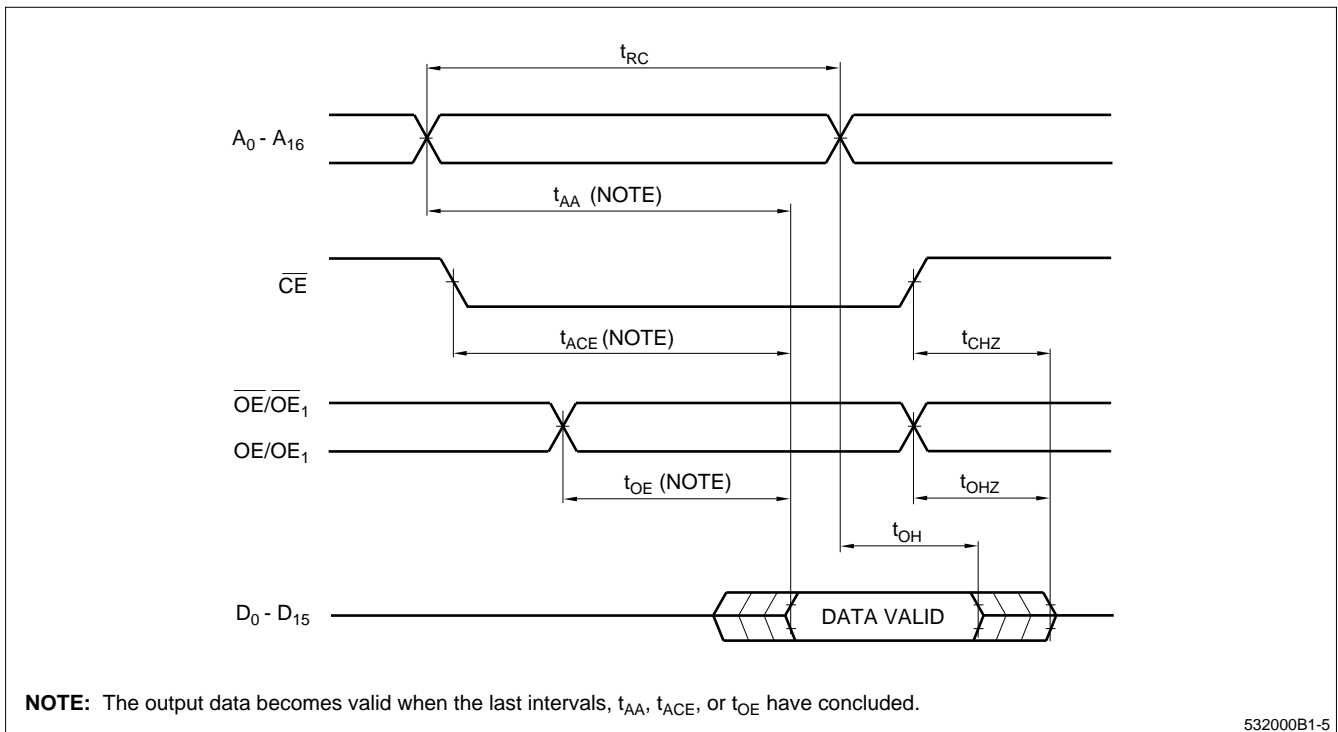
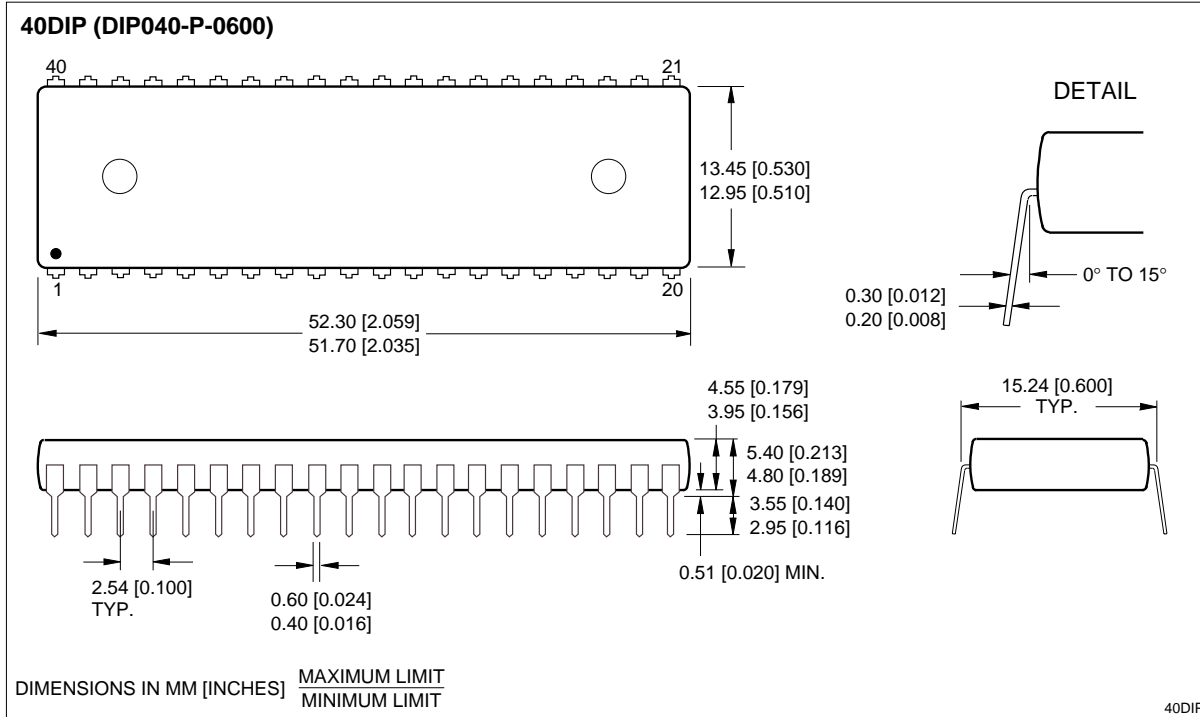
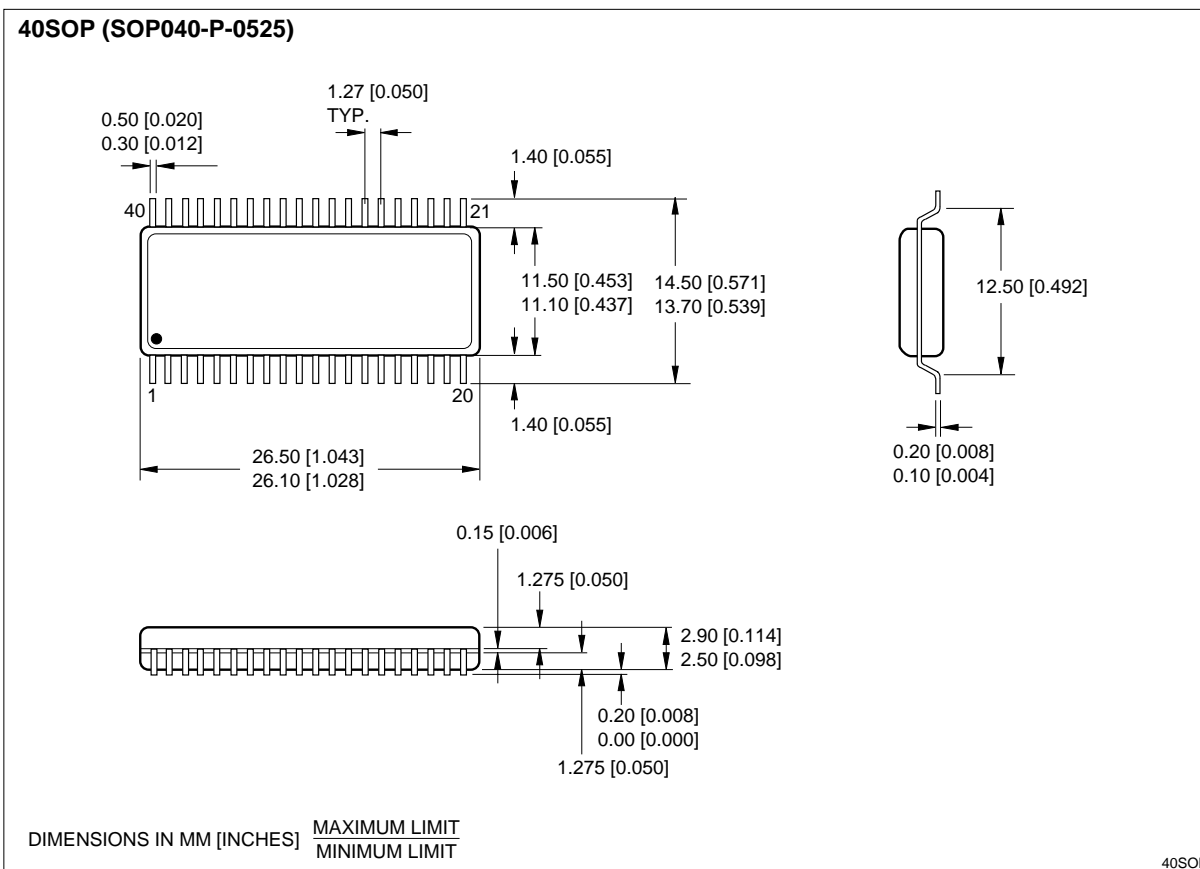


Figure 5. Word Mode (BYTE = VIH)

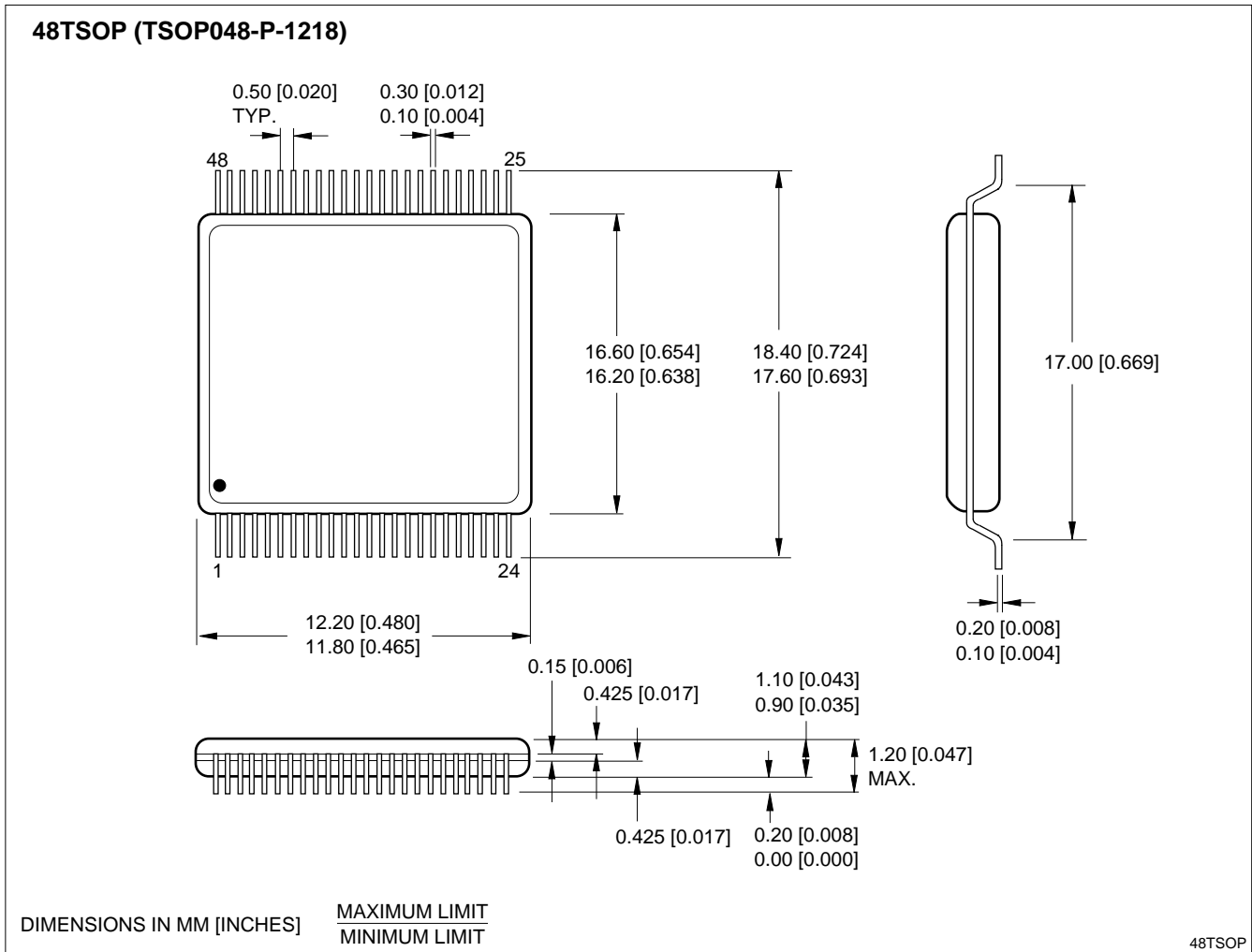
PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP



48-pin, 12 × 18 mm² TSOP (Type I)

ORDERING INFORMATION

LH532000B	X	-1
Device Type	Package	120 ns Version
		{ D 40-pin, 600-mil DIP (DIP040-P-0600)
		{ N 40-pin, 525-mil SOP (SOP040-P-0525)
		{ T 48-pin, 12 x 18 mm ² TSOP (Type I) (TSOP048-P-1218)
		{ TR 48-pin, 12 x 18 mm ² TSOP (Type I) Reverse bend (TSOP048-P-1218)
CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM		
Example: LH532000BD-1 (CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM, 40-pin, 600-mil DIP)		

532000B1-6