LH5332600

CMOS 32M (4M × 8/2M × 16) MROM

FEATURES

- 4,194,304 × 8 bit organization
  (Byte mode: $\overline{BYTE}$ = V_{IL})
  2,097,152 × 16 bit organization
  (Word mode: $\overline{BYTE}$ = V_{IH})
- Access time: 100 ns (MAX.)
- Supply current:
  - Operating: 100 mA (MAX.)
  - Standby: 100 µA (MAX.)
- TTL compatible I/O
- Three-state output
- Single +5 V power supply
- Static operation
- Packages:
  44-pin, 600-mil SOP
  48-pin, 12 mm × 18 mm^2 TSOP (Type I)
- Others:
  - Non programmable
  - Not designed or rated as radiation hardened
  - CMOS process (P type silicon substrate)

DESCRIPTION

The LH5332600 is a 32M-bit mask-programmable ROM organized as 4,194,304 × 8 bits (Byte mode) or 2,097,152 × 16 bits (Word mode) that can be selected by a $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

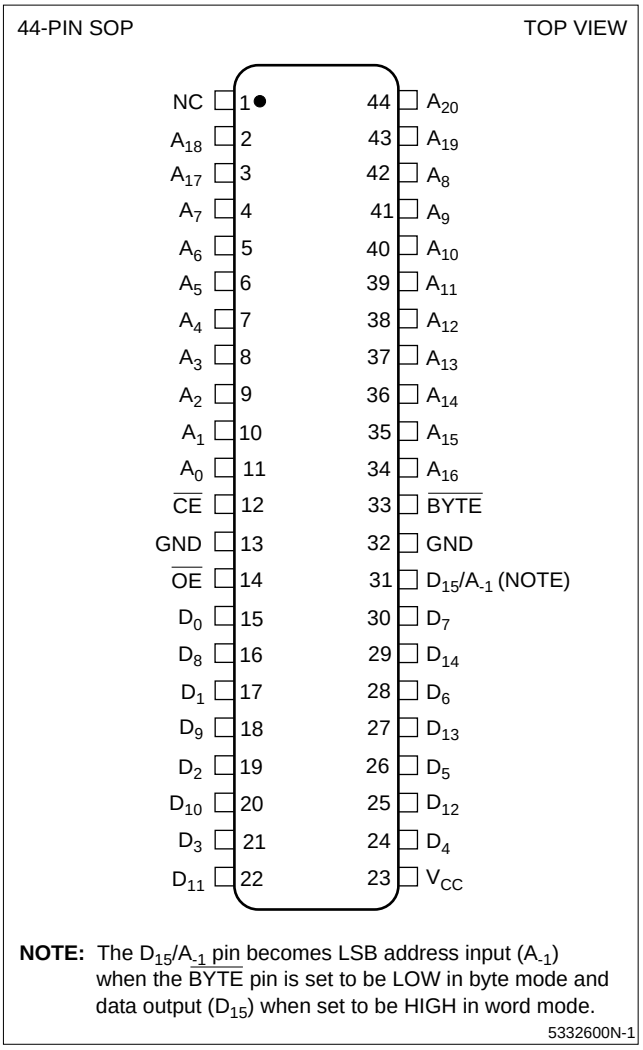


Figure 1. SOP Pin Connections

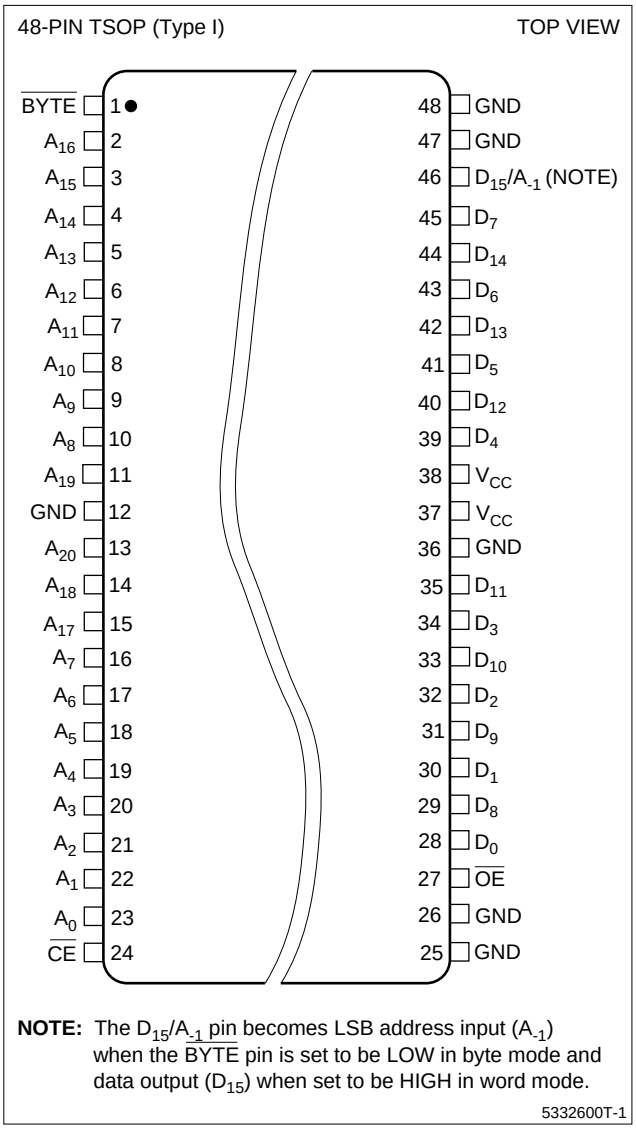


Figure 2. TSOP Pin Connections

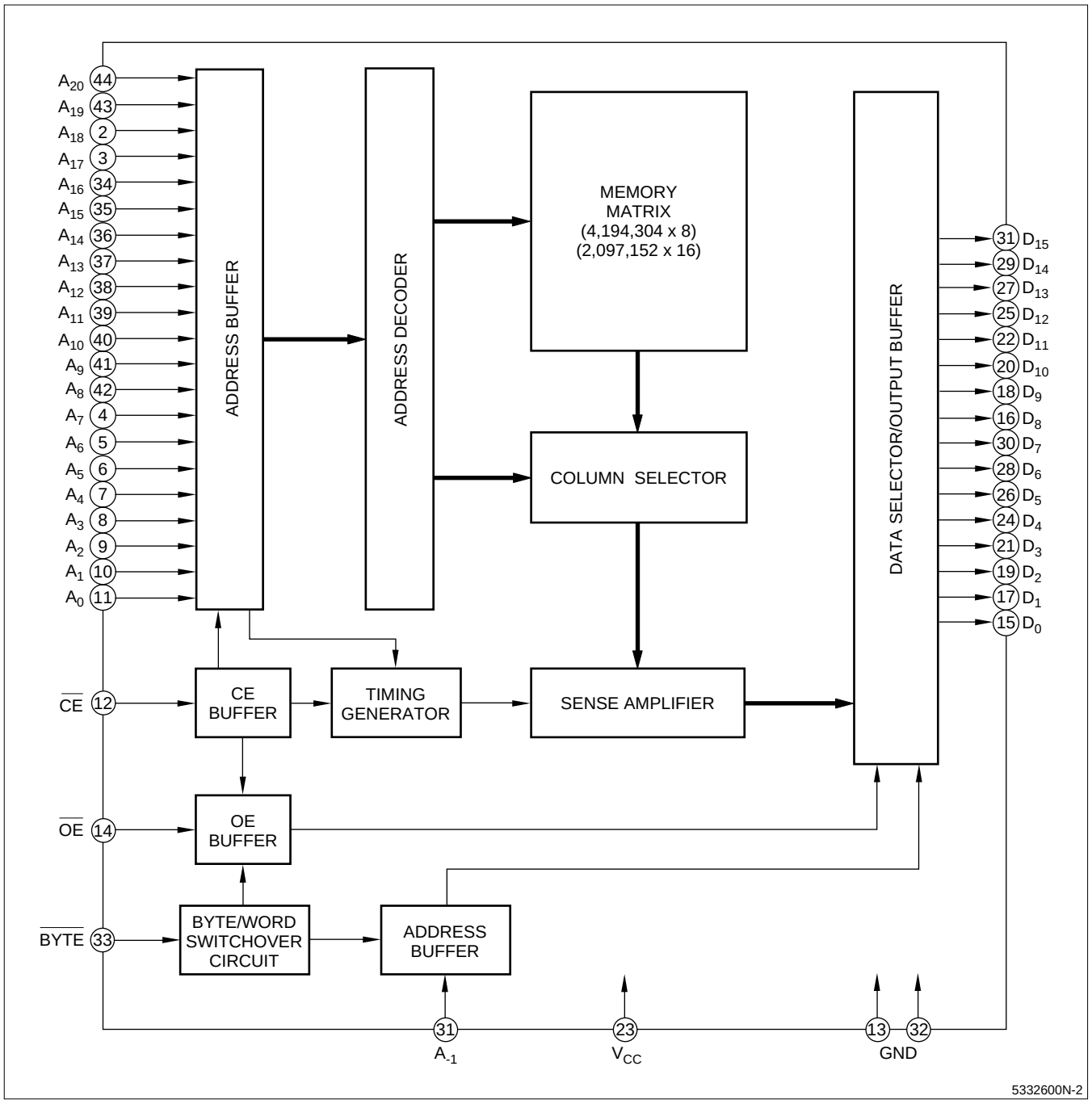


Figure 3. LH5332600 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{20}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	×8bit / ×16 bit (byte/word) mode select input
$\overline{CE}$	Chip enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output enable input
V_{CC}	Power supply
GND	Ground
NC	No connection (Non wire bonding)

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	X	High-Z	High-Z	—	—	Standby (I_{SB})
L	H	X	X	High-Z	High-Z	—	—	Operating
L	L	H	—	D_0 - D_7	D_8 - D_{15}	A_0	A_{20}	Operating
L	L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{20}	Operating
L	L	L	H	D_8 - D_{15}	High-Z	A_{-1}	A_{20}	Operating

NOTES:
X = Don't care; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}	—	2.2	V_{CC} + 0.3	V	—
Input 'Low' voltage	V_{IL}	—	-0.3	0.8	V	—
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4	—	V	—
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA	—	0.4	V	—
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}	—	10	µA	—
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}	—	10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns	—	100	mA	2
	I_{CC2}	t_{RC} = 1 µs	—	90		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}	—	2	mA	—
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V	—	100	µA	—
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C	—	10	pF	—
Output capacitance	C_{OUT}		—	10	pF	—

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, output is open

AC ELECTICAL CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100	—	ns	—
Address access time	t_{AA}	—	100	ns	—
Chip enable access time	t_{ACE}	—	100	ns	—
Output enable delay time	t_{OE}	—	50	ns	—
Output hold time	t_{OH}	5	—	ns	—
Output floating time	t_{CHZ}	—	40	ns	1
	t_{OHZ}	—	40	ns	

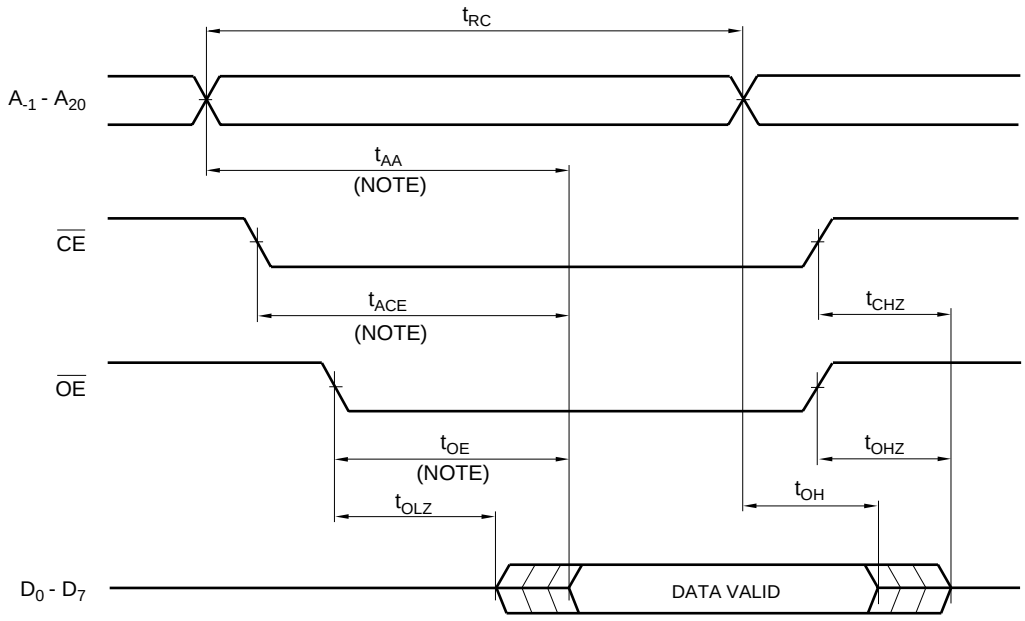
NOTE:
1. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input signal fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

It is recommended that a decoupling capacitor be connected between V_{CC} and GND-Pin.



NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

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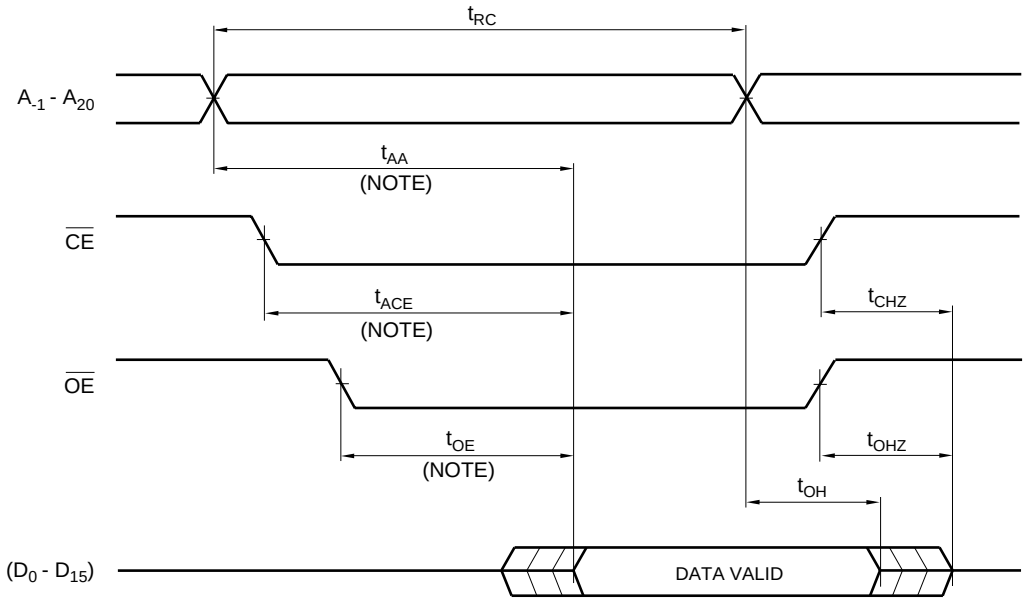
Figure 4. Byte Mode ($\overline{BYTE}$ = V_{IL})



NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

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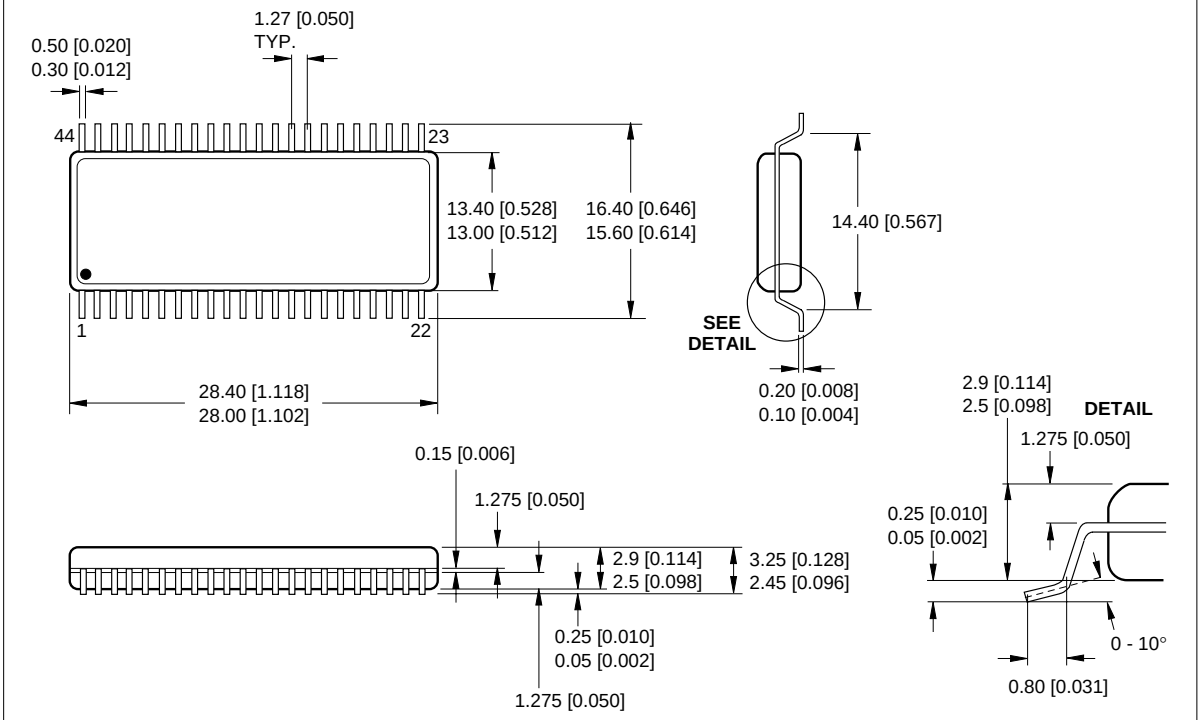
Figure 5. Word Mode ($\overline{BYTE}$ = V_{IH})

PACKAGE DIAGRAM

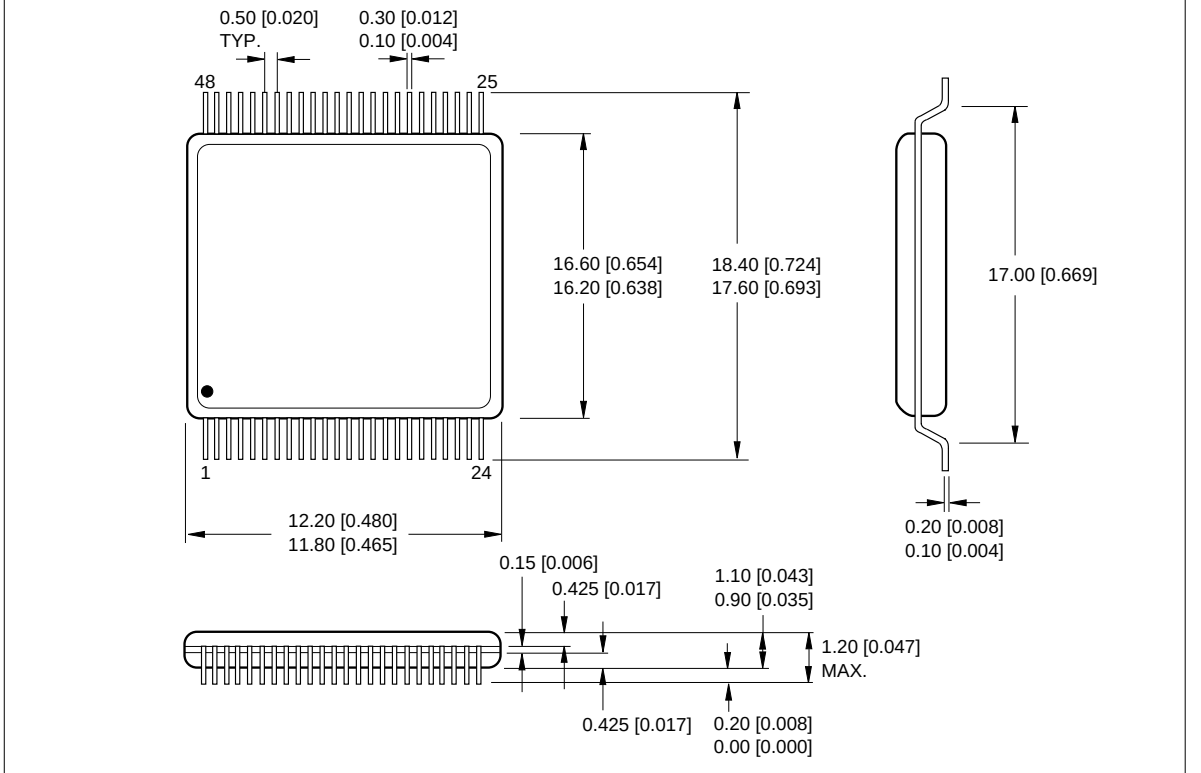
44SOP (SOP044-P-0600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44SOP

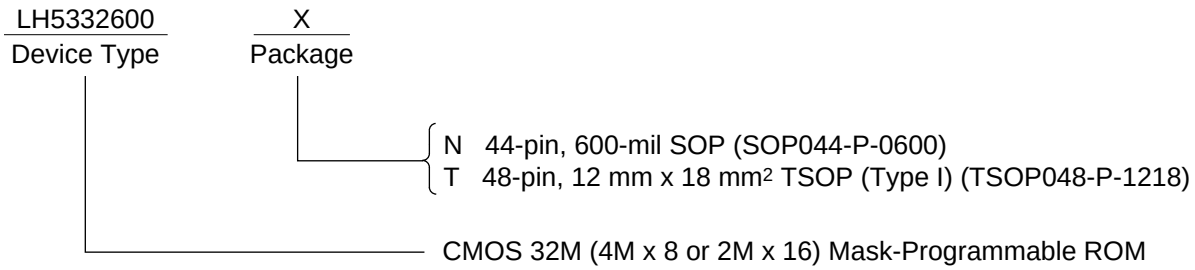
48TSOP (TSOP048-P-1218)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

48TSOP

ORDERING INFORMATION



Example: LH5332600N (CMOS 32M (4M x 8 or 2M x 16) Mask-Programmable ROM, 44-pin, 600-mil SOP)

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