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LIS - 500 Line Scan Image Sensor

DESCRIPTION

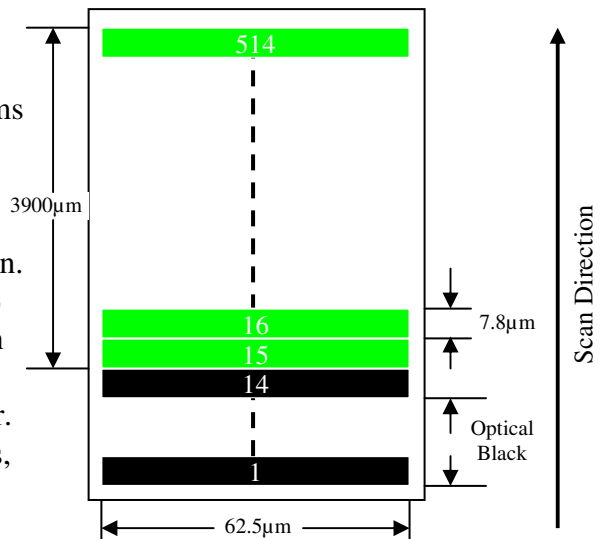
This high performance, ultra low power, low cost sensor is designed to meet the demanding needs for small cost effective decoding, position detection and feedback, OCR, and other applications.

All that is needed to achieve video is a single low voltage power supply, a clock, and up to three control signals.

This device maybe protected by patent number 6,084,229, 6,818,877B2 and others pending.

Key Features

- Single Supply Operation, 2.8 Volt to 3.3 Volt
- Low Cost Compared to CCD multi-chip systems
- High Sensitivity
- Simple operation: one clock and up to three control signals.
- On chip Fixed Pattern Noise (FPN) cancellation.
- Clamping optically black pixels to reference to reduce chip wide offset errors, charge injection and dark current.
- Externally programmable x1, x3 gain amplifier.
- Control signal for Reset of shift register, pixels, integration period and start of readout.



Pixel Type	PANAVISION IMAGING, LLC Proprietary Linear Image Sensor (LIS)™ photo diode
Array Size	1x500 + 13 dark pixels + 1 dummy pixel (invalid - pixel #14)
Pixel Size (Pitch)	7.8u X 62.5 microns
Imaging Active Area	62.5 microns X 3900 microns
Output	10K ohm output impedance analog into 5 pf max.
Fill Factor	100 %

Electrical Characteristics/Recommended Operating Conditions

Note: All parameters are at 24 Deg. Celsius, 51.2 kHz read rate, light color temperature of 5300K, 5pF load, Gain=x1 and VDD=3V, Gain =1x unless otherwise noted.

Parameter	Test Conditions	Min	Typical	Max	Typical at 60 Deg. Celsius.	Units
Supply Voltage, VDD		2.7	3.0	3.3		V
Power Consumption			24	30		mW
Pwr. Down Power Consumption Est.	Low power mode.		30			uW
Input High Level (3)		2.5				V
Input Low Level				0.7		V
CLK Low pulse width	Readout	6				μs
CLK High pulse width	Readout	3.7				μs
Setup time, /CLK	/CLK falling		0.1	0.5		ns
Hold time, /CLK	/CLK falling		0.2	1		ns
Pixel Read Rate - Analog		15	50	1,000(4)		KHz
Video settling time (t _d)			1			μs
Analog output impedance			10K			Ohms
Output Voltage at Saturation			VDD-.8			V
Output Voltage at Dark	Analog Out.	0.58	0.75	0.88		V
V _{BLKRef}	Current Sink			1.0		mA
Linearity per pixel (x1 gain)	5%-70% avg.	0.5	3	5.0	5.0	%SAT
Pixel Non-Uniformity Dark	X3 gain		6			mVrmse (1)
Dark Signal	10 ms Integration time		0.1		3.2	mV
Dynamic Range (RMS)	Vsat/RMS Noise (2)	54				dB
Conversion Gain			3.6			μV/e ⁻
Full Well		235K	290K			e ⁻
Absolute QE	λ=675nm		65			%
Sensitivity	λ=555nm		3.87			V/lux-s
Read Noise, <100kHz			1.5	1.7		mVrmse (2)
Spectral response	See curve	200		1100		nm
Image Lag		0.1	1.0	3.0		%SAT
Relative Humidity	Non-condensing	0		90		%
Operating Temperature		0		70		°C

Table 1 Electro-optical Characteristics

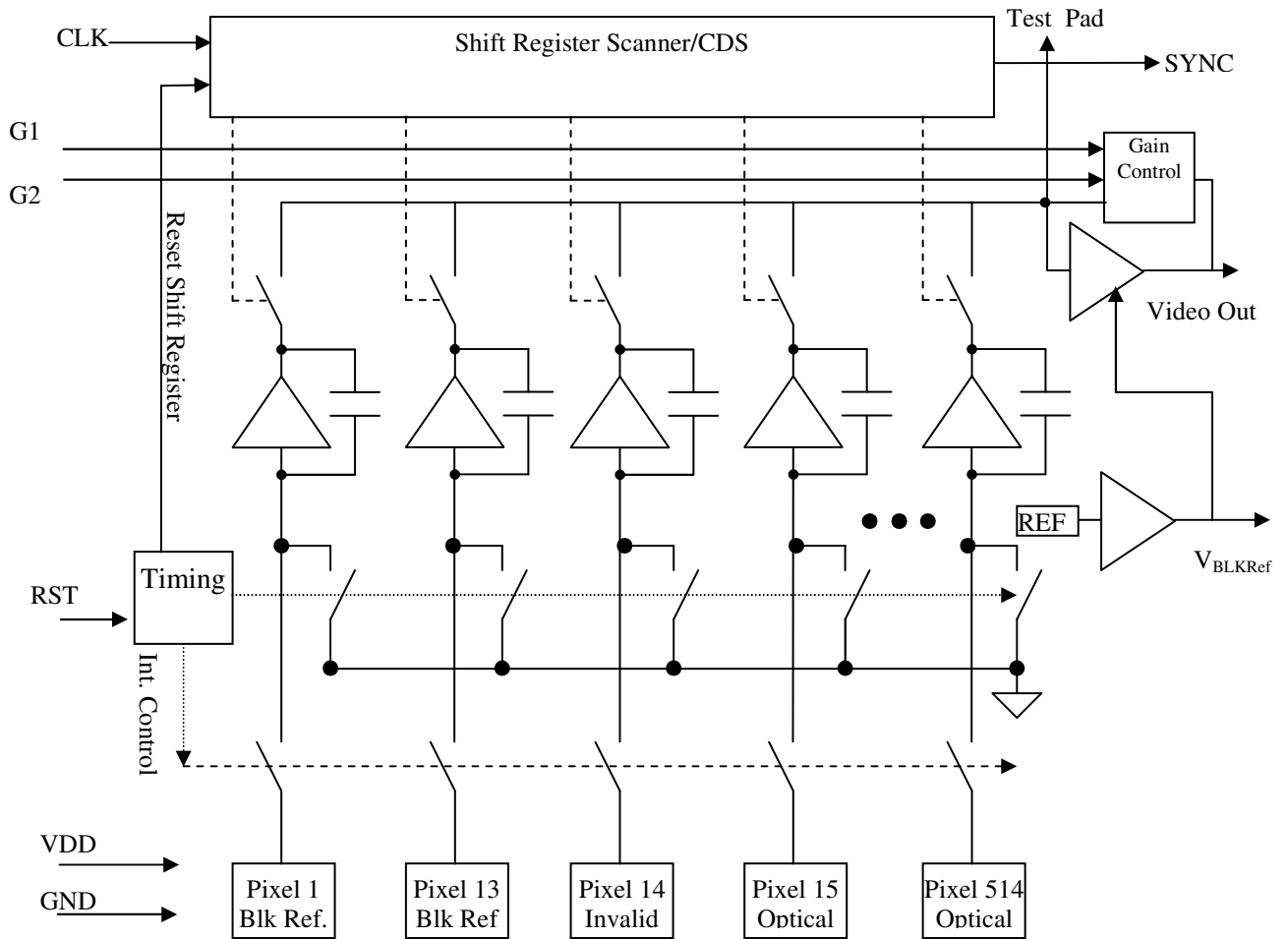
NOTE 1: V_{rmse} of N samples is calculated as
$$V_{rmse} = \sqrt{\frac{1}{N} \sum_{i=1}^N (V_i - |V_i|)^2}$$

NOTE 2: Dynamic range defined as the Output Voltage at Saturation minus Output Voltage at Dark to Read Noise ratio.

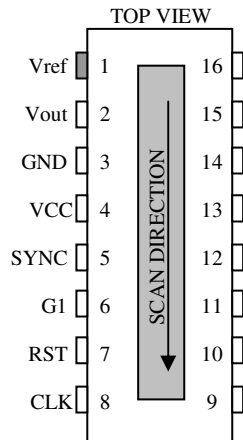
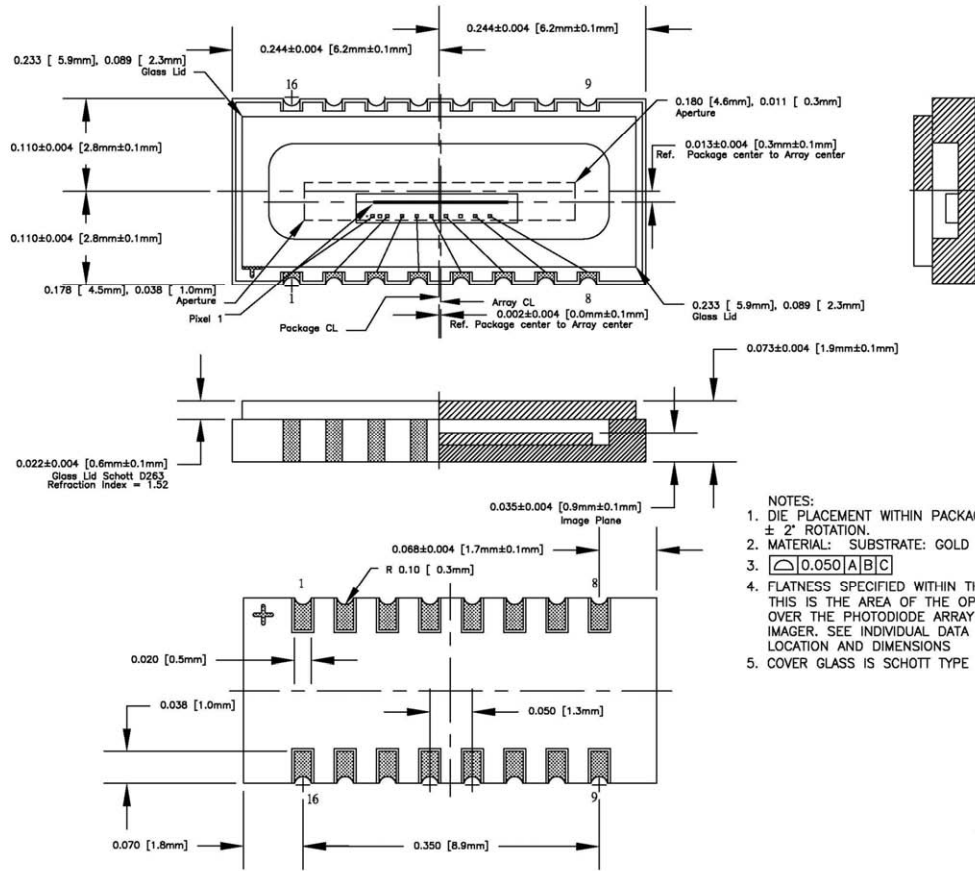
NOTE 3: Amplitude of I/O voltages must not exceed the supply voltage, VDD.

NOTE 4: Note that MTF may degrade at speeds beyond 50khz

Block Diagram



LIS-500 LCC Package Information



Part number info

LIS-500A-KG	Known Good Die (KGD) on wafer
LIS-500A-WP	Waffle Pack
LIS-500A-LG	LCC Package

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This imager may be covered under the following patent(s): 6,084,229, 6,818,877B2 and others pending.

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