

LJ320U21

Features

- Display format: 320 (W) × 240 (H) dots
- Dot pitch ratio: 1:1
- Input signal level: LS TTL level
- Drive method: P-N symmetric drive
- Structure: Al frame
- Net weight: Approx. 600g

Absolute maximum ratings

(Ta=25°C)

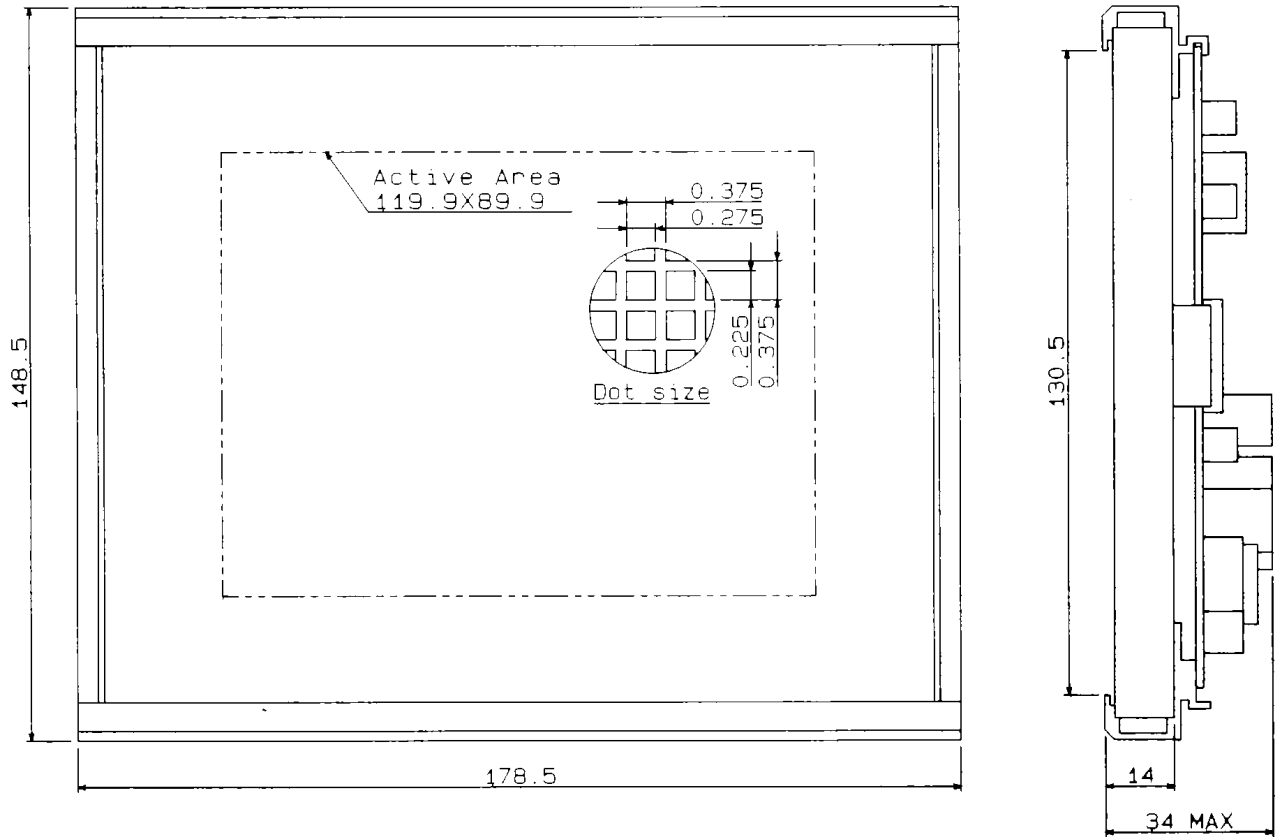
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V _{IH}	5.5	V
Interface signal (Logic "L")	V _{IL}	-0.5	V
Supply voltage (Logic)	V _L	7	V
Supply voltage (Panel drive)	V _D	18	V
Operating temperature	T _{opr}	0 to +55	°C
Storage temperature	T _{stg}	-25 to +70	°C

Corresponding connector:

HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Connector
HIF3F-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V _L	—	4.75	5.0	5.25	V
Supply current (Logic)	I _L	V _L =5V	100	—	450	mA
Supply voltage (Panel drive)	V _D	—	14.25	15.0	15.75	V
Supply current (Panel drive)	I _D	V _D =15V	50	—	550	mA
Power consumption	P _T	V _L =5V, V _D =15V	—	8	—	W
Luminance	B _{ON}	All dots lit	20	—	—	fL
Off luminance	B _{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	ΔB _{DIS}	All dots lit	—	—	35	%

Interface Signals

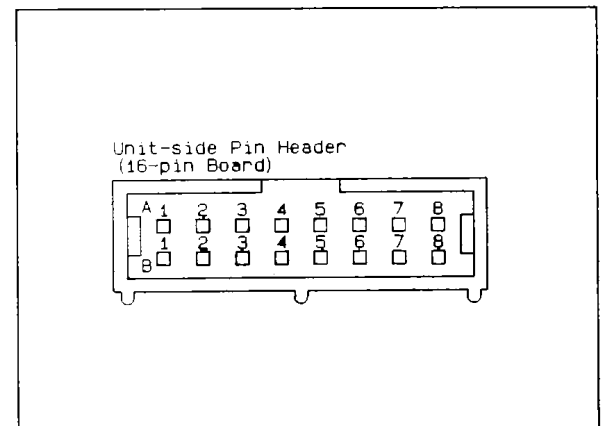
Pin No.	Symbol	Description
A-1	D _{IN}	Data signal
B-1	GND	Ground
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	GND	Ground
A-5	GND	Ground
B-5	GND	Ground
A-6	GND	Ground
B-6	GND	Ground
A-7	V _L	+5V
B-7	V _L	+5V
A-8	V _D	+15V
B-8	V _D	+15V

Interface Timing Ratings

(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	1/T _{CL}	4.4	—	7.5	MHz
Clock duty	T _{CL(H)}/T_{CL} × 100}	45	—	55	%
Horizontal sync. signal cycle time	T _H	62	—	75	μsec
Horizontal sync. signal blanking time	t _{HB}	2	—	—	μsec
Vertical sync. signal blanking time	t _{VB}	1	—	N × T _H	μsec
Vertical sync. signal valid time	t _{VA}	240 × T _H	—	—	μsec
Frame frequency	1/T _V	50	60	63	Hz
Data signal delay time required	t _{DD}	0.01	—	T _{CL}	μsec
Horizontal sync. signal delay time required	t _{HD}	0.01	—	T _{CL}/2}	μsec
Vertical sync. signal rise wait time	t _{VR}	4 × 62	—	—	μsec
Vertical sync. rise timing	t _{VH}	62	—	T _H - t _{HB} + 50	μsec

Connector



Interface Timing Chart

