

# LJ320U27

## Features

- **Display format:** 320 (W) × 256 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- **Net weight:** Approx. 400g
- **LJ320U26:** +5V, +15V type is also available.

## ■ Absolute maximum ratings

(Ta=25°C)

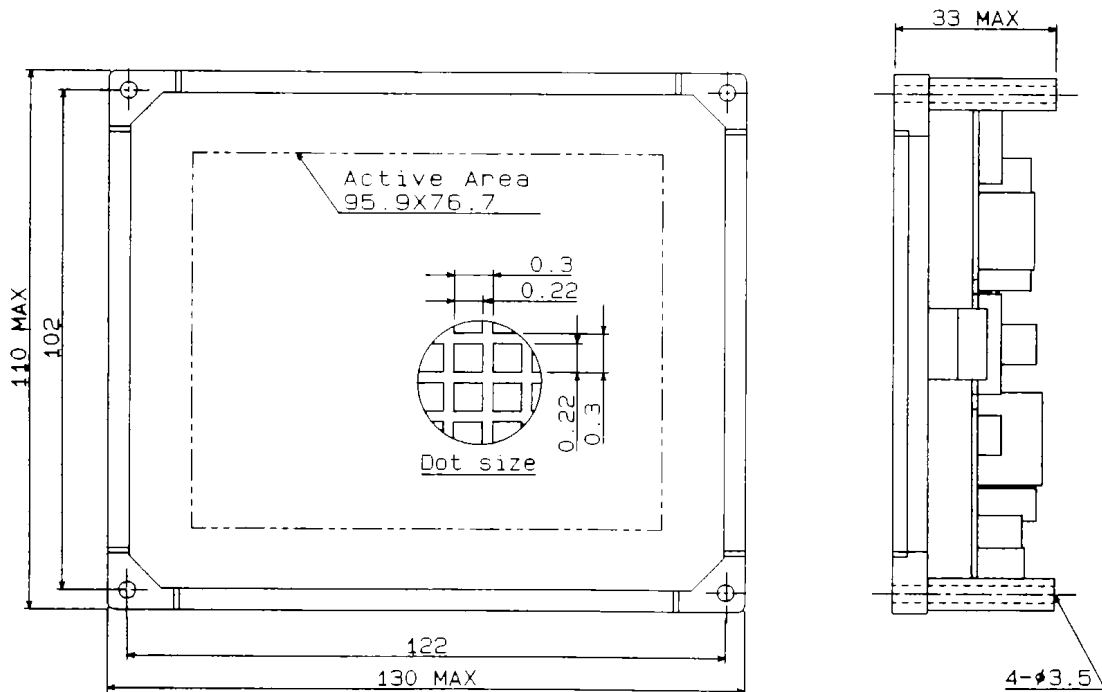
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V <sub>IH</sub>	5.5	V
Interface signal (Logic "L")	V <sub>IL</sub>	-0.5	V
Supply voltage (Logic)	V <sub>L</sub>	7	V
Supply voltage (Panel drive)	V <sub>D</sub>	14	V
Operating temperature	T <sub>opr</sub>	-5 to +65	°C
Storage temperature	T <sub>stg</sub>	-40 to +80	°C

## ■ Corresponding connector:

HIF3A-16D-2.54R (HIROSE) or equivalents

## Outline Dimensions

(Unit:mm)



Connector  
HIF3F-16PA-2.54DSA (HIROSE ELECTRIC) or equivalents.

# LJ320U27

## Tentative Specifications

### Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V <sub>L</sub>		4.75	5.0	5.25	V
Supply current (Logic)	I <sub>L</sub>	V <sub>L</sub> =5V	(50)	—	(450)	mA
Supply voltage (Panel drive)	V <sub>D</sub>		11.4	12.0	12.6	V
Supply current (Panel drive)	I <sub>D</sub>	V <sub>D</sub> =15V	(100)	—	(550)	mA
Power consumption	P <sub>T</sub>	V <sub>L</sub> =5V, V <sub>D</sub> =15V	—	(5)	—	W
Luminance	B <sub>ON</sub>	All dots lit	23	30	—	fL
Off luminance	B <sub>OFF</sub>	All dots turned off	—	—	1.0	fL
Luminance distribution	ΔB <sub>DVS</sub>	All dots lit	—	—	35	%

( ) : Tentative

### Interface Signals

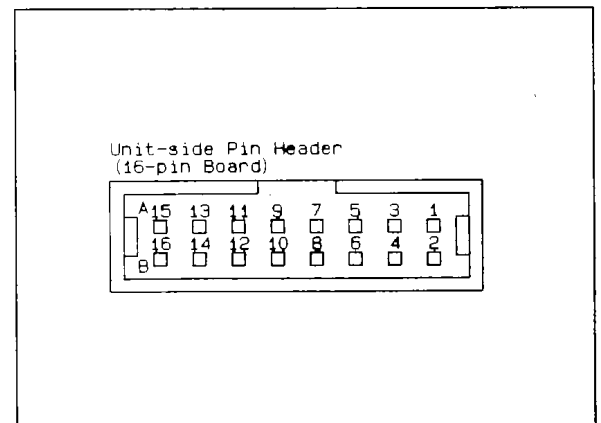
Pin No.	Symbol	Description
1	V <sub>D</sub>	+12V
2	V <sub>D</sub>	+12V
3	V <sub>L</sub>	+5V
4	V <sub>L</sub>	+5V
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	V.D	Vertical sync. signal
10	GND	Ground
11	H.D	Horizontal sync. signal
12	GND	Ground
13	CKD	Data transfer clock
14	GND	Ground
15	D <sub>IN</sub>	Data signal
16	GND	Ground

### Interface Timing Ratings

(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	1/T <sub>CL</sub>	4.4	—	16	MHz
Clock duty	T <sub>CL(H)T<sub>CL</sub> × 100</sub>	45	—	55	%
Horizontal sync. signal cycle time	T <sub>H</sub>	60	—	75	μSEC
Horizontal sync. signal blanking time	t <sub>HB</sub>	2	—	—	μSEC
Vertical sync. signal blanking time	t <sub>VB</sub>	1	—	N × T <sub>H</sub>	μSEC
Vertical sync. signal valid time	t <sub>VA</sub>	256 × T <sub>H</sub>	—	—	μSEC
Frame frequency	1/T <sub>V</sub>	50	60	63	Hz
Data signal delay time required	t <sub>DO</sub>	0.01	—	T <sub>CL</sub>	μSEC
Horizontal sync. signal delay time required	t <sub>HD</sub>	0.01	—	T <sub>CL</sub> /2	μSEC
Vertical sync. signal rise wait time	t <sub>VR</sub>	4 × 60	—	—	μSEC
Vertical sync. rise timing	t <sub>VH</sub>	60	—	T <sub>H</sub> - t <sub>HB</sub> + 50	μSEC

### Connector



### Interface Timing Chart

