LJ720U22

Features

- **Display format:** 720 (W) × 400 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- **Net weight:** Approx. 850g

Absolute maximum ratings

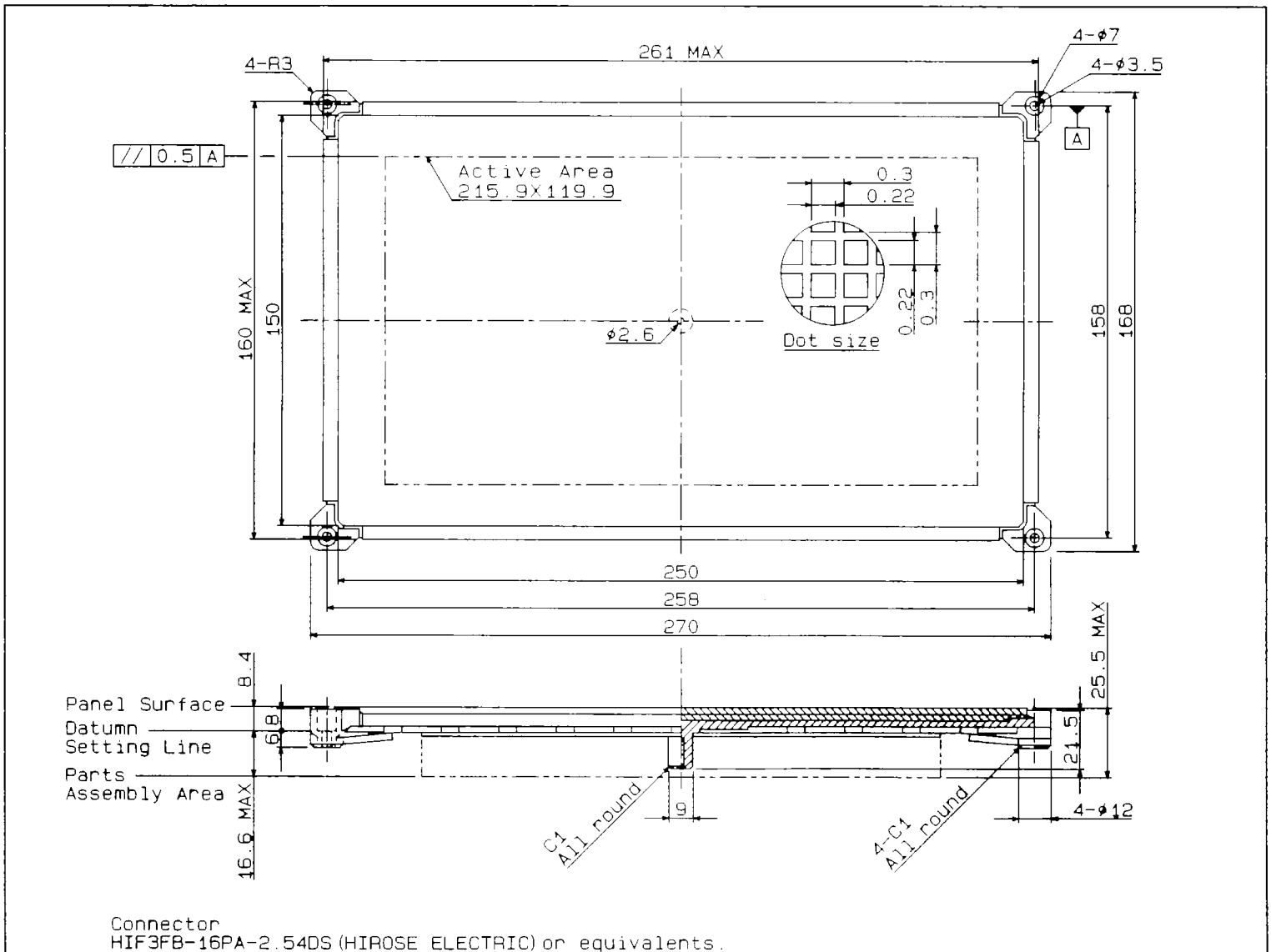
(Ta=25°C)

Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	18	V
Supply voltage (Panel drive)	V_M	30	V
Operating temperature	Topr	0 to +55	°C
Storage temperature	Tstg	−25 to +70	°C

- **Corresponding connector:**
  HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Connector
HIF3FB-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L		4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	50	—	400	mA
Supply voltage (Panel drive)	V_D		14.25	15.0	15.75	V
Supply current (Panel drive)	I_D	V_D=15V	50	—	600	mA
Supply voltage (Panel drive)	V_M		23.75	25.0	26.25	V
Supply current (Panel drive)	I_M	V_M=25V	25	—	600	mA
Power consumption	P_T	V_L=5V, V_D=15V, V_M=25V	—	13	20	W
Luminance	B_{ON}	All dots lit	20	—	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	ΔB_{DIS}	All dots lit	—	—	35	%

Interface Signals

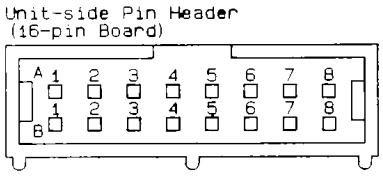
Pin No.	Symbol	Description
A-1	$D_{IN}0$	Data signal for odd column
B-1	$D_{IN}1$	Data signal for even column
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	$\overline{\text{RESET}}$	
A-5	GND	Ground
B-5	GND	Ground
A-6	V_M	+25V
B-6	V_M	+25V
A-7	V_L	+5V
B-7	V_L	+5V
A-8	V_D	+15V
B-8	V_D	+15V

Interface Timing Ratings

(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	8	10	12	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	40	—	49	μsec
Horizontal sync. signal blanking time	t_{HB}	1	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$400\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	50	60	61	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×40	—	—	μsec
Vertical sync. rise timing	t_{VH}	40	—	$T_{HH}+35$	μsec

Connector



Interface Timing Chart