SHARP

No.	LD-K22553
DATE	May. 21. 2010

TENTATIVE

TECHNICAL LITERATURE

FOR

TFT - LCD PANEL
(Open Cell)

MODEL No. LK400D3HA＊＊

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DEVELOPMENT DEPARTMENT. 2
LIQUID CRYSTAL DISPLAY DIVISION.1
LIQUID CRYSTAL DISPLAY GROUP
SHARP CORPORATION

RECORDS OF REVISION

LK400D3HA＊＊

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-K22553	May. 21. 2010	-	-	-	1st. Issue

1 Application

This specification applies to the color 40.0" TFT-LCD Open Cell LK400D3HA＊＊
(With parts (FPC,C-PWB) to drive it.)

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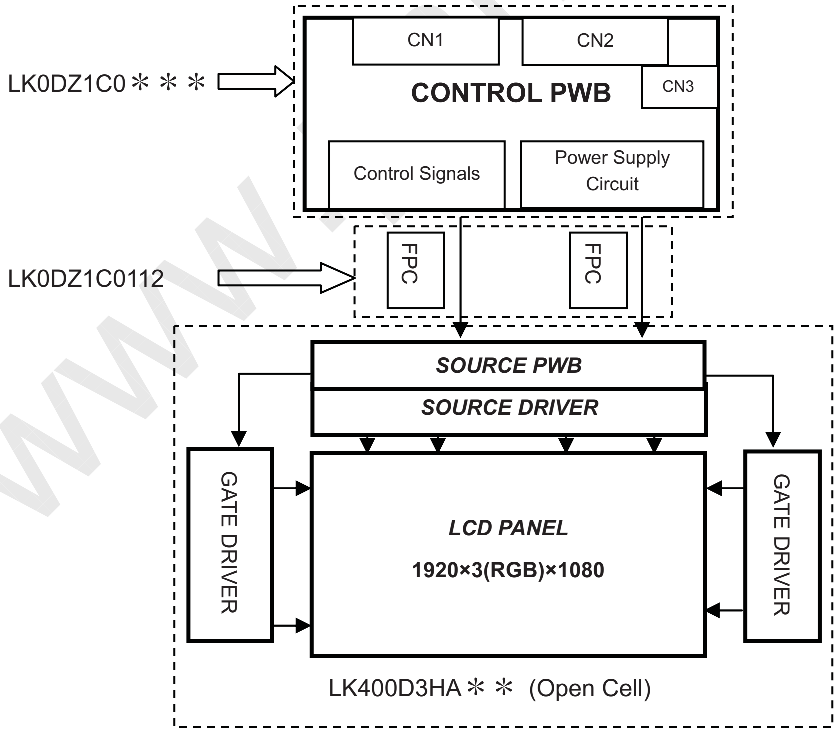
2 Overview

This Open Cell is a color active matrix LCD Open-Cell incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs and Source PWB. The following content can be achieved in using LK0DZ1C0＊＊＊(CONTROL PWB "C-PWB") and LK0DZ1C0112 (FPC) that SHARP specifies. Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with one billion colors by using 10bit+ LVDS (Low Voltage Differential Signaling) to interface, +12V of DC supply voltages.Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with one billion colors by using 10bit+ LVDS (Low Voltage Differential Signaling) to interface, +12V of DC supply voltages.

And in order to improve the response time of LCD, This C-PWB applies the Over Shoot driving (O/S driving) technology for the control circuit .In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.



3 Mechanical Specifications

Parameter	Specifications	Unit
Display size	101.609 （Diagonal）	cm
	40.0 （Diagonal）	inch
Active area	885.6H) x 498.15 (V)	mm
Pixel Format	1920(H) x 1080(V) （1pixel = R + G + B dot）	pixel
Pixel pitch	461.25(H) x 461.25 (V)	um
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Cell Outline Dimensions[Note1]	921.18(H) x 548.55(V) x 1.82(D)	mm
Mass	1.81 ±0.3	kg
Surface treatment [Note2] (Upper Polarizing film)	Low-Haze Anti Glare Hard coating : 2H and more	
Surface treatment [Note2] (Lower Polarizing film)	Plane Hard coating : —	

[Note1] Outline dimensions are shown in P21.
[Note2] With the protection film removed.

4 Cell Driving Specifications

4.1 Driving interface of Control PWB SHARP specifies[LK0DZ1C0＊＊＊]

CN1 (Interface signals and +12V DC power supply) (Shown in Fig1)

Using connector : FI-RNE51SZ-HF (Japan Aviation Electronics Ind., Ltd.)

Matching connector : FI-RE51HL, FI-RE51CL (Japan Aviation Electronics Ind., Ltd.)

Matching LVDS transmitter : THC63LVD1023 or equivalent device

Pin No.	Symbol	Function	Remark
1	GND		
2	Reserved	It is required to set non-connection(OPEN)	Pull up 3.3V
3	Reserved	It is required to set non-connection(OPEN)	Pull up 3.3V
4	Reserved	It is required to set non-connection(OPEN)	Pull up 3.3V
5	FRAME	Frame frequency setting 0:120Hz 1:100Hz [Note 1]	Pull down : (GND)
6	O/S set	O/S operation setting H:O/S ON, L:O/S OFF [Note 2]	Pull up 3.3V
7	SELLVDS	Select LVDS data order [Note 2,3]	Pull up 3.3V
8	Reserved	It is required to set non-connection(OPEN)	Pull down : (GND)
9	Reserved	It is required to set non-connection(OPEN)	Pull down : (GND)
10	Reserved	It is required to set non-connection(OPEN)	Pull down : (GND)
11	GND		
12	AIN0-	Aport (-)LVDS CH0 differential data input	
13	AIN0+	Aport (+)LVDS CH0 differential data input	
14	AIN1-	Aport (-)LVDS CH1 differential data input	
15	AIN1+	Aport (+)LVDS CH1 differential data input	
16	AIN2-	Aport (-)LVDS CH2 differential data input	
17	AIN2+	Aport (+)LVDS CH2 differential data input	
18	GND		
19	ACK-	Aport LVDS Clock signal(-)	
20	ACK+	Aport LVDS Clock signal(+)	
21	GND		
22	AIN3-	Aport (-)LVDS CH3 differential data input	
23	AIN3+	Aport (+)LVDS CH3 differential data input	
24	AIN4-	Aport (-)LVDS CH4 differential data input	
25	AIN4+	Aport (+)LVDS CH4 differential data input	
26	GND		
27	GND		
28	BIN0-	Bport (-)LVDS CH0 differential data input	
29	BIN0+	Bport (+)LVDS CH0 differential data input	
30	BIN1-	Bport (-)LVDS CH1 differential data input	
31	BIN1+	Bport (+)LVDS CH1 differential data input	
32	BIN2-	Bport (-)LVDS CH2 differential data input	
33	BIN2+	Bport (+)LVDS CH2 differential data input	
34	GND		
35	BCK-	Bport LVDS Clock signal(-)	
36	BCK+	Bport LVDS Clock signal(+)	
37	GND		
38	BIN3-	Bport (-)LVDS CH3 differential data input	
39	BIN3+	Bport (+)LVDS CH3 differential data input	
40	BIN4-	Bport (-)LVDS CH4 differential data input	
41	BIN4+	Bport (+)LVDS CH4 differential data input	
42	GND		
43	GND		
44	GND		
45	GND		
46	GND		
47	VCC	+12V Power Supply	
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

CN2 (Interface signals) (Shown in Fig1)

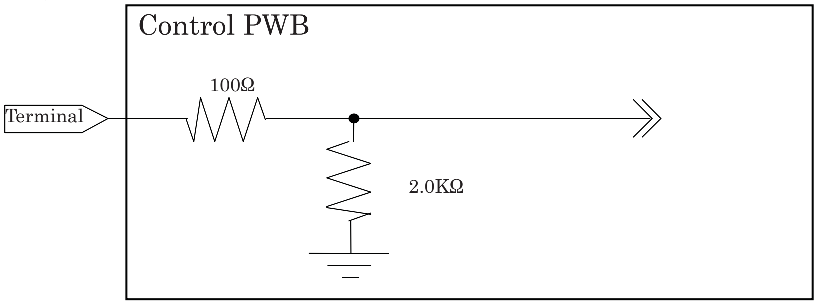
Using connector : FI-RNE41SZ-HF (Japan Aviation Electronics Ind., Ltd.)

Matching connector : FI-RE41HL, FI-RE41CL (Japan Aviation Electronics Ind., Ltd.)

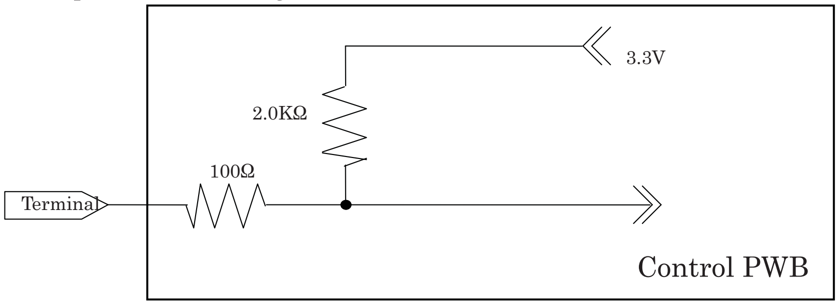
Pin No.	Symbol	Function	Remark
1	Reserved (VCC)	(+12V Power Supply)	
2	Reserved (VCC)	(+12V Power Supply)	
3	Reserved (VCC)	(+12V Power Supply)	
4	Reserved		
5	Reserved		
6	Reserved		
7	Reserved		
8	Reserved		
9	GND		
10	CIN0-	Cport (-)LVDS CH0 differential data input	
11	CIN0+	Cport (+)LVDS CH0 differential data input	
12	CIN1-	Cport (-)LVDS CH1 differential data input	
13	CIN1+	Cport (+)LVDS CH1 differential data input	
14	CIN2-	Cport (-)LVDS CH2 differential data input	
15	CIN2+	Cport (+)LVDS CH2 differential data input	
16	GND		
17	CCK-	Cport LVDS Clock signal(-)	
18	CCK+	Cport LVDS Clock signal(+)	
19	GND		
20	CIN3-	Cport (-)LVDS CH3 differential data input	
21	CIN3+	Cport (+)LVDS CH3 differential data input	
22	CIN4-	Cport (-)LVDS CH4 differential data input	
23	CIN4+	Cport (+)LVDS CH4 differential data input	
24	GND		
25	GND		
26	DIN0-	Dport (-)LVDS CH0 differential data input	
27	DIN0+	Dport (+)LVDS CH0 differential data input	
28	DIN1-	Dport (-)LVDS CH1 differential data input	
29	DIN1+	Dport (+)LVDS CH1 differential data input	
30	DIN2-	Dport (-)LVDS CH2 differential data input	
31	DIN2+	Dport (+)LVDS CH2 differential data input	
32	GND		
33	DCK-	Dport LVDS Clock signal(-)	
34	DCK+	Dport LVDS Clock signal(+)	
35	GND		
36	DIN3-	Dport (-)LVDS CH3 differential data input	
37	DIN3+	Dport (+)LVDS CH3 differential data input	
38	DIN4-	Dport (-)LVDS CH4 differential data input	
39	DIN4+	Dport (+)LVDS CH4 differential data input	
40	GND		
41	GND		

[Note] GND of parts drived a liquid crystal panel drive has connected with a module chassis.

[Note 1]The equivalent circuit figure of the terminal



[Note 2]The equivalent circuit figure of the terminal

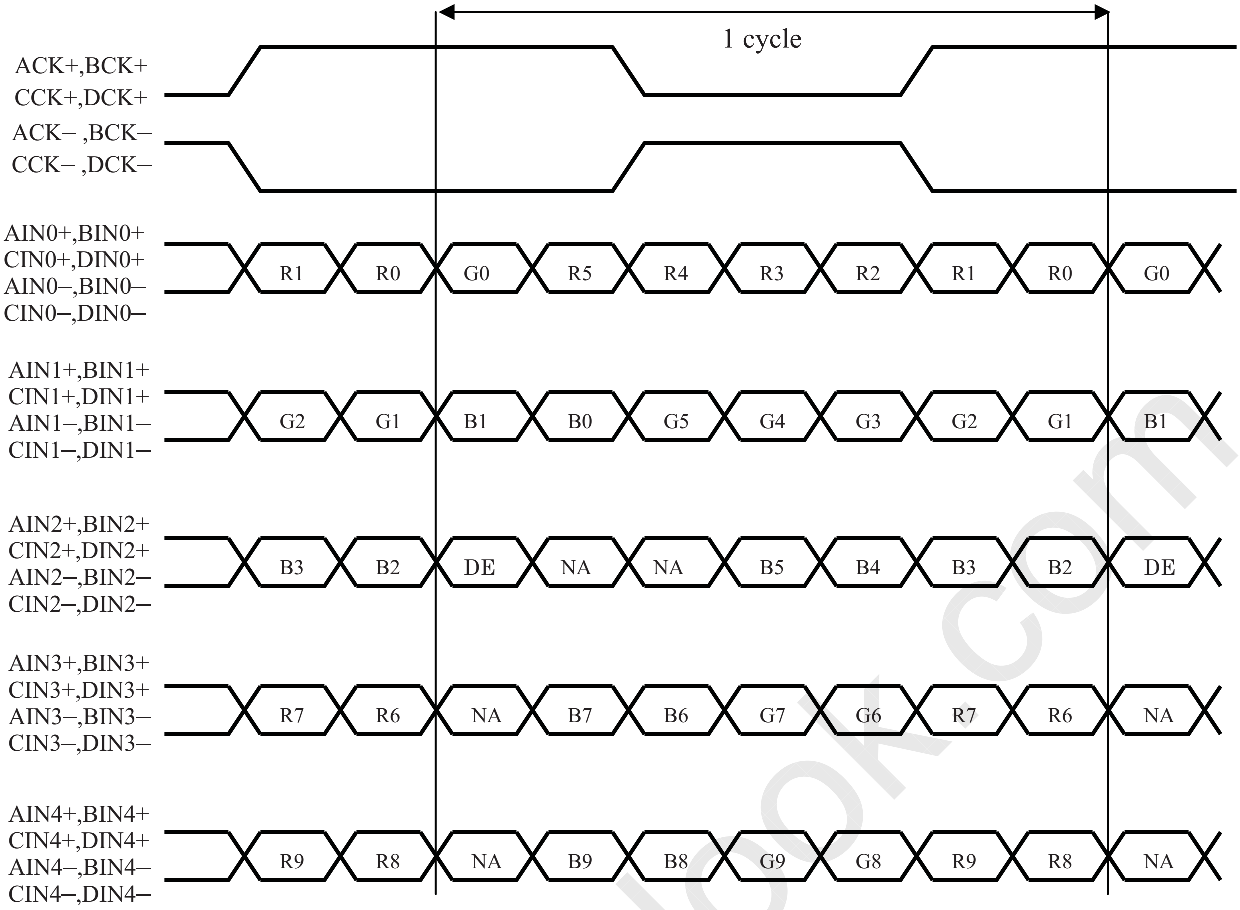


[Note 3] LVDS Data order

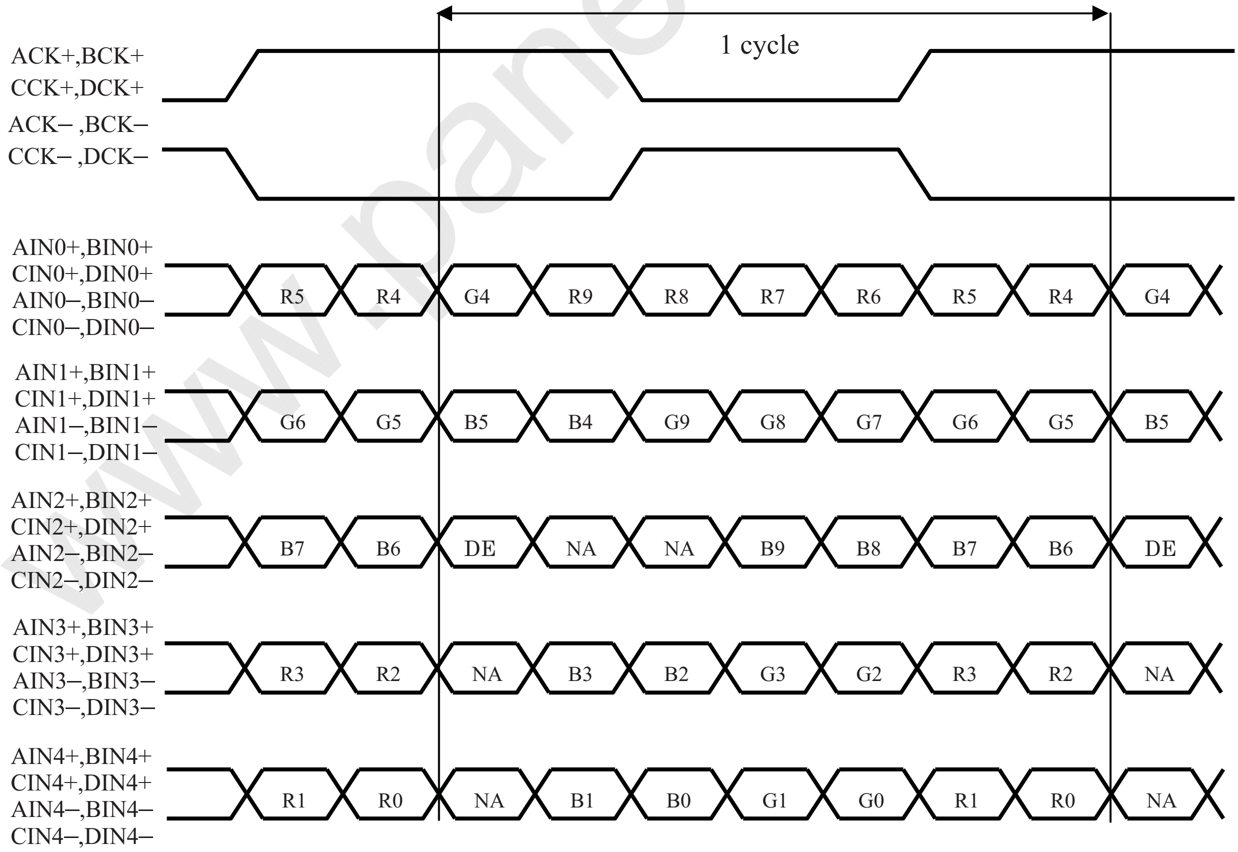
SELLVDS		
Data	L(GND) [VESA]	H(3.3V) or Open [JEIDA]
TA0	R0(LSB)	R4
TA1	R1	R5
TA2	R2	R6
TA3	R3	R7
TA4	R4	R8
TA5	R5	R9(MSB)
TA6	G0(LSB)	G4
TB0	G1	G5
TB1	G2	G6
TB2	G3	G7
TB3	G4	G8
TB4	G5	G9(MSB)
TB5	B0(LSB)	B4
TB6	B1	B5
TC0	B2	B6
TC1	B3	B7
TC2	B4	B8
TC3	B5	B9(MSB)
TC4	NA	NA
TC5	NA	NA
TC6	DE(*)	DE(*)
TD0	R6	R2
TD1	R7	R3
TD2	G6	G2
TD3	G7	G3
TD4	B6	B2
TD5	B7	B3
TD6	N/A	N/A
TE0	R8	R0(LSB)
TE1	R9(MSB)	R1
TE2	G8	G0(LSB)
TE3	G9(MSB)	G1
TE4	B8	B0(LSB)
TE5	B9(MSB)	B1
TE6	N/A	N/A

NA: Not Available
(*)Since the display position is prescribed by the rise of DE(Display Enable)signal, please do not fix DE signal during operation at "High".

SELLVDS= Low (GND)



SELLVDS= High (3.3V) or OPEN



DE: Display Enable, NA: Not Available (Fixed Low)

・Interface block diagram

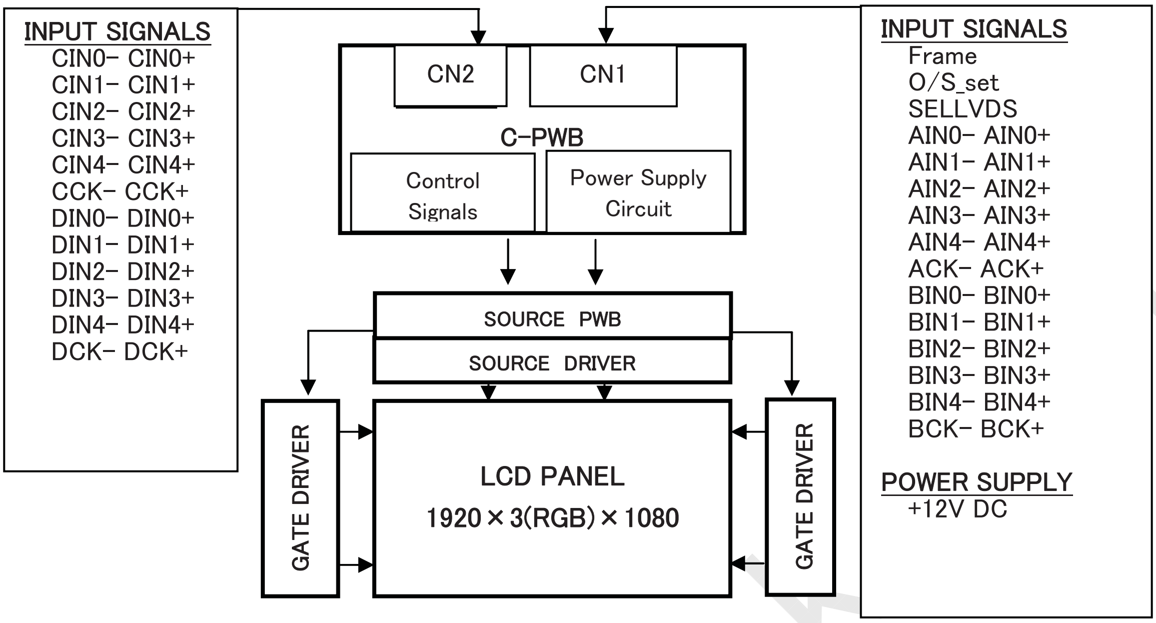


Fig.1 Interface block diagram

4.2 Vcom Adjusting interface of Control PWB SHARP specifies[LK0DZ1C0＊＊＊]

CN2(Interface Vcom Adjusting) [note1]

Using Via Hole : 1.5mm Pitch (ϕ 0.7mm)

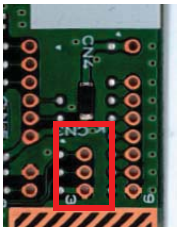
Mating connector : (housing)3P-SZN, (contact)SZN-002T-P0.7K (JST Co.,Ltd.)

Communication method : I2C

Pin No.	Symbol	Function	Remark
1	SDA	I2C DATA	Pull up 3.3V[Note2]
2	SCL	I2C CLK	Pull up 3.3V[Note2]
3	GND		

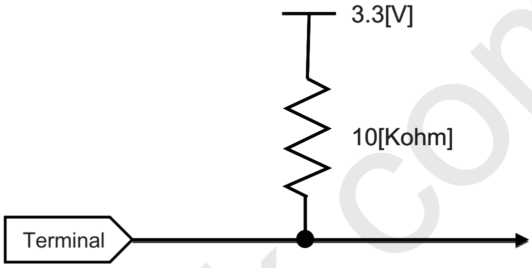
Refer to specifications of ISL24837 for the I2C command of Vcom adjustment.

[Note1]Interface



PinNo	Symbol
1	**SDA**
2	**SCL**
3	**GND**

[Note2] The equivalent circuit figure of the terminal



4.3 Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage (for Control)	V_I	Ta=25 °C	-0.3 ~ 3.6	V	[Note 1]
12V supply voltage (for Control)	VCC	Ta=25 °C	0 ~ + 14	V	
Storage temperature	Tstg	-	-25 ~ +60	°C	[Note 2] [Note 3]
Operation temperature (Ambient)	Topa	-	0 ~ +50	°C	

[Note 1] SELLVDS FRAME, O/S_set,

[Note 2] Humidity 95%RH Max.(Ta≦40°C)

Maximum wet-bulb temperature at 39 °C or less.(Ta>40°C)

No condensation.

[Note 3] Because the operation temperature of IC200 is MAX 105℃, thermally conductive interface Pad is recommended.

Refer to C-PWB specifications for IC200.

4.4 Electrical Characteristics of input signals

Ta=25 °C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+12V supply voltage	Supply voltage	Vcc	11.4	12	12.6	V	[Note 1]
	Current dissipation	Icc	-	700	2000	mA	[Note 2]
	Inrush current	I_{RUSH}	-	6000	-	mA	[Note 7]
Permissible input ripple voltage		V_{RP}	-	-	100	mV_{P-P}	Vcc = +12.0V
Differential input threshold voltage	High	V_{TH}	-	-	100	mV	V_{CM} = +1.2V [Note 6]
	Low	V_{TL}	-100	-	-	mV	
Input Low voltage		V_{IL}	0	-	1.0	V	[Note 3]
Input High voltage		V_{IH}	2.3	3.3	3.6	V	
Input leak current (Low)		I_{IL1}	-	-	400	μA	V_I = 0V [Note 4]
		I_{IL2}	-	-	40	μA	V_I = 0V [Note 5]
Input leak current (High)		I_{IH1}	-	-	40	μA	V_I = 3.3V [Note 4]
		I_{IH2}	-	-	400	μA	V_I = 3.3V [Note 5]
Terminal resistor		R_T	-	100	-	Ω	Differential input

[Note]V_{CM}: Common mode voltage of LVDS driver.

[Note 1]

Input voltage sequences

0 < t1 ≦ 20ms

10 < t2 ≦ 50ms

10 < t3 ≦ 50ms

0 < t4 ≦ 1s

t5 ≧ 1000 ms

t6 ≧ 0

t7 ≧ 300ms

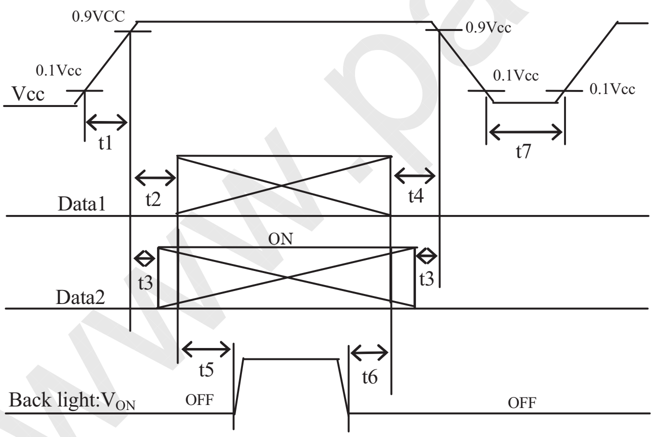
Dip conditions for supply voltage

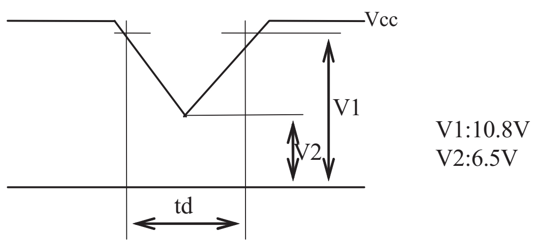
a) 6.5V ≦ Vcc < 10.8V

td ≦ 10ms

b) Vcc < 6.5V

Dip conditions for supply voltage is based on input voltage sequence.





※ Data1: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±,BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4± CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±,DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±

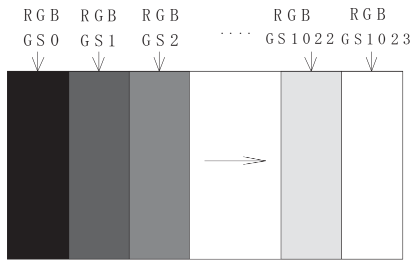
*V_{CM} voltage pursues the sequence mentioned above

※ Data2: SELLVDS, FRAME, O/S_SET

[Note]About the relation between data input and back light lighting, please base on the above-mentioned input sequence. When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

[Note 2] Typical current situation: 1024 gray-bar patterns. (Vcc = +12.0V)

The explanation of RGB gray scale is seen in section 8.



Vcc=+12.0V
CK=74.25MHz
Th=7.41μs

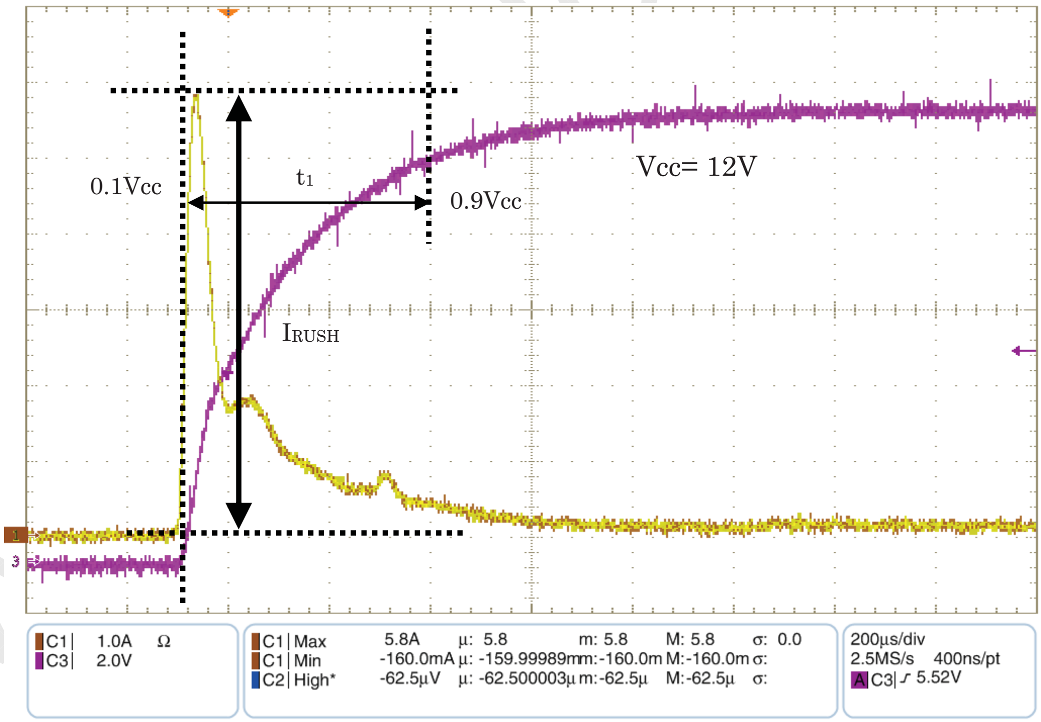
[Note 3] SELLVDS, FRAME, O/S_SET

[Note 4] O/S_SET, SELLVDS

[Note 5] FRAME

[Note 6] ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±,BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4± CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±,DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±

[Note 7] Vcc12V inrush current waveform (This figure is I_{RUSH} : t_1=500 μ s)



200 μ s/div

4.5 Timing characteristics of input signals for C-PWB

Timing diagrams of input signal are shown in Fig.2.

<table>
<tr><th colspan="2">Parameter</th><th>Symbol</th><th>Min.</th><th colspan="2">Typ.</th><th>Max.</th><th>Unit</th><th>Remark</th></tr>
<tr><td>Clock</td><td>Frequency</td><td>1/Tc</td><td>69</td><td colspan="2">74.25</td><td>76</td><td>MHz</td><td></td></tr>
<tr><td rowspan="6">Data enable signal</td><td rowspan="2">Horizontal period</td><td rowspan="2">TH</td><td>542</td><td colspan="2">550</td><td>600</td><td>clock</td><td></td></tr>
<tr><td>7.3</td><td colspan="2">7.41</td><td>8.1</td><td>μs</td><td></td></tr>
<tr><td>Horizontal period (High)</td><td>THd</td><td>480</td><td colspan="2">480</td><td>480</td><td>clock</td><td></td></tr>
<tr><td rowspan="2">Vertical period</td><td rowspan="2">TV</td><td>1096</td><td>1350</td><td>1125</td><td>1400</td><td>line</td><td></td></tr>
<tr><td>88.2</td><td>100</td><td>120</td><td>123.10</td><td>Hz</td><td></td></tr>
<tr><td>Vertical period (High)</td><td>TVd</td><td>1080</td><td colspan="2">1080</td><td>1080</td><td>line</td><td></td></tr>
</table>

[Note]-When vertical period is very long, flicker and etc. may occur.

-Please turn off the module after it shows the black screen.

-Please make sure that length of vertical period should become of an integral multiple of horizontal length of period. Otherwise, the screen may not display properly.

-As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.

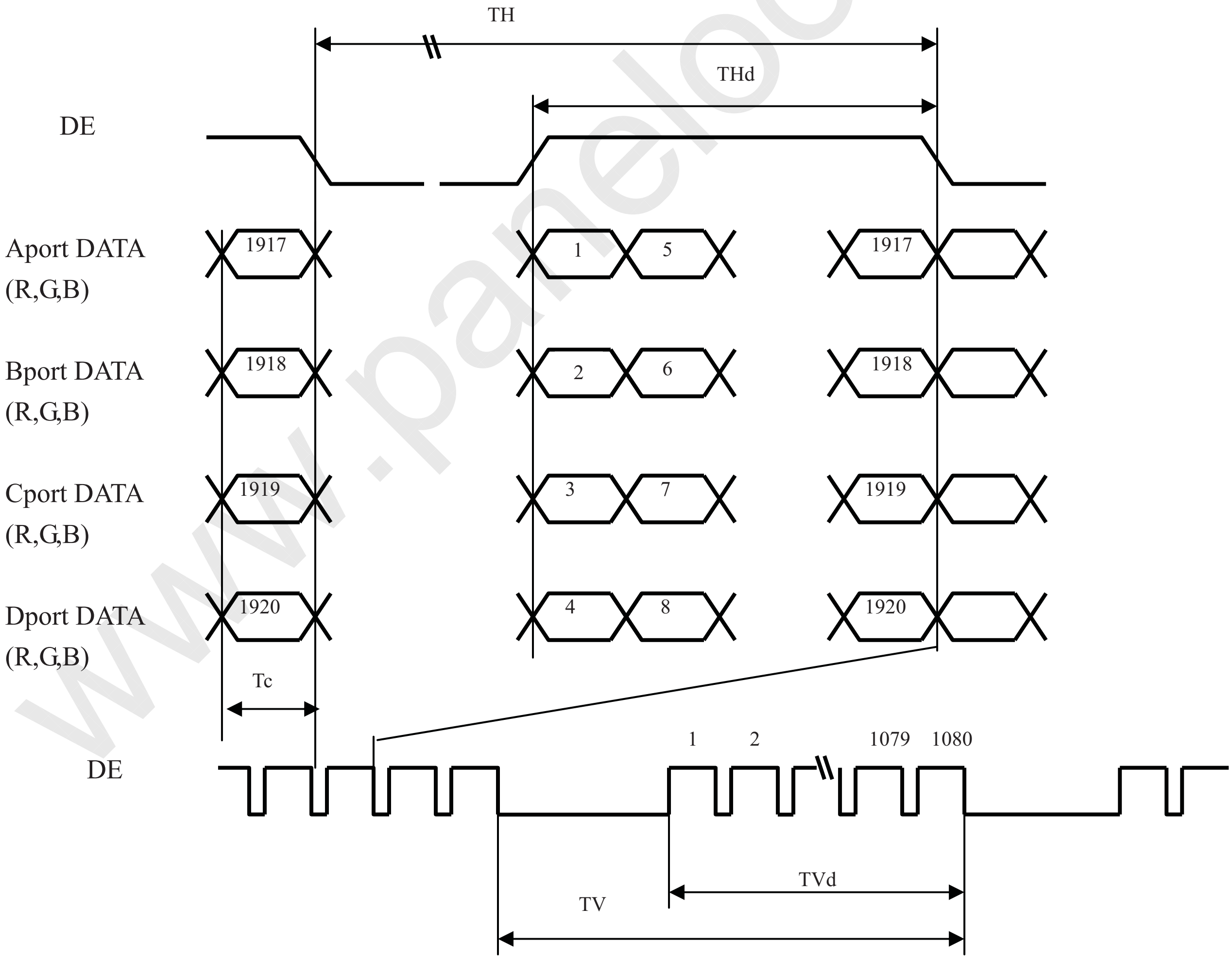
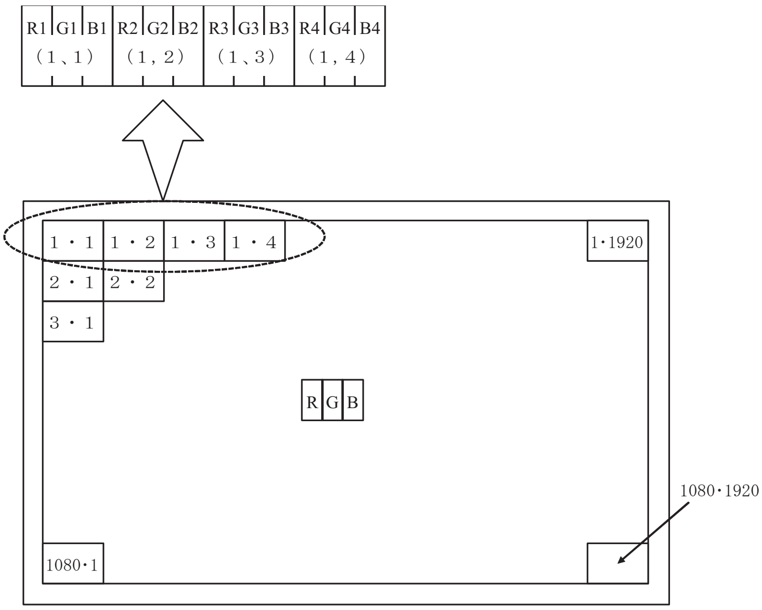


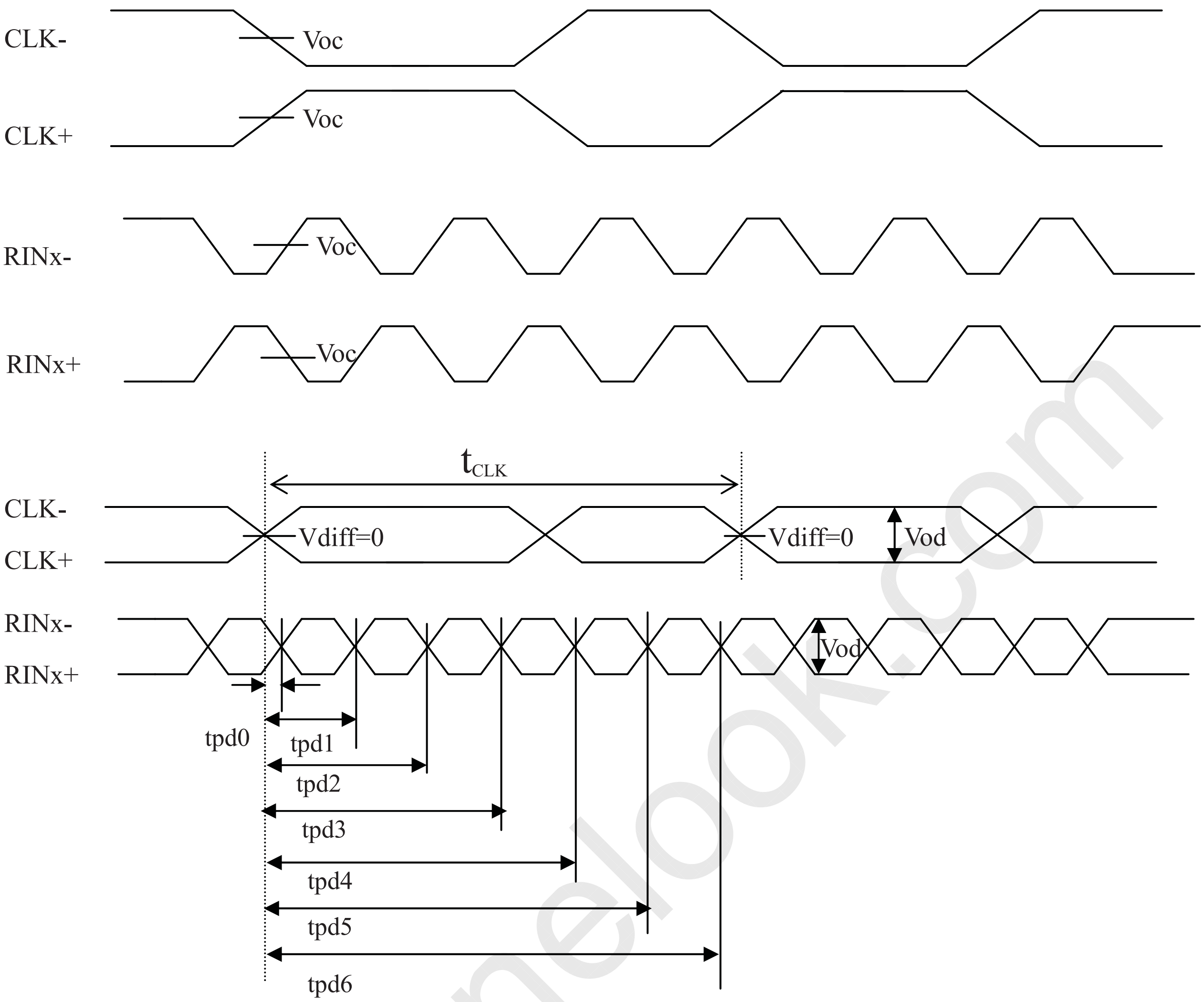
Fig.2.Timing characteristics of input signal

4.6 Input data signal and display position on the screen



Display position of Dat (V,H)

4.7 LVDS signal characteristics



The item		Symbol	min.	typ.	max.	unit
Differential voltage		Vod	200	400	600	mV
Common mode voltage		Voc	Vod/2	1200	2400－Vod/2	
LVDS clock period		t_{CLK}	12.35	13.50	13.69	ns
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	-0.25	0	0.25	
	Delay time, CLK rising edge to serial bit position 1	tpd1	$1*t_{CLK}/7-0.25$	$1*t_{CLK}/7$	$1*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 2	tpd2	$2*t_{CLK}/7-0.25$	$2*t_{CLK}/7$	$2*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 3	tpd3	$3*t_{CLK}/7-0.25$	$3*t_{CLK}/7$	$3*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 4	tpd4	$4*t_{CLK}/7-0.25$	$4*t_{CLK}/7$	$4*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 5	tpd5	$5*t_{CLK}/7-0.25$	$5*t_{CLK}/7$	$5*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 6	tpd6	$6*t_{CLK}$ 7-0.25	$6*t_{CLK}/7$	$6*t_{CLK}/7+0.25$	

5 Input Signal, Basic Display Color and Gray scale of Each Color

	Colors & Gray scale	Gray Scale	Data signal																													
			R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	GS1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	⇩	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage.

Each basic color can be displayed in 1024 gray scales from 10 bits data signals. According to the combination of total 30 bits data signals, one billion-color display can be achieved on the screen.

6 Optical Specifications

6.1 Optical characteristics (Reference value)

Ta=25°C, Vcc=12.0V, Timing:120Hz(typ. value)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21 θ22	CR≧10	70	88	-	Deg.	[Note1,4]
	Vertical	θ11 θ12		70	88	-	Deg.	
Contrast ratio		CRn	θ=0 deg.	-	5000	-	-	[Note2,4]
Response time		τ_{DRV}			4		ms	[Note3,4,5]
Luminance	White	x		Typ.-0.03	0.278	Typ.+0.03	-	[Note4]
		y		Typ.-0.03	0.285	Typ.+0.03	-	
	Red	x		Typ.-0.03	0.644	Typ.+0.03	-	
		y		Typ.-0.03	0.344	Typ.+0.03	-	
	Green	x		Typ.-0.03	0.284	Typ.+0.03	-	
		y		Typ.-0.03	0.607	Typ.+0.03	-	
	Blue	x		Typ.-0.03	0.147	Typ.+0.03	-	
		y		Typ.-0.03	0.069	Typ.+0.03	-	
Transmittance		T	θ=0 deg.	-	6.16	-	%	
Luminance uniformity	White	δw		-	-	1.25		[Note 6]

-Optical characteristics are based on SHARP standard module LK400D3LA14

-The measurement shall be executed 60 minutes after lighting at rating.

[Note]The optical characteristics are measured using the following equipment.

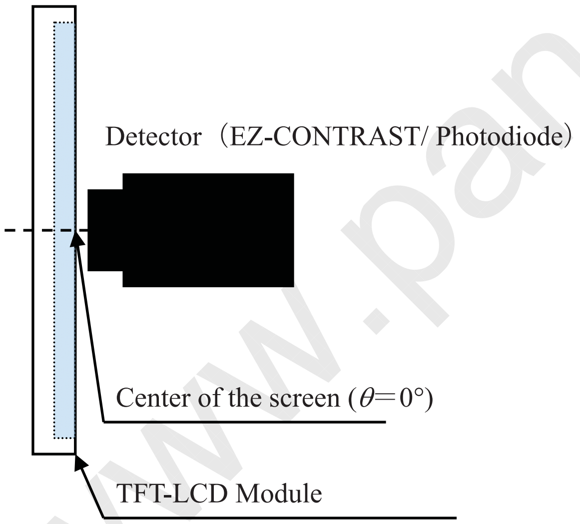


Fig.3-1 Measurement of viewing angle range and Response time.

Viewing angle range: EZ-CONTRAST

Response time: Photodiode

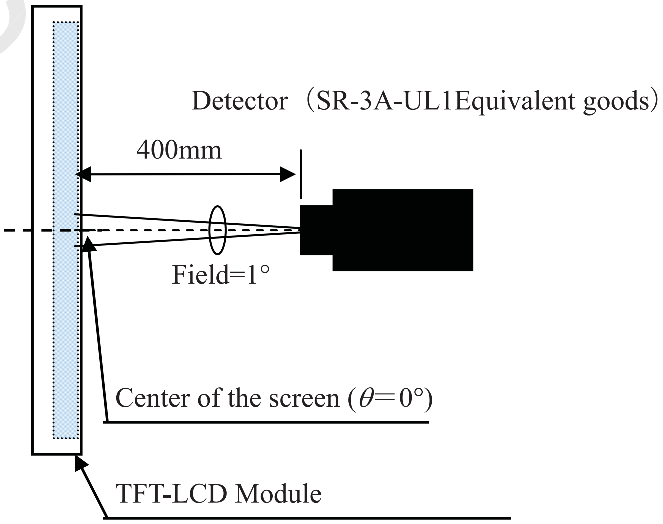
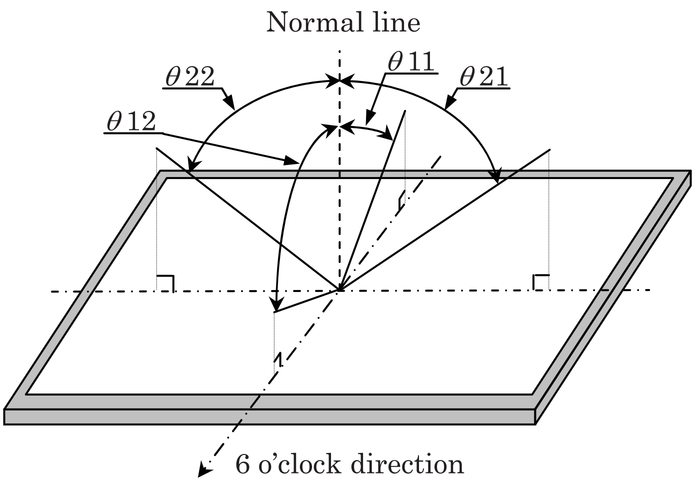


Fig.3-2 Measurement of Contrast, Luminance, Chromaticity.

[Note 1]Definitions of viewing angle range :



[Note 2]Definition of contrast ratio :

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

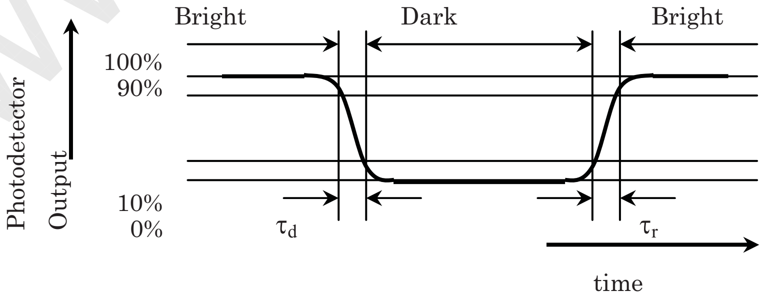
[Note 3]Definition of response time

The response time (τ_d and τ_r) is defined as the following figure and shall be measured by switching the input signal for "any level of gray (0%, 25%, 50%, 75% and 100%)" and "any level of gray (0%, 25%, 50%, 75% and 100%)".

	0%	25%	50%	75%	100%
0%		tr:0%-25%	tr:0%-50%	tr:0%-75%	tr:0%-100%
25%	td: 25%-0%		tr: 25%-50%	tr25%-75%	tr: 25%-100%
50%	td: 50%-0%	td: 50%-25%		tr: 50%-75%	tr: 50%-100%
75%	td: 75%-0%	td: 75%-25%	td: 75%-50%		tr: 75%-100%
100%	td: 100%-0%	td: 100%-25%	td: 100%-50%	td:100%-75%	

t*:x-y...response time from level of gray(x) to level of gray(y)

$\tau_r = \Sigma(\text{tr:x-y})/10$, $\tau_d = \Sigma(\text{td:x-y})/10$



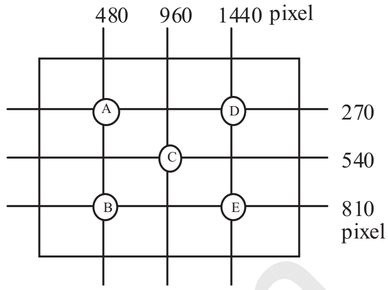
[Note 4]This shall be measured at center of the screen.

[Note 5] This value is valid when O/S driving is used at typical input time value.

[Note 6]Definition of white uniformity ;

White uniformity is defined as the following with five measurements. (A~E)

$$\delta w = \frac{\text{Maximum luminance of five points (brightness)}}{\text{Minimum luminance of five points (brightness)}}$$



7 Shipping and Packing

7.1 Packing form

a) Piling number of cell boxes : 14cell box/1 palette

b) Packing quantity in one cell box :10pcs

c) Carton size :1360(W)×112(D)×1063(H)

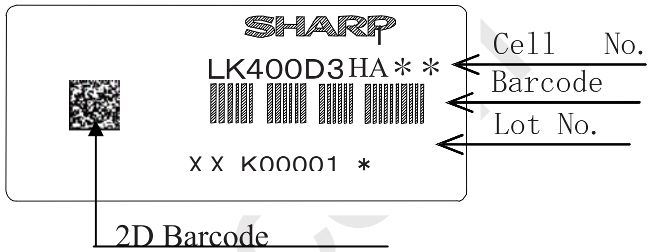
d) Total mass of one carton filled with full cell :428.5kg Max

7.2 Label

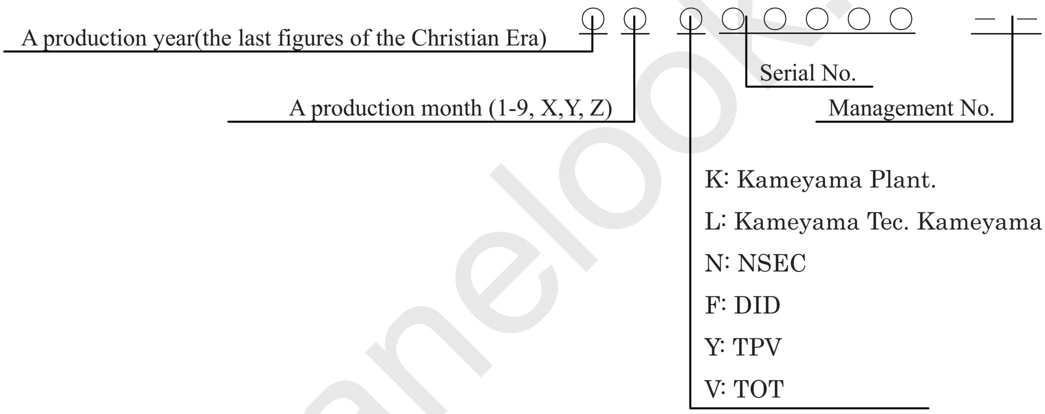
a) Cell Label

This label is stuck on the protection film of front polarizer.

【LK400D3HA＊＊】 JAPAN PRODUCTION



How to express Lot No.

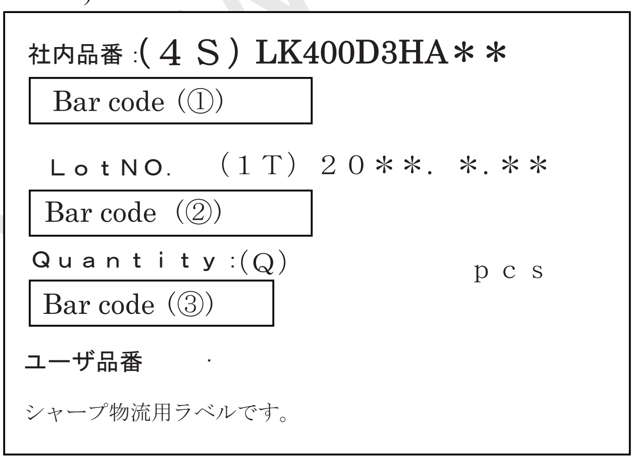


b) Packing Label

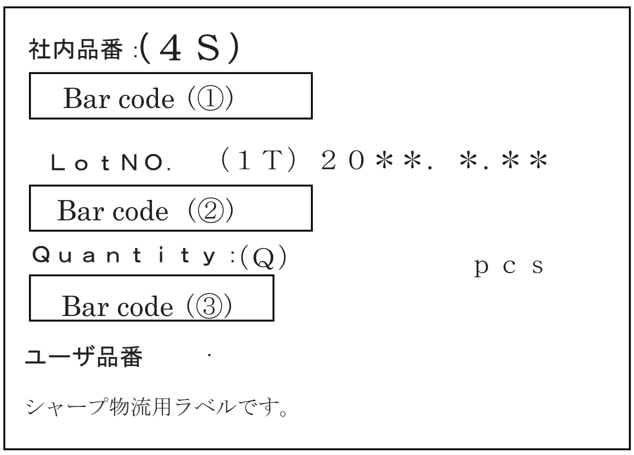
This Label is stuck on the packing case(cell box) and carton.

[LK400D3HA＊＊]

b-1)Cell box



b-2)Carton



①Management No

②Lot No.(Date)

③Quantity

8 Carton storage condition.

Temperature 0°C to 40°C

Humidity 95%RH or less

Reference condition : 20°C to 35°C, 85%RH or less (summer)

: 5°C to 15°C, 85%RH or less (winter)

· the total storage time (40°C, 95%RH) : 240H or less

Sunlight Be sure to shelter a product from the direct sunlight.

Atmosphere Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.

Notes Be sure to put cartons on palette or base, don't put it on floor, and store them with removing from wall

Please take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment

Storage life 1 year

9 Reliability

Reliability test item

No.	Test item	Condition
1	High temperature storage test	Ta=60°C 240h
2	Low temperature storage test	Ta=-25°C 240h
3	High temperature and high humidity operation test	Ta=40°C ; 95%RH 240h (No condensation)
4	High temperature operation test	Ta=50°C 240h
5	Low temperature operation test	Ta=0°C 240h

Above tests are executed under the CCFL module conditions.

10 Precautions

a) Since the polarizer is easily damaged, pay attention not to scratch it.

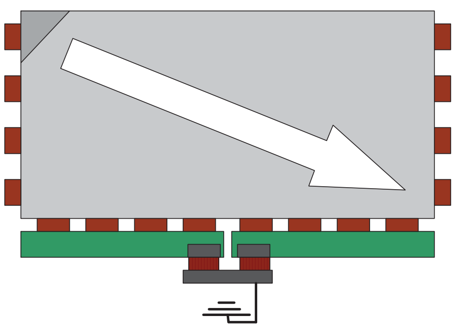
b) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.

c) When the polarizer is soiled, wipe it with absorbent cotton or other soft cloth.

d) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

e) Precautions of peeling off the protection film.

- Be sure to peel off slowly (recommended more than 7sec) and constant speed.
- Peeling direction shows Fig.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to ground S-PWB while peeling of the protection film.
- Ionized air should be blown over during peeling action.
- The protection film must not touch drivers and S-PWBs.
- If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.



f) Since the Open Cell consists of TFT and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharges, persons who are handling the Open Cell should be grounded through adequate methods such as the anti-static wrist band. Connector pins should not be touched directly with bare hands.

- Reference : Process control standard of sharp

	Item	Management standard value and performance standard
1	Anti-static mat (floor)	1 to 50 [M ohm]
2	Anti-static mat (shelf, desk)	1 to 100 [M ohm]
3	Ionizer	Attenuate from ±1000V to ±100V within 2 sec
4	Anti-static wrist band	0.8 to 10 [M ohm]
5	Anti-static wrist band entry and ground resistance	Below 1000 [ohm]
6	Temperature	22 to 26 [°C]
7	Humidity	60 to 70 [%RH]

g) The Open Cell has some PWBs, take care to keep them from any stress or pressure when handling or installing the Open Cell, otherwise some of electronic parts on the PWBs may be damaged.

h) Be sure to turn off the power supply when inserting or disconnecting the cable.

i) Be sure to design the module and cabinet so that the Open Cell can be installed without any extra stress such as warp or twist.

j) When handling the Open Cell and assembling them into module and cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open Cell.

k) Applying too much force and stress to PWB and driver may cause a malfunction electrically and mechanically.

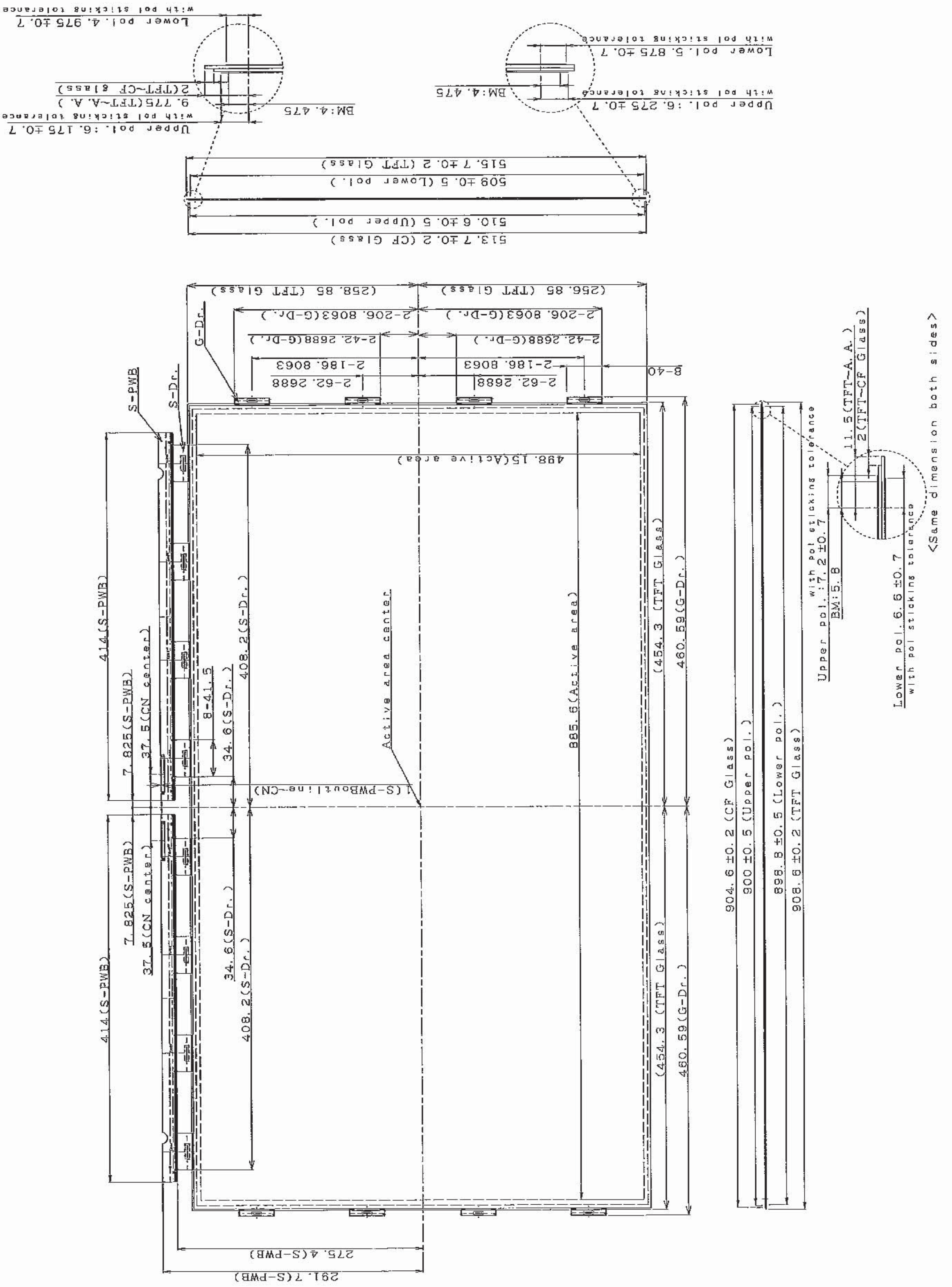
l) The Open Cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufacturers.

m) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

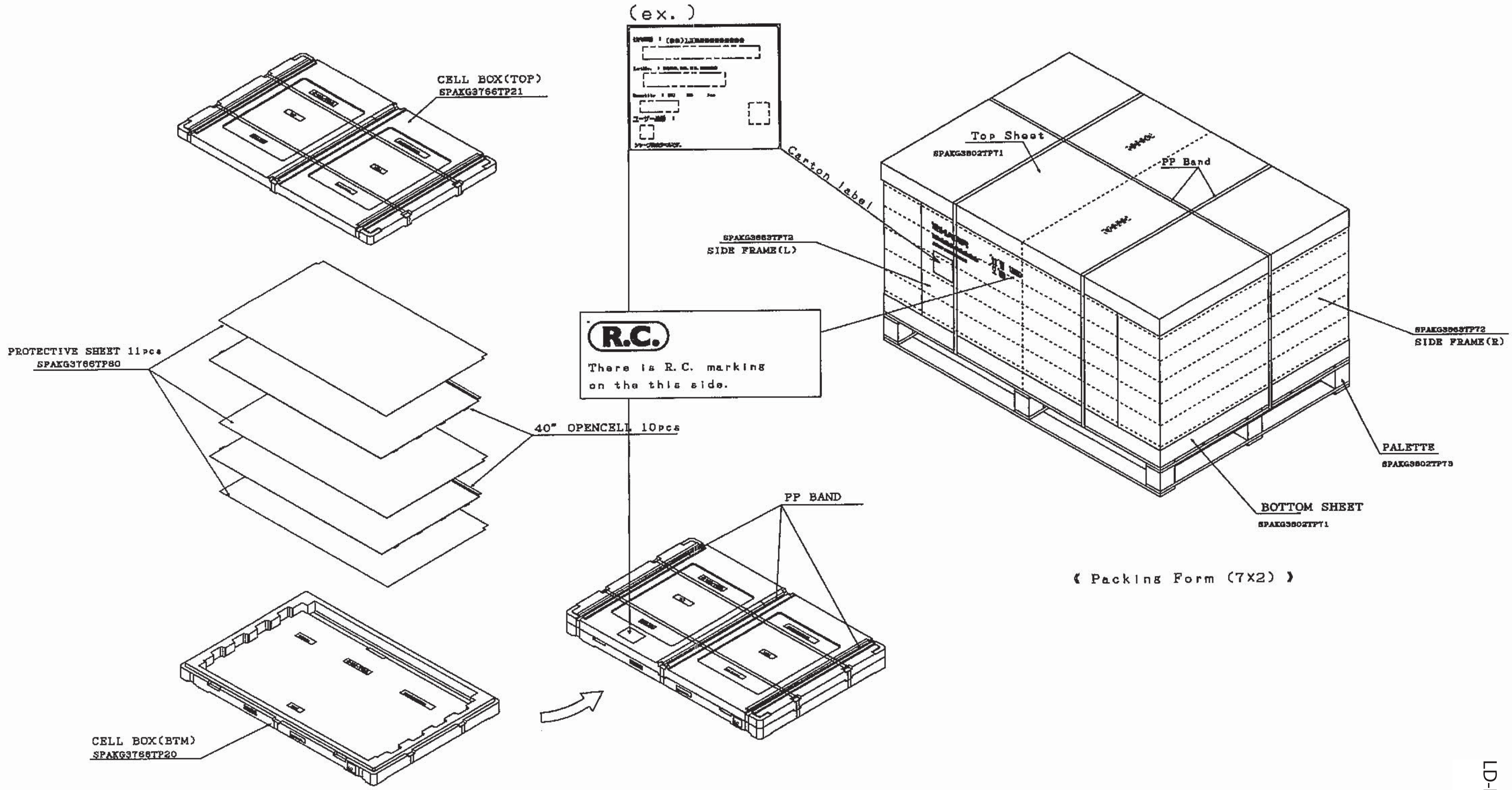
n) The chemical compound, which causes the destruction of ozone layer, is not used.

o) This Open Cell is corresponded to RoHS. “R.C.” label on the side of palette shows it.

p) When any question or issue occurs, it shall be solved by mutual discussion.



Outline dimensions of LK400D3HAxx



40INCH OPENCELL Packing Form