SHARP

No.	LD-K25750
DATE	July. 24. 2013

TECHNICAL LITERATURE

FOR

TFT-LCD Open Cell

MODEL No. LK400D3HC84M

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DISPLAY DEVICE UNIT 5

DISPLAY DEVICE BUSINESS DIVISION

SHARP CORPORATION

RECORDS OF REVISION

MODEL No. : LK400D3HC84M

TL No. : LD-K25750

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-K25750	2013.7.24	-	-	-	1st ISSUE

1. Application

This technical literature applies to the color 40.0" TFT-LCD Open Cell LK400D3HC84M.

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2. Overview

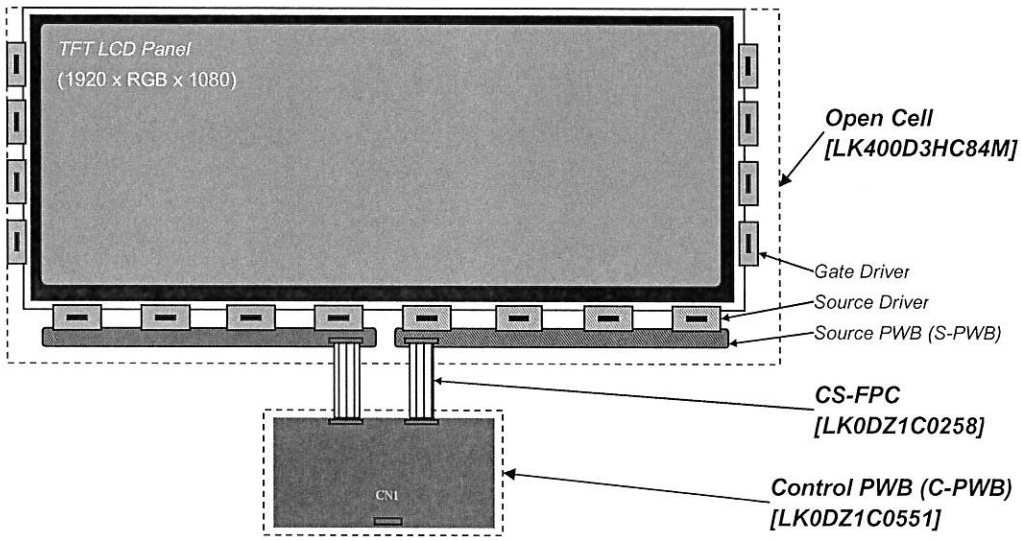
This Open Cell is color active matrix LCD Open Cell incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs and Source PWB.

The following contents can be achieved in using LK0DZ1C0551 (C-PWB) and LK0DZ1C0258 (CS-FPC) that SHARP specifies.

Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with one billion colors by using 10bit (8bit+2FRC) LVDS (Low Voltage Differential Signaling) to interface, +12V of DC supply voltages.

And in order to improve the response time of LCD, this module applies the Over Shoot driving (O/S driving) technology for the control circuit. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.



3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	101.609 (Diagonal)	cm
	40.0036 (Diagonal)	inch
Active area	885.60 (H) x 498.15 (V)	mm
Pixel Format	1920 (H) x 1080 (V) (1pixel = R + G + B dot)	pixel
Pixel pitch	0.461250 (H) x 0.461250 (V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Open Cell Outline Dimensions [Note1]	921.18(W)x 548.55(H) x1.82 (D)	mm
Mass	1.88 ± 0.3	kg
Surface treatment [Note2]	- Front polarizer: Low Haze, Anti Glare Hard coating: 2H and more - Rear polarizer: Hard coating less	

[Note1] Outline dimensions are shown in P20.
[Note2] With the protection film removed.

4. Open Cell Driving Specifications

4.1. Driving interface of C-PWB SHARP specifies [LK0DZ1C0551]

CN1 (Interface signals and +12V DC power supply) shown in Fig.1

Using connector : 91213-0510 (Aces Electronics Co., Ltd.)

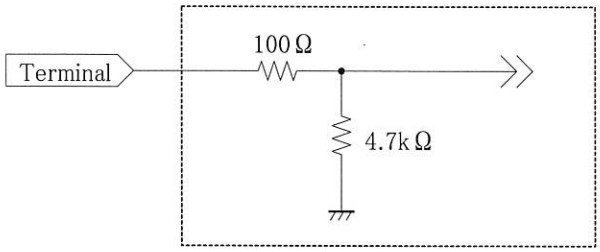
Mating connector : FI-RE51HL, FI-RE51CL (Japan Aviation Electronics Ind., Ltd.) or equivalent device

Matching LVDS transmitter : THC63LVD1023 or equivalent device

Pin No.	Symbol	Function	Remark
1	GND		
2	Reserved	It is required to set non-connection(OPEN)	
3	Reserved	It is required to set non-connection(OPEN)	
4	Reserved	It is required to set non-connection(OPEN)	
5	Reserved	It is required to set non-connection(OPEN)	
6	Reserved	It is required to set non-connection(OPEN)	
7	SELLVDS	Select LVDS data order [Note 1,2]	Pull down
8	Reserved	It is required to set non-connection(OPEN)	
9	Reserved	It is required to set non-connection(OPEN)	
10	Reserved	It is required to set non-connection(OPEN)	
11	GND		
12	AIN0-	Aport (-)LVDS CH0 differential data input	
13	AIN0+	Aport (+)LVDS CH0 differential data input	
14	AIN1-	Aport (-)LVDS CH1 differential data input	
15	AIN1+	Aport (+)LVDS CH1 differential data input	
16	AIN2-	Aport (-)LVDS CH2 differential data input	
17	AIN2+	Aport (+)LVDS CH2 differential data input	
18	GND		
19	ACK-	Aport LVDS Clock signal(-)	
20	ACK+	Aport LVDS Clock signal(+)	
21	GND		
22	AIN3-	Aport (-)LVDS CH3 differential data input	
23	AIN3+	Aport (+)LVDS CH3 differential data input	
24	AIN4-	Aport (-)LVDS CH4 differential data input	
25	AIN4+	Aport (+)LVDS CH4 differential data input	
26	GND		
27	GND		
28	BIN0-	Bport (-)LVDS CH0 differential data input	
29	BIN0+	Bport (+)LVDS CH0 differential data input	
30	BIN1-	Bport (-)LVDS CH1 differential data input	
31	BIN1+	Bport (+)LVDS CH1 differential data input	
32	BIN2-	Bport (-)LVDS CH2 differential data input	
33	BIN2+	Bport (+)LVDS CH2 differential data input	
34	GND		
35	BCK-	Bport LVDS Clock signal(-)	
36	BCK+	Bport LVDS Clock signal(+)	
37	GND		
38	BIN3-	Bport (-)LVDS CH3 differential data input	
39	BIN3+	Bport (+)LVDS CH3 differential data input	
40	BIN4-	Bport (-)LVDS CH4 differential data input	
41	BIN4+	Bport (+)LVDS CH4 differential data input	
42	GND		
43	GND		
44	GND		
45	GND		
46	GND		
47	VCC	+12V Power Supply	
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

[Note] You should connect GND plane in Control PWB to module chassis.

[Note 1] The equivalent circuit figure of the terminal:



Control PWB

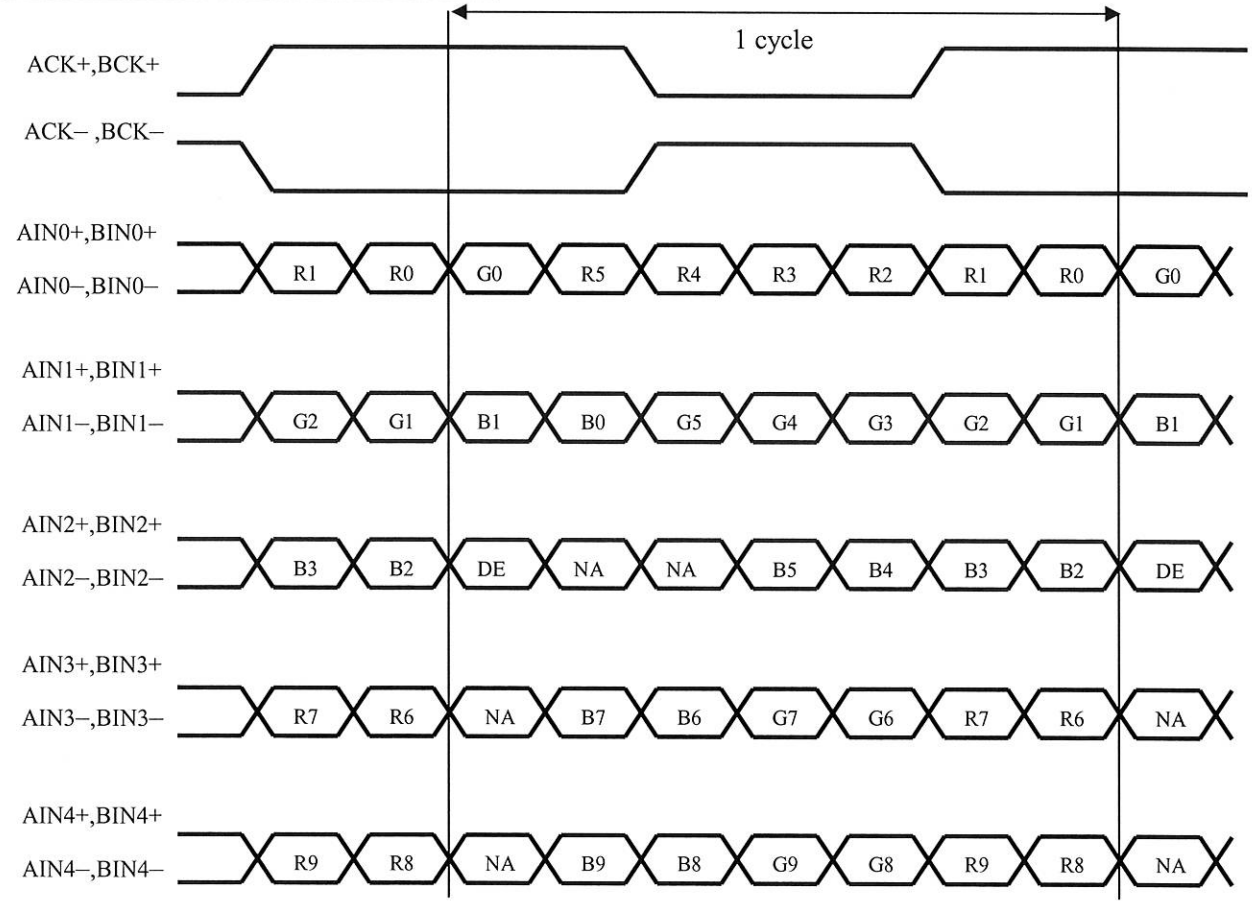
[Note 2] LVDS Data order

SELLVDS		
Data	L(GND) or Open [VESA]	H(3.3V) [JEIDA]
TA0	R0(LSB)	R4
TA1	R1	R5
TA2	R2	R6
TA3	R3	R7
TA4	R4	R8
TA5	R5	R9(MSB)
TA6	G0(LSB)	G4
TB0	G1	G5
TB1	G2	G6
TB2	G3	G7
TB3	G4	G8
TB4	G5	G9(MSB)
TB5	B0(LSB)	B4
TB6	B1	B5
TC0	B2	B6
TC1	B3	B7
TC2	B4	B8
TC3	B5	B9(MSB)
TC4	NA	NA
TC5	NA	NA
TC6	DE(*)	DE(*)
TD0	R6	R2
TD1	R7	R3
TD2	G6	G2
TD3	G7	G3
TD4	B6	B2
TD5	B7	B3
TD6	N/A	N/A
TE0	R8	R0(LSB)
TE1	R9(MSB)	R1
TE2	G8	G0(LSB)
TE3	G9(MSB)	G1
TE4	B8	B0(LSB)
TE5	B9(MSB)	B1
TE6	N/A	N/A

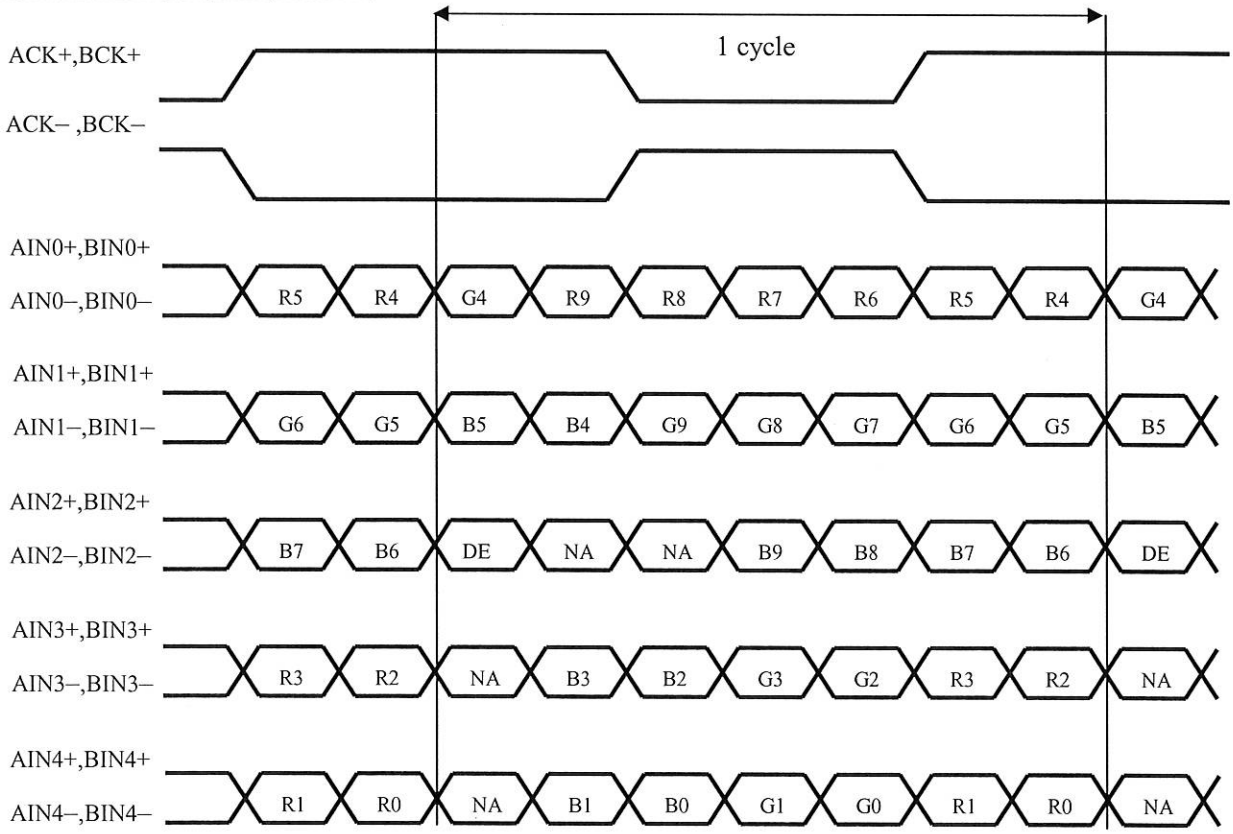
NA: Not Available

(*)Since the display position is prescribed by the rise of DE(Display Enable)signal, please do not fix DE signal at "High" during operation. And you should input DE signal in all LVDS port.

SELLVDS= Low (GND) or OPEN : VESA



SELLVDS= High (3.3V) : JEIDA



DE: Display Enable, NA: Not Available (Fixed Low)

・Interface block diagram

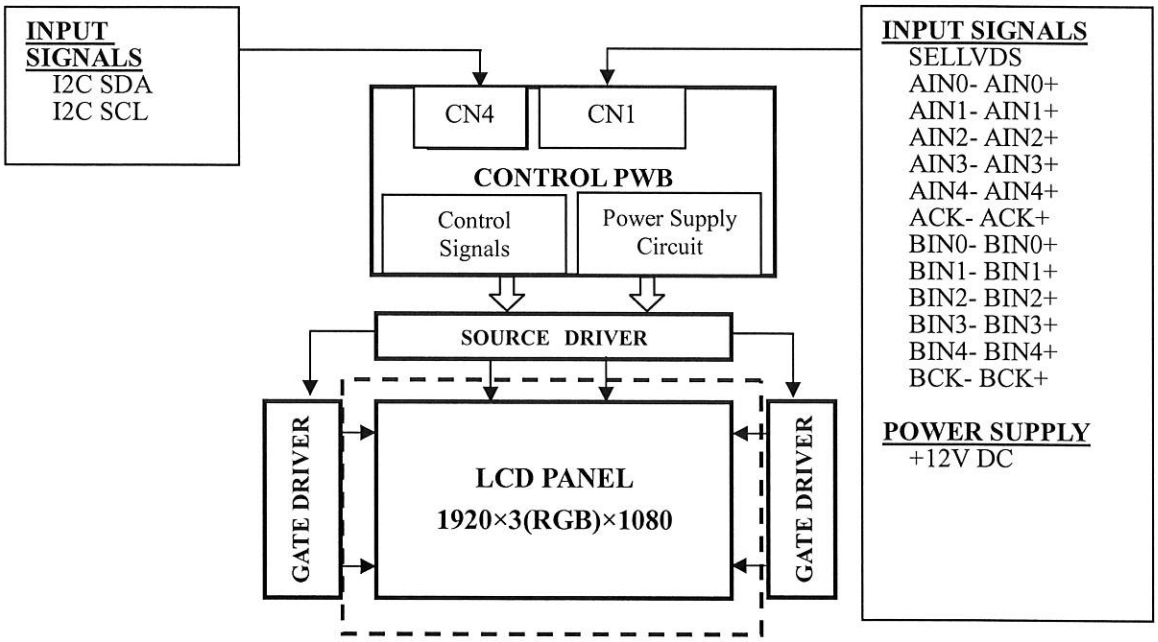


Fig.3 Interface block diagram

4.2. Vcom adjustment

For the prevention of long-time image sticking of TFT-LCD panel, be sure to adjust Vcom flicker to be minimized on the center of display by visual or flicker meter.

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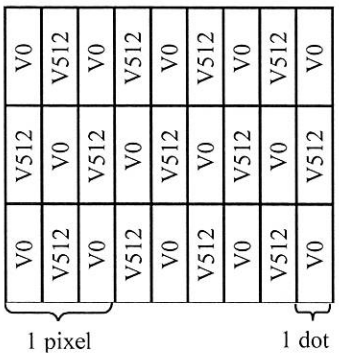
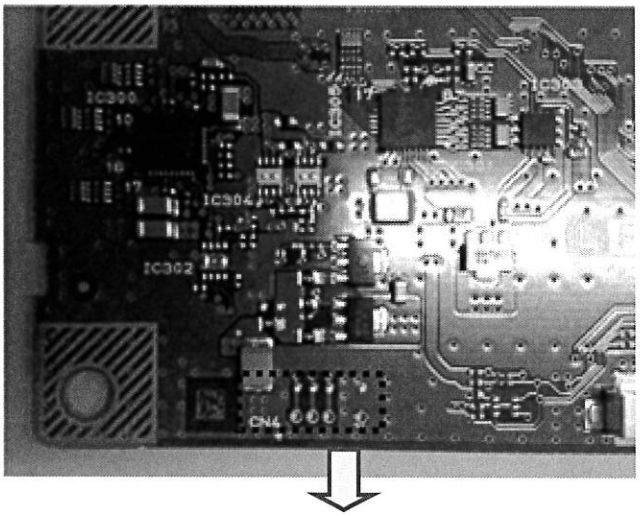
[Note 1] Please adjust VCOM voltage at below pattern:



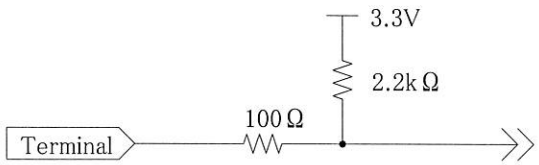
[Note 2] VCOM voltage can be adjusted through via hole (CN4). Potentiometer IC and via hole are as follows:

IC for adjusting VCOM	: ISL24837A (Intersil)
Using Via Hole	: 1.5mm Pitch (ϕ 0.7mm)
Mating connector	: (housing)5P-SZN, (contact)SZN-002T-P0.7K (JST Co.,Ltd.)
Communication method	: I2C



CN4 Pin No.	symbol	Function	Remark
1	SCL	I2C CLK	Pull up:3.3V[Note3]
2	SDA	I2C DATA	Pull up:3.3V[Note3]
3	BUS_EN	—	Required to set NC
4	—	—	
5	GND	GND	-

[Note3] The equivalent circuit figure of the terminal



4.3. Absolute maximum ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage	V_I	Ta=25°C	-0.3 ~ 3.6	V	[Note 1]
12V supply voltage	VCC	Ta=25°C	0 ~ +14	V	
Storage temperature	Tstg	-	-25 ~ +60	°C	[Note 2]
Operation temperature	Topa	-	0 ~ +50	°C	

[Note1] Applies to the input signals to C-PWB

LVDS_SEL

[Note2] Applies to the LK400D3HC84M (OpenCell) and C-PWB, CS-FPC

- Humidity: 95%RH Max.(Ta ≦ 40°C)
- Maximum wet-bulb temperature at 39°C or less. (Ta > 40°C)
- No condensation.

4.4. Electrical characteristics of input signals

Ta=25°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+12V supply voltage	Supply voltage	Vcc	11.4	12	12.6	V	[Note 1]
	Current dissipation	Icc	-	(0.56)	(1.4)	A	[Note 2]
	Inrush current	$I_{RUSH}1$	-	(4.0)	-	A	t1=500us [Note 4]
Permissible input ripple voltage		V_{RP}	-	-	300	mV_{P-P}	Vcc = +12.0V
Differential input threshold voltage	High	V_{TH}	-	-	100	mV	V_{CM} = +1.2V [Note 3]
	Low	V_{TL}	-100	-	-	mV	
Input Low voltage		V_{IL}	0	-	0.7	V	SELLVDS
Input High voltage		V_{IH}	2.3	3.3	3.6	V	
Input leak current (Low)		I_{IL}	-	-	1500	μA	V_I= 0V SCL,SDA
Input leak current (High)		I_{IH}	-	-	700	μA	V_I= 3.3V SELLVDS
Terminal resistor		R_T	-	100	-	Ω	Differential input

[Note] V_{CM}: Common mode voltage of LVDS driver.

[Note1]

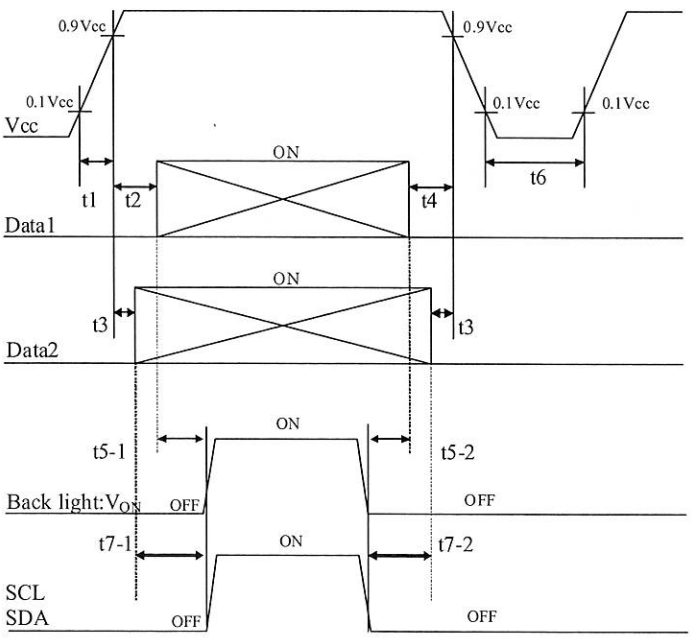
Input voltage sequences

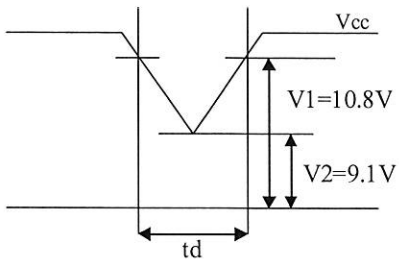
50us < t1 < 20ms
20ms < t2 < 50ms
20ms < t3 < 50ms
0 < t_4 < 1s
700ms < t_{5-1} 1s < t_{5-2}
1s < t_6
1s < t_{7-1} 1s < t_{7-2}

Dip conditions for supply voltage

9.1V ≦ Vcc < 10.8V
td < 10ms

This case is based on input voltage sequences.



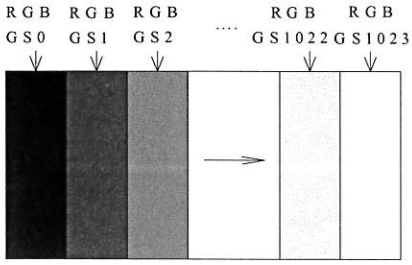


※ Data1: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±,BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±

※ Data2: SELLVDS

[Note] About the relation between data input and back light lighting, please base on the above-mentioned input sequence. When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

[Note2] Typical current situation: 1024 gray-bar patterns. (Vcc = +12.0V)
The explanation of RGB gray scale is seen in section 4.8.



Vcc = +12.0V
1/Tc = 74.25MHz
TH = 14.8μs
TV = 60Hz

[Note 3] ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±
[Note 4] (TBD)

4.5. Timing characteristics of input signals

Timing diagrams of input signal are shown in below figure.

Parameter		Symbol	Min.	Typ.		Max.	Unit
				NTSC	PAL		
Clock	Frequency	1/Tc	69	74.25		76	MHz
Data enable signal	Horizontal period	TH	1050	1100		1300	clock
			14.2	14.8		16.1	μs
	Horizontal period (High)	THd	960	960		960	clock
	Vertical period	TV	1109	1125	1350	1400	line
			47	60	50	63	Hz
	Vertical period (High)	TVd	1080	1080		1080	line

[Note]-When vertical period is very long, flicker and etc. may occur.

-Please turn off the module after it shows the black screen.

-Please make sure that length of vertical period should become of an integral multiple of horizontal length of period. Otherwise, the screen may not display properly.

-As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.

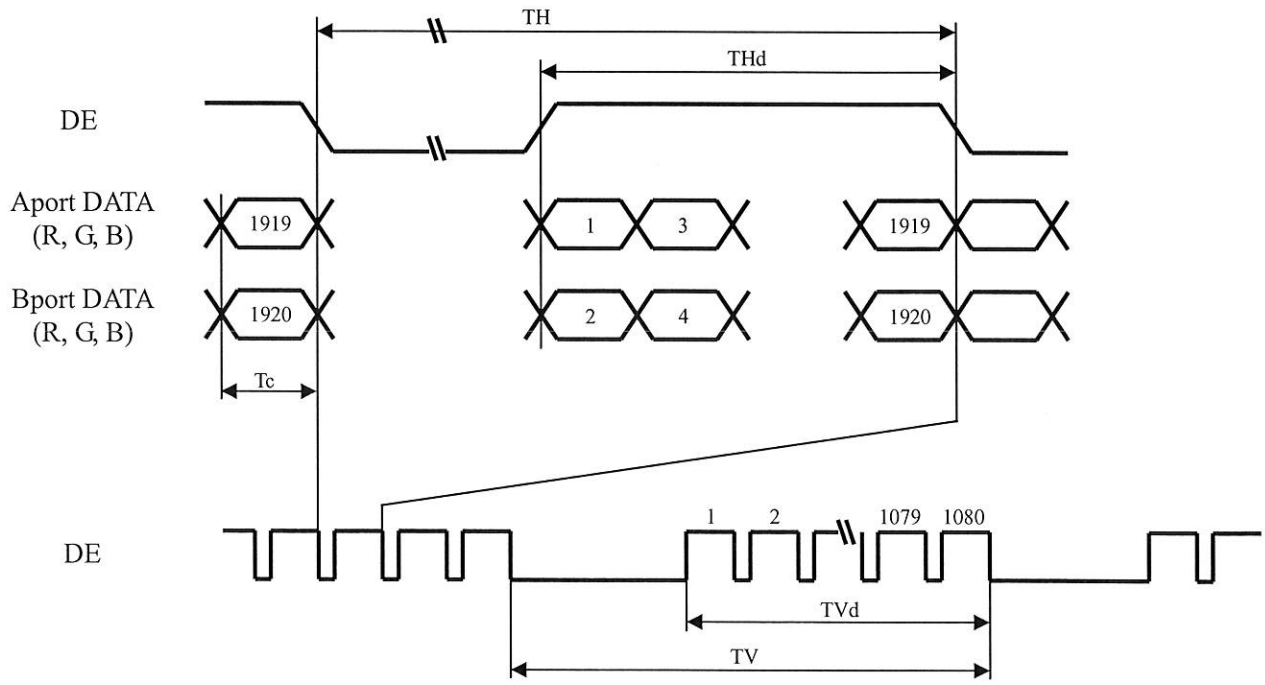
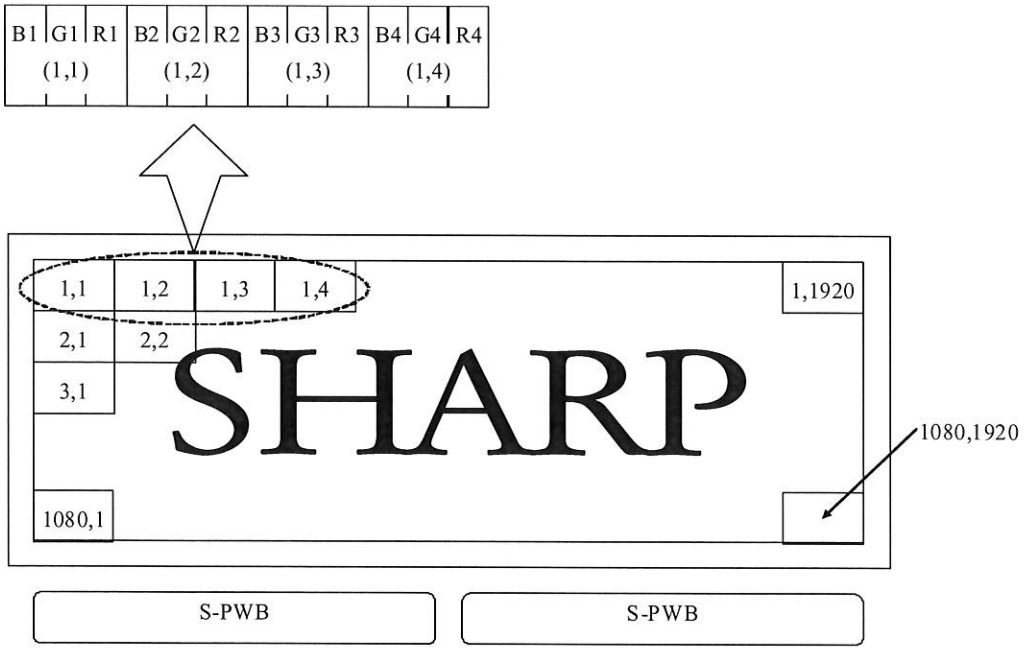


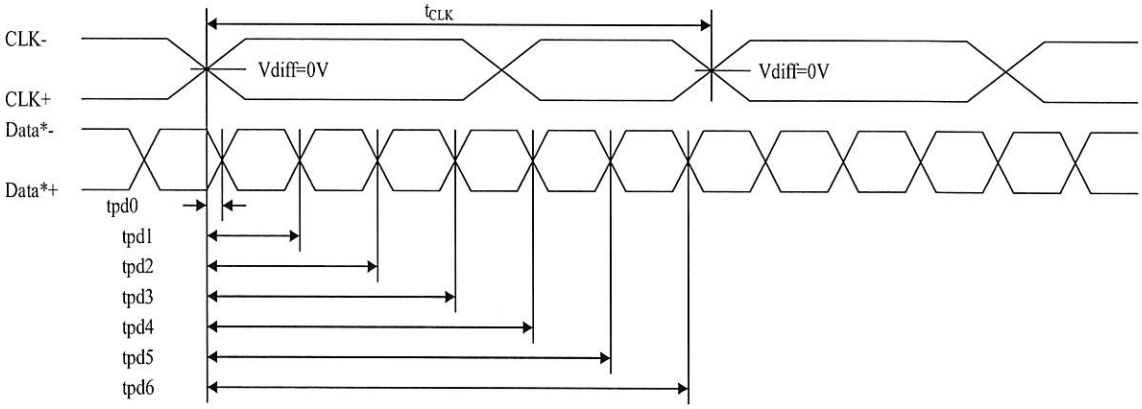
Fig3. Timing characteristics of input signal.

4.6. Input data signal and display position on the screen



[Note] Scan direction is setting for using S-PWBs' side down.

4.7. LVDS signal characteristics



Item		Symbol	Min.	Typ.	Max.	Unit
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	-0.25	0	0.25	ns
	Delay time, CLK rising edge to serial bit position 1	tpd1	$1*t_{CLK}/7-0.25$	$1*t_{CLK}/7$	$1*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 2	tpd2	$2*t_{CLK}/7-0.25$	$2*t_{CLK}/7$	$2*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 3	tpd3	$3*t_{CLK}/7-0.25$	$3*t_{CLK}/7$	$3*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 4	tpd4	$4*t_{CLK}/7-0.25$	$4*t_{CLK}/7$	$4*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 5	tpd5	$5*t_{CLK}/7-0.25$	$5*t_{CLK}/7$	$5*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 6	tpd6	$6*t_{CLK}7-0.25$	$6*t_{CLK}/7$	$6*t_{CLK}/7+0.25$	

4.8. Input signal, basic display colors and gray scale of each color

	Colors & Gray scale	Gray Scale	Data signal																													
			R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓						↓										↓										↓				
	⇩	↓						↓										↓										↓				
	Brighter	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓						↓										↓										↓				
	⇩	↓						↓										↓										↓				
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	GS1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	⇩	↓						↓										↓										↓				
	⇩	↓						↓										↓										↓				
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

- 0: Low level voltage / 1: High level voltage
- Each basic color can be displayed in 1024 gray scales from 10 bits data signals. According to the combination of total 30 bits data signals, one billion-color display can be achieved on the screen.

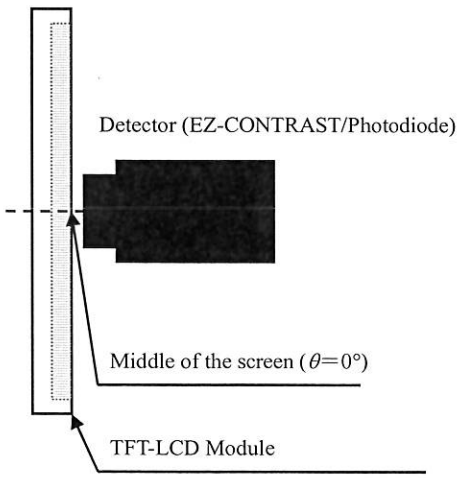
5. Optical characteristics

Ta=25°C, Vcc=12.0V, Frame rate:60Hz (typical)

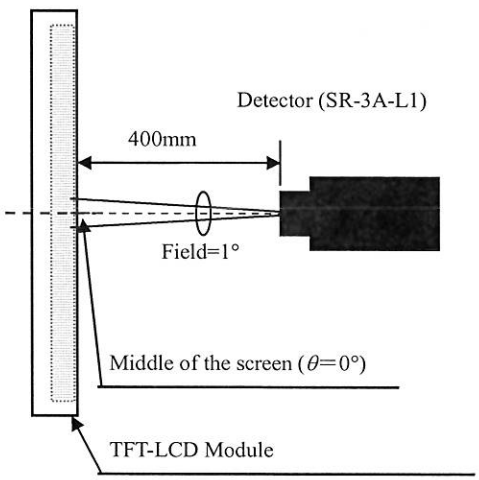
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21 θ22	CR≧10	70	88	-	Deg.	[Note1,4]
	Vertical	θ11 θ12		70	88	-	Deg.	
Contrast ratio		CRn	θ=0 deg.	4000	5000	-		[Note2,4]
Response time		τ_{DRV}			6		ms	[Note3,4,5]
Chromaticity	White	x		Typ.-0.03	(0.281)	Typ.+0.03	-	[Note4]
		y		Typ.-0.03	(0.285)	Typ.+0.03	-	
	Red	x		Typ.-0.03	(0.640)	Typ.+0.03	-	
		y		Typ.-0.03	(0.354)	Typ.+0.03	-	
	Green	x		Typ.-0.03	(0.324)	Typ.+0.03	-	
		y		Typ.-0.03	(0.624)	Typ.+0.03	-	
	Blue	x		Typ.-0.03	(0.152)	Typ.+0.03	-	
		y		Typ.-0.03	(0.056)	Typ.+0.03	-	
Luminance uniformity	White	δw				1.25		[Note 6]

- Optical characteristics are based on SHARP standard module's backlight system.
- The measurement shall be executed 60 minutes after lighting at rating.

[Note] The optical characteristics are measured using the following equipment.

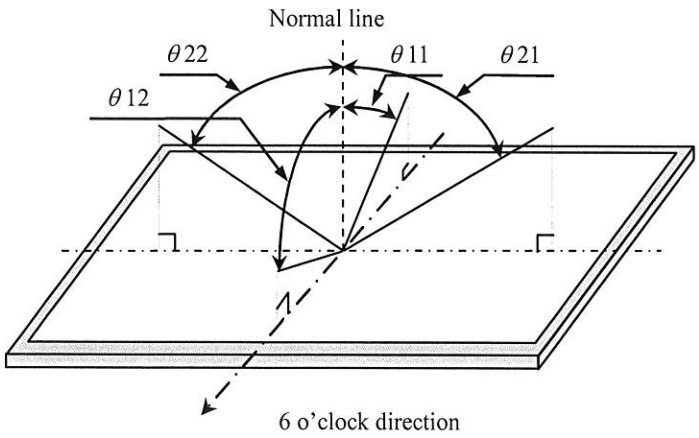


Measurement of viewing angle range and Response time.
-Viewing angle range: EZ-CONTRAST
- Response time: Photodiode



Measurement of Contrast, Luminance, Chromaticity.

[Note1] Definitions of viewing angle range:



[Note2] Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

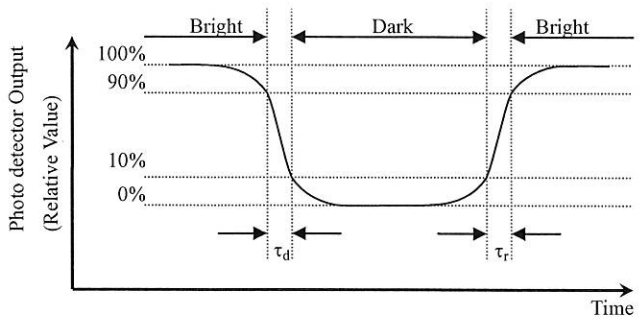
[Note3] Definition of response time

The response time (τ) is defined as the following figure and shall be measured by switching the input signal for "any level of gray (0%, 25%, 50%, 75% and 100%)" and "any level of gray (0%, 25%, 50%, 75% and 100%)".

	0%	25%	50%	75%	100%
0%		tr: 0%-25%	tr: 0%-50%	tr: 0%-75%	tr: 0%-100%
25%	td: 25%-0%		tr: 25%-50%	tr: 25%-75%	tr: 25%-100%
50%	td: 50%-0%	td: 50%-25%		tr: 50%-75%	tr: 50%-100%
75%	td: 75%-0%	td: 75%-25%	td: 75%-50%		tr: 75%-100%
100%	td: 100%-0%	td: 100%-25%	td: 100%-50%	td:100%-75%	

t*:x-y --- response time from level of gray(x) to level of gray(y)

$\tau_r = \Sigma(tr:x\text{-}y)/10$, $\tau_d = \Sigma(td:x\text{-}y)/10$

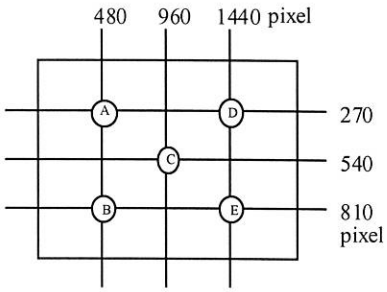


[Note4] This value shall be measured at center of the screen.

[Note5] This value is valid when O/S driving is used at typical input time value.

[Note6] This value is calculated as the following with nine measurements. (A~E)

$$\delta W = \frac{\text{Maximum luminance of five points (brightness)}}{\text{Minimum luminance of five points (brightness)}}$$



6. Packing for shipping

6.1. Packing form

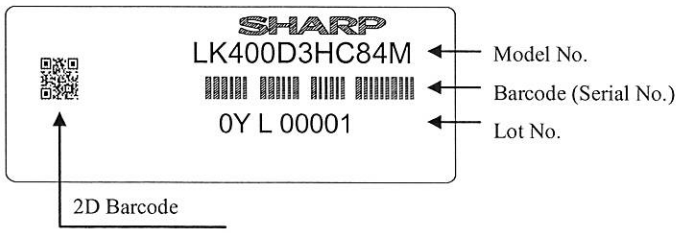
a) Open Cell quantity in 1 cell box : 15 cells
b) Piling number of cell box : 14 Maximum
c) 1 palette size : 1390(W) x 1150(D) x 1059(H) [mm]
d) Total mass of 1 palette filled with full open cells : 490.5 kg Maximum

6.2. Label

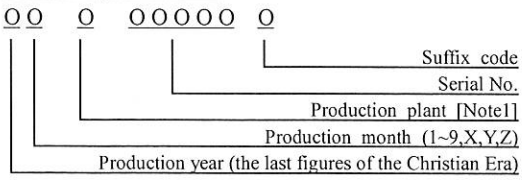
a) Open Cell Label

This label is stuck on the protection film of front polarizer.

ex) LK400D3HAxx-2 [Japan production]



How to express Lot No.



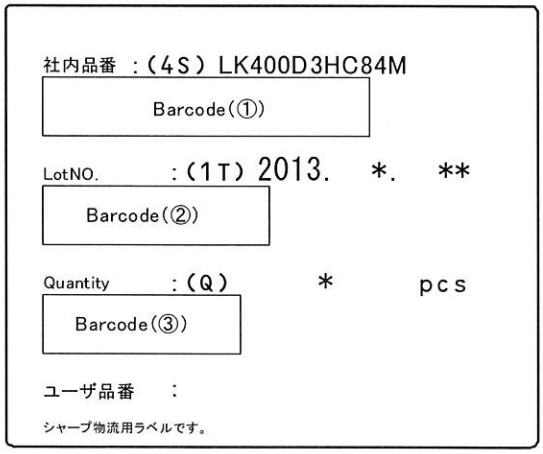
[Note1] Production plant code

Code	Plant	Model No. & Suffix Code
L	Japan	LK400D3HC84M [tentative]
(TBD)	(EMS)	LK400D3HC84M [tentative]

b) Packing label

This label is stuck on the cell box and palette.

ex) LK400D3HC84M



① Model No.& Suffix Code
② Lot No.
③ Quantity

7. Reliability test item

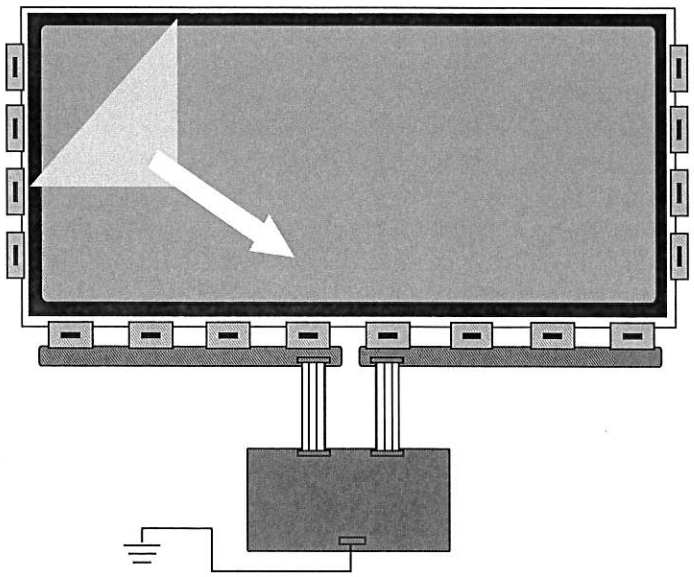
No.	Test item	Condition
1	High temperature storage test (Open Cell)	Ta = 60°C 240h
2	Low temperature storage test (Open Cell)	Ta = -25°C 240h
3	High temperature and high humidity operation test (Open Cell)	Ta = 40°C 95%RH 240h (No condensation)
4	High temperature operation test (Open Cell)	Ta = 50°C 240h
5	Low temperature operation test (Open Cell)	Ta = 0°C 240h
6	Vibration test (Cell Box with full Open Cells)	X and Y direction: 15min, Z direction: 60min. 5Hz to 50Hz acceleration velocity: 1.0G Sweeping ratio: 3min
7	Drop test (Cell Box with full Open Cells)	Height: 25cm (corner and edge), 32cm (surface) Number: 8times (corner 1time and edge 3times and surface 4times)

[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

8. Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable.
b) Be sure to design the module and cabinet so that the Open Cell can be installed without any extra stress such as warp or twist.
c) Since the polarizer is easily damaged, pay attention not to scratch it.
d) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
e) When the polarizer is soiled, wipe it with absorbent cotton or other soft cloth.
f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
g) Precautions of peeling off the protection film.



- Be sure to peel off slowly (recommended more than 7sec) and constant speed.
- Peeling direction shows Fig.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to ground S-PWB while peeling of the protection film.
- Ionized air should be blown over during peeling action.
- The protection film must not touch drivers and S-PWBs.
- If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

h) Since the Open Cell consists of TFT and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharges, persons who are handling the Open Cell should be grounded through adequate methods such as the anti-static wrist band. Connector pins should not be touched directly with bare hands.

- Reference : Process control standard of sharp

	Item	Management standard value and performance standard
1	Anti-static mat (shelf)	1 to 50 [M ohm]
2	Anti-static mat (floor, desk)	1 to 100 [M ohm]
3	Ionizer	Attenuate from ±1000V to ±100V within 2 sec
4	Anti-static wrist band	0.8 to 10 [M ohm]
5	Anti-static wrist band entry and ground resistance	Below 1000 [ohm]
6	Temperature	22 to 26 [°C]
7	Humidity	60 to 70 [%RH]

i) The Open Cell has some PWBs, take care to keep them from any stress or pressure when handling or installing the Open Cell, otherwise some of electronic parts on the PWBs may be damaged.

j) When handling the Open Cell and assembling them into module and cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open Cell.

k) Applying too much force and stress to PWB and driver (COF) may cause a malfunction electrically and mechanically.

l) The Open Cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufacturers.

m) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

n) Please design the heat dissipation of the module with enough care for C-PWB, Source-driver and Gate-driver's IC

o) This Open Cell may have some black stains.

p) The chemical compound, which causes the destruction of ozone layer, is not used.

q) This Open Cell is corresponded to RoHS. "R.C." label on the side of palette shows it.

r) When any question or issue occurs, it shall be solved by mutual discussion.

9. Carton storage condition

Temperature	0°C to 40°C
Humidity	95% RH or less
Reference condition	20°C to 35°C, 85% RH or less (summer) 5°C to 15°C, 85% RH or less (winter) the total storage time (40°C, 95% RH) : 240h or less
Sunlight	Be sure to shelter a production from the direct sunlight.
Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Notes	Be sure to put cartons on palette or base, don't put it on floor, and store them with removing from wall. Please take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
Storage life	1 year.

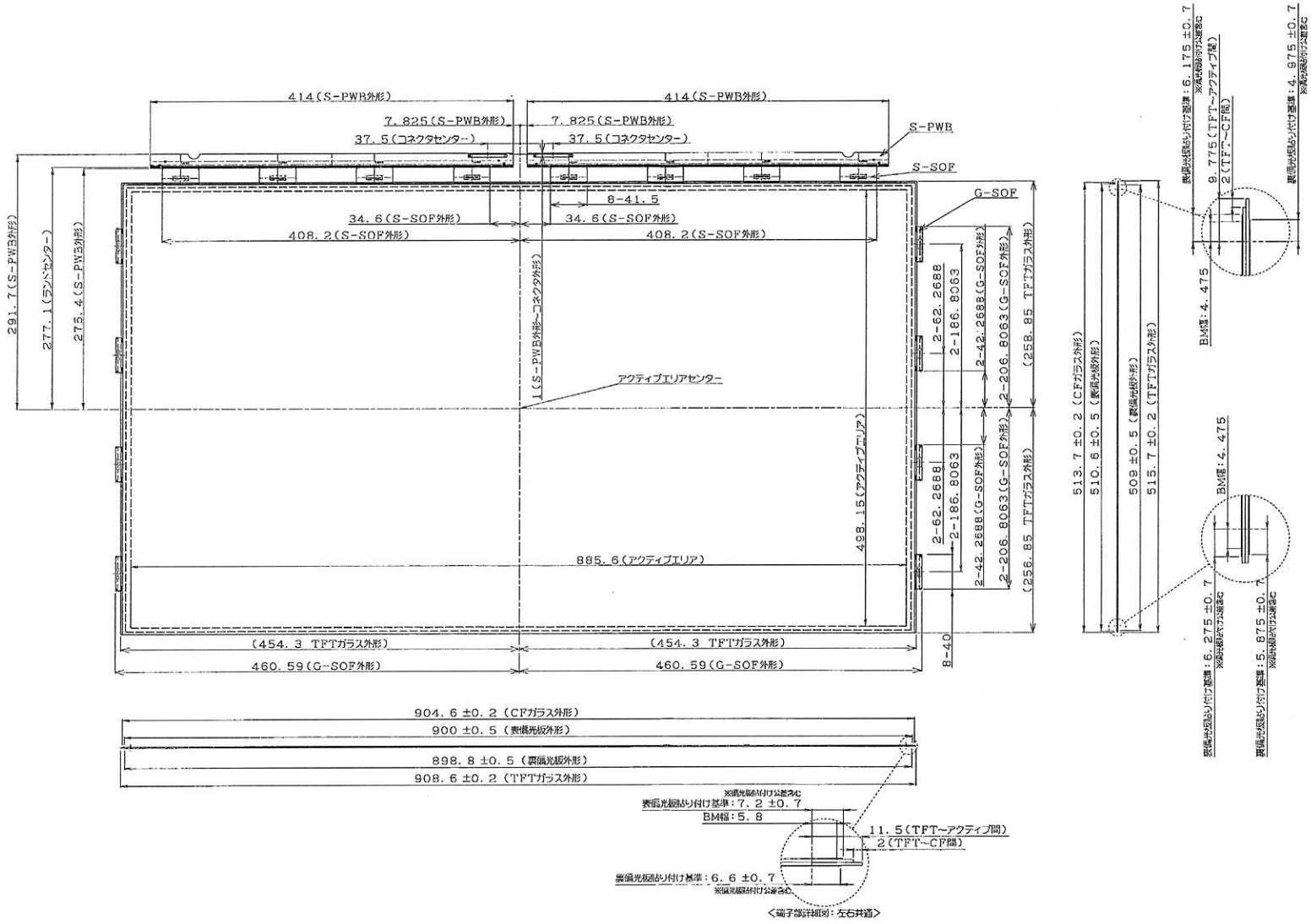


Fig.4 LK400D3HC84M