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	AVC LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION **SPECIFICATION**	MODULE DEVELOPMENT CENTER AVC LIQUID CRYSTAL DISPLAY GROUP

DEVICE SPECIFICATION FOR

TFT-LCD module

Model No. LK520D3LA63

CUSTOMER'S APPROVAL

DATE _____

PRESENTED

BY _____ BY _____

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AVC LIQUID CRYSTAL DISPLAY GROUP
SHARP CORPORATION

RECORDS OF REVISION

MODEL No. : LK520D3LA63

SPEC No. : LD-K20Z07B

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-K20Z07	2008/12/8	-	-	-	1st ISSUE
	2009/9/4	A	P12	- Correction of error in spec.	▲A-1
			P19, 22	- Addition of precaution about fix point.	
			P21	- Addition of records about design change.	▲A-2
			P10, 19,20, 21, 25	- Addition of new model ''LA63P''.	▲A-3
	2009/10/28	B	P20	- Addition of description about user barcode label.	▲B
			P21	- Addition of model list.	
			P10,19,20,21,26	- Addition of limited time model ''LA63P●''.	

1. Application

This specification applies to the color 52.0" TFT-LCD module LK520D3LA63.

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2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, control circuit, power supply circuit, inverter circuit and back light system etc. Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with one billion colors by using 8bit+FRC LVDS (Low Voltage Differential Signaling) to interface, +12V of DC supply voltages.

This module also includes the DC/AC inverter to drive the CCFT. (+24V of DC supply voltage)

And in order to improve the response time of LCD, this module applies the Over Shoot driving (O/S driving) technology for the control circuit. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With this technology, image signals can be set so that liquid crystal response completes within one frame. As a result, motion blur reduces and clearer display performance can be realized.

This LCD module also adopts Double Frame Rate driving method.

With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.

3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	132.174 (Diagonal)	cm
	52.0 (Diagonal)	inch
Active area	1152.0(H) x 648.0 (V)	mm
Pixel Format	1920(H) x 1080(V) (1pixel = R + G + B dot)	pixel
Pixel pitch	0.600(H) x 0.600 (V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Unit Outline Dimensions (*1)	1219.0(W) x 706.7(H) x 59.3(D)	mm
Mass	15.0 ±1.0	kg
Surface treatment	Anti glare, Hard coating: 2H and more Haze value: 8% (typ.)	

(*1) Outline dimensions are shown in Fig.1 (excluding protruding portion)

4. Input Terminals

4.1. TFT panel driving

CN1 (Interface signals and +12V DC power supply) (Shown in Fig.1)

Using connector : FI-RE51S-HF (Japan Aviation Electronics Ind., Ltd.)

Mating connector : FI-RE51HL, FI-RE51CL (Japan Aviation Electronics Ind., Ltd.)

Mating LVDS transmitter : THC63LVD1023 or equivalent device

Pin No.	Symbol	Function	Remark
1	GND		
2	Reserved	It is required to set non-connection (OPEN)	Pull up 3.3V
3	Reserved	It is required to set non-connection (OPEN)	Pull up 3.3V
4	Reserved	It is required to set non-connection (OPEN)	Pull up 3.3V
5	FRAME	Frame frequency setting 1:60Hz 0:50Hz [Note 1]	Pull down (GND)
6	O/S set	O/S operation setting H:O/S ON, L:O/S OFF [Note 3]	Pull up 3.3V
7	SELLVDS	Select LVDS data order [Note 2]	Pull down (GND)
8	Reserved	It is required to set non-connection (OPEN)	Pull down (GND)
9	Reserved	It is required to set non-connection (OPEN)	Pull down (GND)
10	Reserved	It is required to set non-connection (OPEN)	Pull down (GND)
11	GND		
12	AIN0-	Aport (-)LVDS CH0 differential data input	
13	AIN0+	Aport (+)LVDS CH0 differential data input	
14	AIN1-	Aport (-)LVDS CH1 differential data input	
15	AIN1+	Aport (+)LVDS CH1 differential data input	
16	AIN2-	Aport (-)LVDS CH2 differential data input	
17	AIN2+	Aport (+)LVDS CH2 differential data input	
18	GND		
19	ACK-	Aport LVDS Clock signal(-)	
20	ACK+	Aport LVDS Clock signal(+)	
21	GND		
22	AIN3-	Aport (-)LVDS CH3 differential data input	
23	AIN3+	Aport (+)LVDS CH3 differential data input	
24	AIN4-	Aport (-)LVDS CH4 differential data input	
25	AIN4+	Aport (+)LVDS CH4 differential data input	
26	GND		
27	GND		
28	BIN0-	Bport (-)LVDS CH0 differential data input	
29	BIN0+	Bport (+)LVDS CH0 differential data input	
30	BIN1-	Bport (-)LVDS CH1 differential data input	
31	BIN1+	Bport (+)LVDS CH1 differential data input	
32	BIN2-	Bport (-)LVDS CH2 differential data input	
33	BIN2+	Bport (+)LVDS CH2 differential data input	
34	GND		
35	BCK-	Bport LVDS Clock signal(-)	
36	BCK+	Bport LVDS Clock signal(+)	
37	GND		
38	BIN3-	Bport (-)LVDS CH3 differential data input	
39	BIN3+	Bport (+)LVDS CH3 differential data input	
40	BIN4-	Bport (-)LVDS CH4 differential data input	
41	BIN4+	Bport (+)LVDS CH4 differential data input	
42	GND		
43	GND		
44	GND		
45	GND		
46	GND		

47	Reserved (VCC)	(+12V Power Supply)	
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

CN2 (Interface signals) (Shown in Fig1)

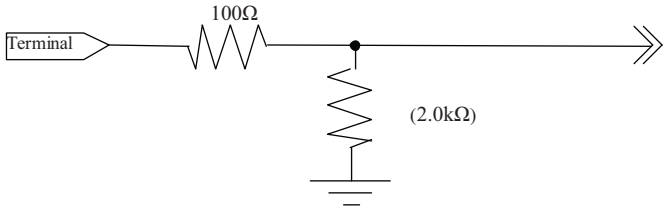
Using connector : FI-RE41S-HF (Japan Aviation Electronics Ind., Ltd.)

Mating connector : FI-RE41HL, FI-RE41CL (Japan Aviation Electronics Ind., Ltd.)

Pin No.	Symbol	Function	Remark
1	Reserved (VCC)	(+12V Power Supply)	
2	Reserved (VCC)	(+12V Power Supply)	
3	Reserved (VCC)	(+12V Power Supply)	
4	Reserved (VCC)	(+12V Power Supply)	
5	Reserved		
6	Reserved		
7	Reserved		
8	Reserved		
9	GND		
10	CIN0-	Cport (-)LVDS CH0 differential data input	
11	CIN0+	Cport (+)LVDS CH0 differential data input	
12	CIN1-	Cport (-)LVDS CH1 differential data input	
13	CIN1+	Cport (+)LVDS CH1 differential data input	
14	CIN2-	Cport (-)LVDS CH2 differential data input	
15	CIN2+	Cport (+)LVDS CH2 differential data input	
16	GND		
17	CCK-	Cport LVDS Clock signal(-)	
18	CCK+	Cport LVDS Clock signal(+)	
19	GND		
20	CIN3-	Cport (-)LVDS CH3 differential data input	
21	CIN3+	Cport (+)LVDS CH3 differential data input	
22	CIN4-	Cport (-)LVDS CH4 differential data input	
23	CIN4+	Cport (+)LVDS CH4 differential data input	
24	GND		
25	GND		
26	DIN0-	Dport (-)LVDS CH0 differential data input	
27	DIN0+	Dport (+)LVDS CH0 differential data input	
28	DIN1-	Dport (-)LVDS CH1 differential data input	
29	DIN1+	Dport (+)LVDS CH1 differential data input	
30	DIN2-	Dport (-)LVDS CH2 differential data input	
31	DIN2+	Dport (+)LVDS CH2 differential data input	
32	GND		
33	DCK-	Dport LVDS Clock signal(-)	
34	DCK+	Dport LVDS Clock signal(+)	
35	GND		
36	DIN3-	Dport (-)LVDS CH3 differential data input	
37	DIN3+	Dport (+)LVDS CH3 differential data input	
38	DIN4-	Dport (-)LVDS CH4 differential data input	
39	DIN4+	Dport (+)LVDS CH4 differential data input	
40	GND		
41	GND		

[Note] GND of a liquid crystal panel drive part has connected with a module chassis.

[Note 1]The equivalent circuit figure of the terminal

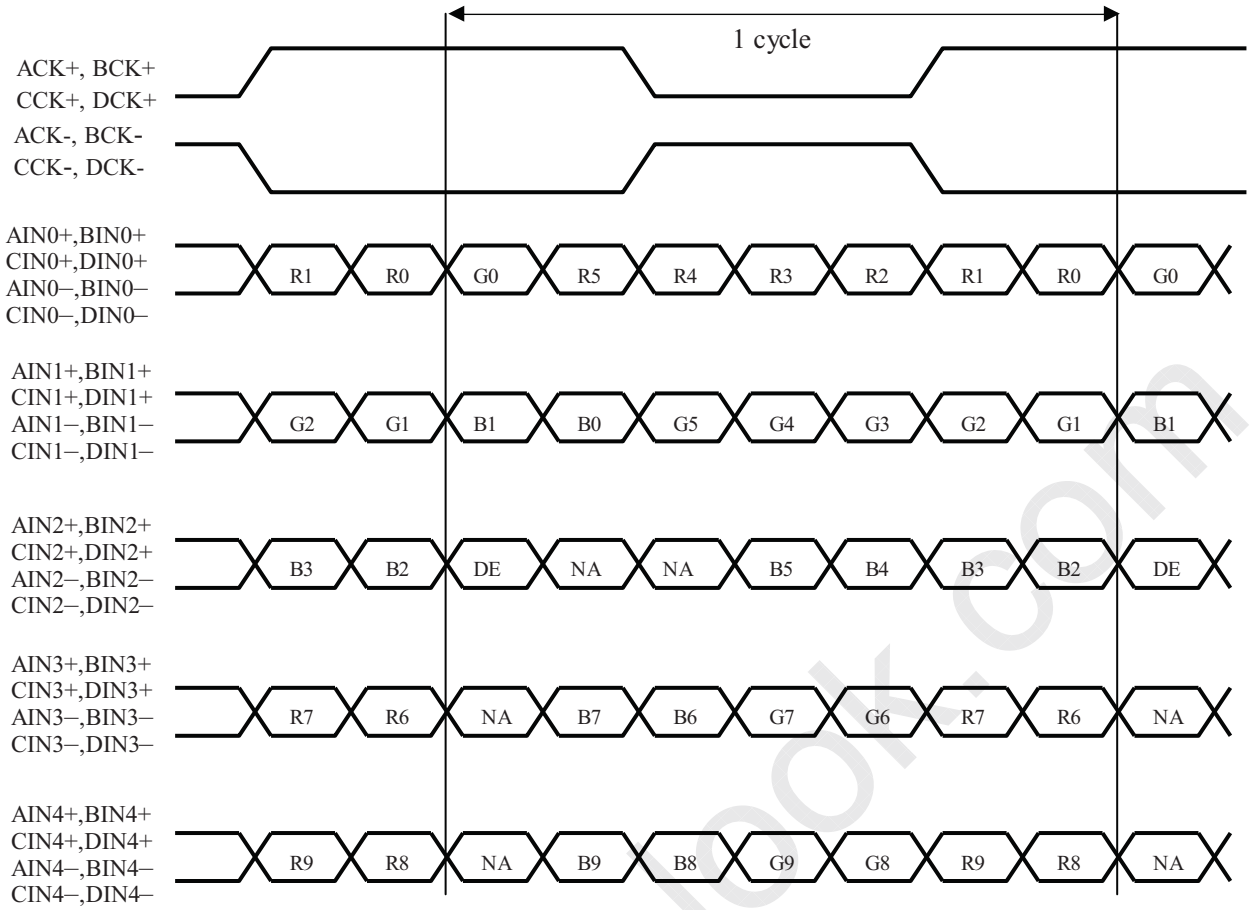


[Note 2] LVDS Data order

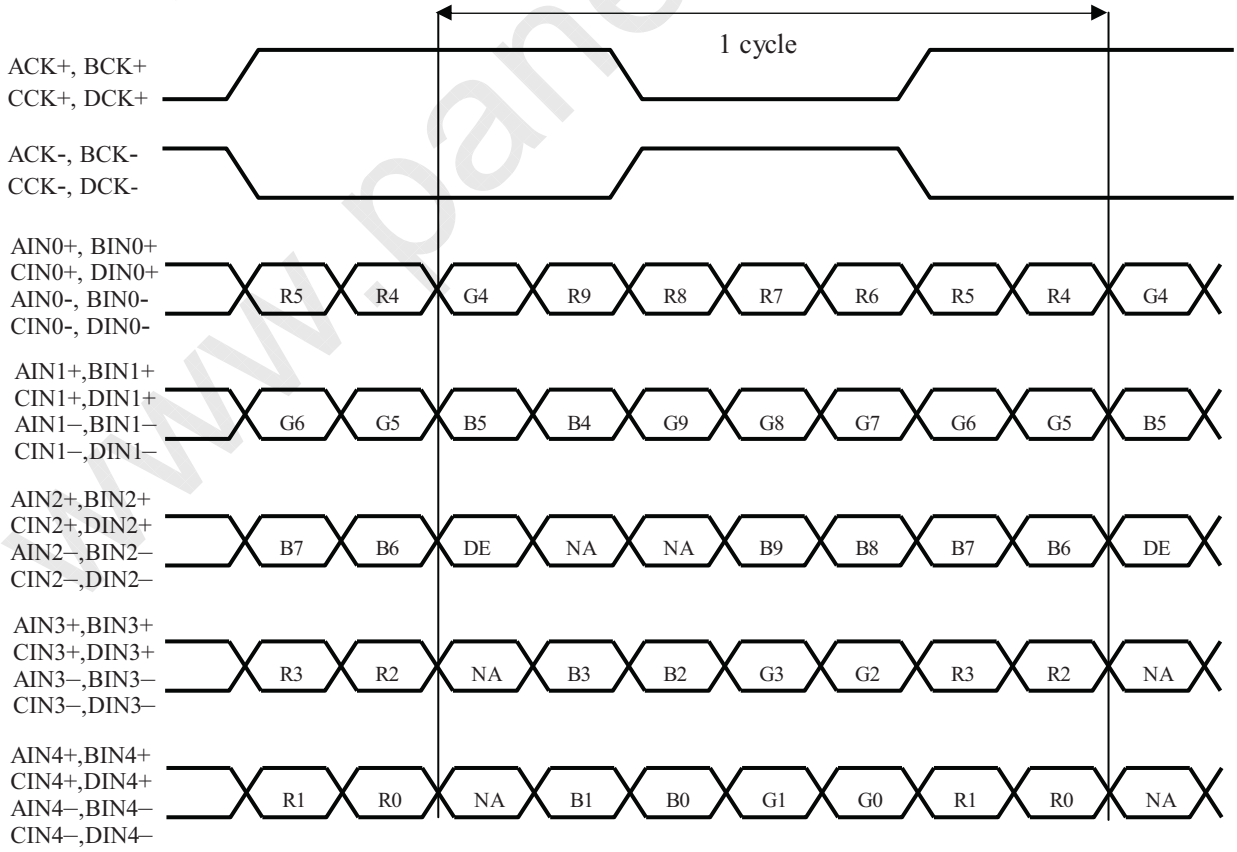
SELLVDS		
Data	L(GND) or Open [VESA]	H(3.3V) [JEIDA]
TA0	R0(LSB)	R4
TA1	R1	R5
TA2	R2	R6
TA3	R3	R7
TA4	R4	R8
TA5	R5	R9(MSB)
TA6	G0(LSB)	G4
TB0	G1	G5
TB1	G2	G6
TB2	G3	G7
TB3	G4	G8
TB4	G5	G9(MSB)
TB5	B0(LSB)	B4
TB6	B1	B5
TC0	B2	B6
TC1	B3	B7
TC2	B4	B8
TC3	B5	B9(MSB)
TC4	NA	NA
TC5	NA	NA
TC6	DE(*)	DE(*)
TD0	R6	R2
TD1	R7	R3
TD2	G6	G2
TD3	G7	G3
TD4	B6	B2
TD5	B7	B3
TD6	N/A	N/A
TE0	R8	R0(LSB)
TE1	R9(MSB)	R1
TE2	G8	G0(LSB)
TE3	G9(MSB)	G1
TE4	B8	B0(LSB)
TE5	B9(MSB)	B1
TE6	N/A	N/A

NA: Not Available
(*)Since the display position is prescribed by the rise of DE (Display Enable) signal, please do not fix DE signal during operation at ”High”.

SELLVDS= Low (GND) or OPEN

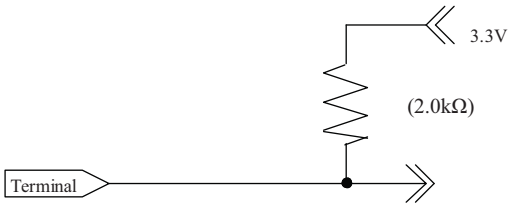


SELLVDS= High (3.3V)

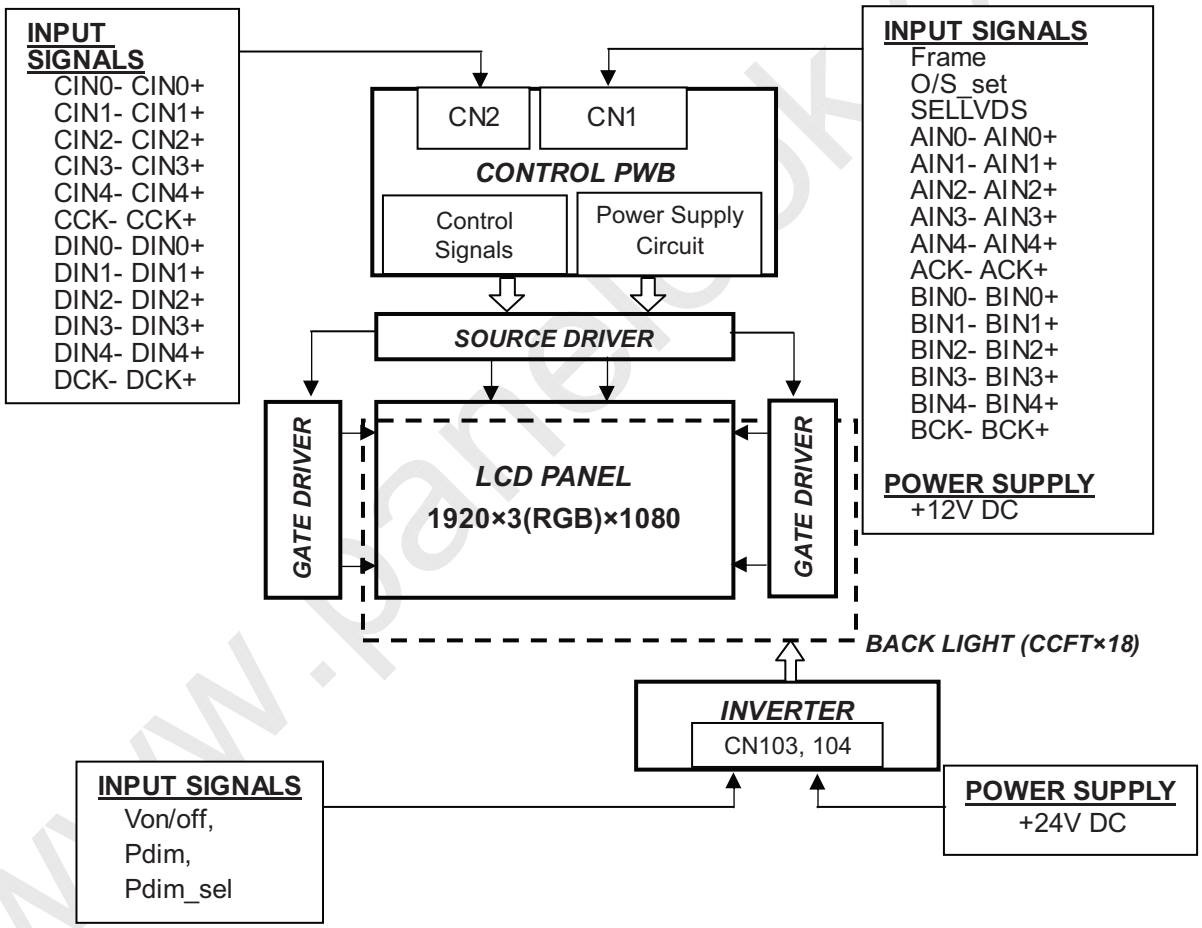


DE: Display Enable, NA: Not Available (Fixed Low)

[Note 3] The equivalent circuit figure of the terminal



4.2. Interface block diagram



4.3. Backlight driving

CN103 (+24V DC power supply and inverter control)

Using connector : S14B-PHA-SM (LF) (JST)

Mating connector : PHR-14 (JST)

Pin No.	Symbol	Function	Default(OPEN)	Input Impedance	Remark
1	VINV	+24V	-		
2	VINV	+24V	-		
3	VINV	+24V	-		
4	VINV	+24V	-		
5	VINV	+24V	-		
6	GND		-		
7	GND		-		
8	GND		-		
9	GND		-		
10	GND		-		
11	Reserved	For LCD module internal usage, should be open			
12	Von/off	Inverter ON/OFF	3.3V : pull up Inverter ON	75kohm	[Note 1]
13	Pdim	Brightness Control	3.3V : pull up Brightness 100%	1.02Mohm	[Note 2]
14	Pdim_sel	PWM selection	3.3V : pull up Selected Analog PWM	67kohm	[Note 3]

CN104 (+24V DC power supply)

Using connector : S12B-PHA-SM (LF) (JST)

Mating connector : PHR-12 (JST)

Pin No.	Symbol	Function	Default(OPEN)	Input Impedance	Remark
1	VINV	+24V	-		
2	VINV	+24V	-		
3	VINV	+24V	-		
4	VINV	+24V	-		
5	VINV	+24V	-		
6	GND		-		
7	GND		-		
8	GND		-		
9	GND		-		
10	GND		-		
11	Reserved	For LCD module internal usage, should be open			
12	Reserved	For LCD module internal usage, should be open			

[Note 1] Inverter ON/OFF

Input voltage	Function
0V	Inverter : OFF
3.3V	Inverter : ON

[Note 2] Brightness Control selection

Pin No.14 is used for the selection of dimming control for Pdim pin (Pin No.13).

Input voltage	Pdim
0V	Pulse dimming
3.3V	Analog dimming

[Note 3] Brightness Control

1. Analog Dimming

Brightness control is regulated by analog input voltage (0V to 3.3V).

Ta=25°C

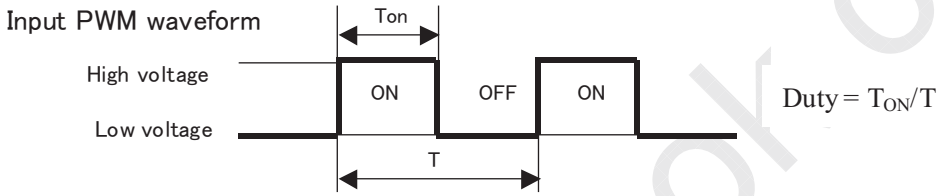
	MIN	TYP	MAX	Function
Input voltage [Pdim]	0V	<->	3.3V	0V: Dark - 3.3V: Bright
[Reference] Brightness ratio[%]	10	<->	100	

[Note] PWM frequency : 110±10Hz

[Note] There is a case that lamp mura may happen, depending on ambient temperature and dimming. Dimming level should be set according to your evaluation of actual display performance. (Minimum input voltage 1.5V at below 15°C)

2. Pulse Dimming

Pin No.13 is used for the control of the PWM duty with input pulse from 95Hz to 350Hz.



		MIN	TYP	MAX	Remark
Pulse signal	[Hz]	95	110	350	
DUTY(T_{ON}/T)	[%]	20	<->	100	Ta=25°C
Dimming level (luminance ratio)	[%]	10	<->	100	Ta=25°C Pulse signal=110Hz

[Note] There is a case that lamp mura may happen, depending on ambient temperature, in dimming. Minimum dimming level should be set according to your evaluation of actual display performance. (Minimum duty 60% at below 15°C)

[Note] In case of using Pulse Dimming, be careful so that the Pdim signal (Pin 13) doesn't have glitch.

4.4. The back light system characteristics

The back light system is direct type with 18 CCFTs (Cold Cathode Fluorescent Tube).

The characteristics of the lamp are shown in the following table. The value mentioned below is at the case of one CCFT.

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Life time	T_L	-	60000	-	Hour	[Note]

[Note]

- Lamp life time is defined as the time when brightness becomes 50% of the original value in the continuous operation under the condition of Ta=25°C.
- Above value is applicable when the long side of LCD module is placed horizontally (Landscape position). (Lamp lifetime may vary if LCD module is in portrait position due to the change of mercury density inside the lamp.)

5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage (for Control)	V_I	Ta=25°C	-0.3 ~ 3.6	V	[Note 1]
12V supply voltage (for Control)	V_{CC}	Ta=25°C	0 ~ +14	V	
Input voltage (for Inverter)	V_{ON} Pdim	Ta=25°C	0 ~ +6	V	
24V supply voltage (for Inverter)	V_{INV}	Ta=25°C	0 ~ +29	V	
Storage temperature	Tstg	-	-25 ~ +60	°C	[Note 2]
Operation temperature (Ambient)	Topa	-	0 ~ +50	°C	

[Note 1] SELLVDS, FRAME, O/S_set

[Note 2] Humidity 95%RH Max. (Ta≦40°C)

Maximum wet-bulb temperature at 39°C or less.(Ta>40°C)

No condensation.

6. Electrical Characteristics

6.1. Control circuit driving Ta=25°C

Parameter		Symbol	Min.	Typ.	Max.	Uniit	Remark
+12V supply voltage	Supply voltage	Vcc	11.4	12	12.6	V	[Note 1]
	Current dissipation	Icc	-	1.0	2.5	A	[Note 2]
	Inrush current	$I_{RUSH}1$	-	5.0	-	A	t1=500us [Note 7]
		$I_{RUSH}2$	-	1.7	-	A	t1>5ms [Note 7]
Permissible input ripple voltage		V_{RP}	-	-	100	mV_{P-P}	Vcc = +12.0V
Input Low voltage		V_{IL}	0	-	1.0	V	[Note 3]
Input High voltage		V_{IH}	2.3	-	3.3	V	
Input leak current (Low)		I_{IL1}	-	-	400	µA	V_I = 0V [Note 4]
		I_{IL2}	-	-	40	µA	V_I = 0V [Note 5]
Input leak current (High)		I_{IH1}	-	-	40	µA	V_I = 3.3V [Note 4]
		I_{IH2}	-	-	400	µA	V_I = 3.3V [Note 5]
Terminal resistor		R_T	-	100	-	Ω	Differential input
Input Differential voltage		|VID|	200	400	600	mV	[Note 6]
Differential input common mode voltage		VCM	|VID|/2	1.2	2.4-|VID|/2	V	[Note 6]

[Note] V_{CM}: Common mode voltage of LVDS driver.

[Note 1]

Input voltage sequences

0 < t1 ≦ 20ms

10 < t2 ≦ 50ms

10 < t3 ≦ 50ms

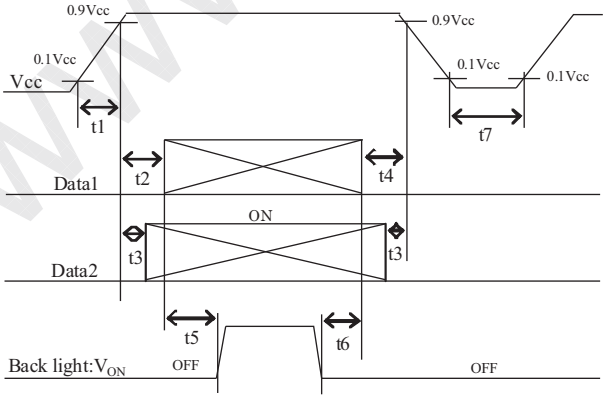
0 < t4 ≦ 1s

t5 ≧ 950ms [LA63X/LA63P●] ▲B

t5 ≧ 300ms [LA63P] ▲A-3

t6 ≧ 0ms

t7 ≧ 300ms



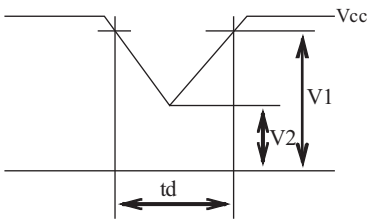
Dip conditions for supply voltage

a) 6.5V ≦ Vcc < 10.8V

td ≦ 10ms

b) Vcc < 6.5V

Dip conditions for supply voltage is based on input voltage sequence.



V1:10.8V
V2:6.5V

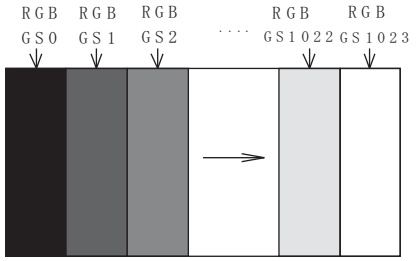
※ Data1: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4± CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±, DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±

*V_{CM} voltage pursues the sequence mentioned above

※ Data2: SELLVDS, FRAME, O/S_SET

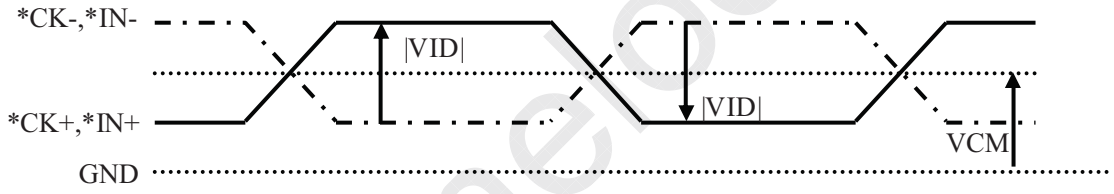
[Note] About the relation between data input and back light lighting, please base on the above-mentioned input sequence. When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

[Note 2] Typical current situation: 1024 gray-bar patterns. (Vcc = +12.0V)
The explanation of RGB gray scale is seen in section 8.

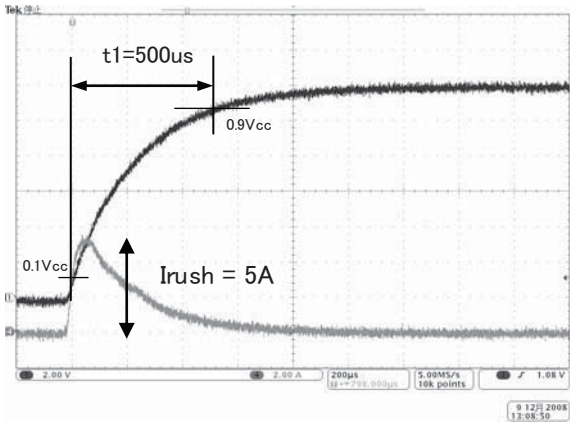


Vcc = +12.0V
CK = 74.25MHz
Th = 7.41μs

[Note 3] SELLVDS, FRAME, O/S_SET
[Note 4] O/S_SET
[Note 5] FRAME, SELLVDS
[Note 6] ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±
CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±, DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±



[Note 7] Vcc12V inrush current waveform



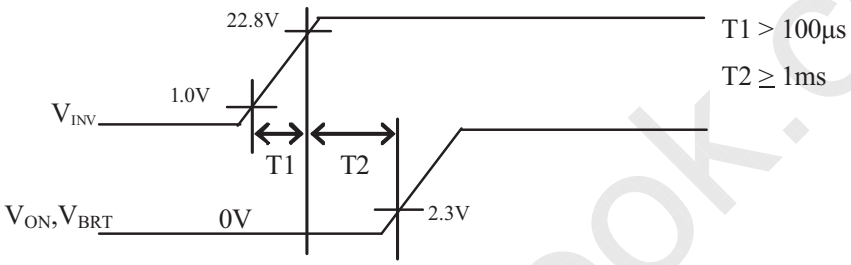
Input voltage conditions
Vcc= +12V

6.2. Inverter driving for back light

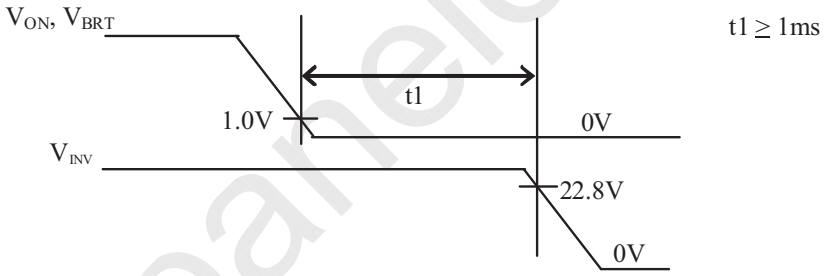
The back light system is direct type with 18 CCFTs (Cold Cathode Fluorescent Tube).

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+24V	Current dissipation 1 ▲A-1	I_{INV1}	-	9.9	11.4	A	V_{INV} = 24V, Ta=25°C Pdim = 3.3V [Note 1,2]
	Current dissipation 2 ▲A-1	I_{INV2}	-	8.3	9.5	A	
	Inrush current ▲A-1	I_{RUSH}	-	-	10.9	A	
	Supply voltage	V_{INV}	22.8	24.0	25.2	V	
Permissible input ripple voltage		V_{RF}	-	-	1.1	V_{p-p}	V_{INV} = +24.0V
Input voltage (Low)		V_{ONL}	0	-	1.0	V	$V_{ON/OFF}$, Pdim, Pdim_sel
Input voltage (High)		V_{ONH}	2.3	-	3.6	V	

[Note 1] 1) V_{INV}-turn-on condition



2) V_{INV}-turn-off condition



[Note 2] Current dissipation 1 : Definition within 60 minutes after turn on. (Rush current is excluded.)

Current dissipation 2 : Definition more than 60minutes after turn on.

7. Timing characteristics of input signals

7.1. Timing characteristics

Timing diagrams of input signal are shown in Fig.2.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Clock	Frequency	1/Tc	55	74.25	80	MHz	
Data enable signal	Horizontal period	TH	515	550	825	clock	
			6.94	7.41	11.1	μs	
	Horizontal period (High)	THd	480	480	480	clock	
	Vertical period	TV	1120	1125	1400	line	
			73.052	120	120.54	Hz	
	Vertical period (High)	TVd	1080	1080	1080	line	

[Note]-When vertical period is very long, flicker and etc. may occur.

-Please turn off the module after it shows the black screen.

-Please make sure that length of vertical period should become of an integral multiple of horizontal length of period. Otherwise, the screen may not display properly.

-As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.

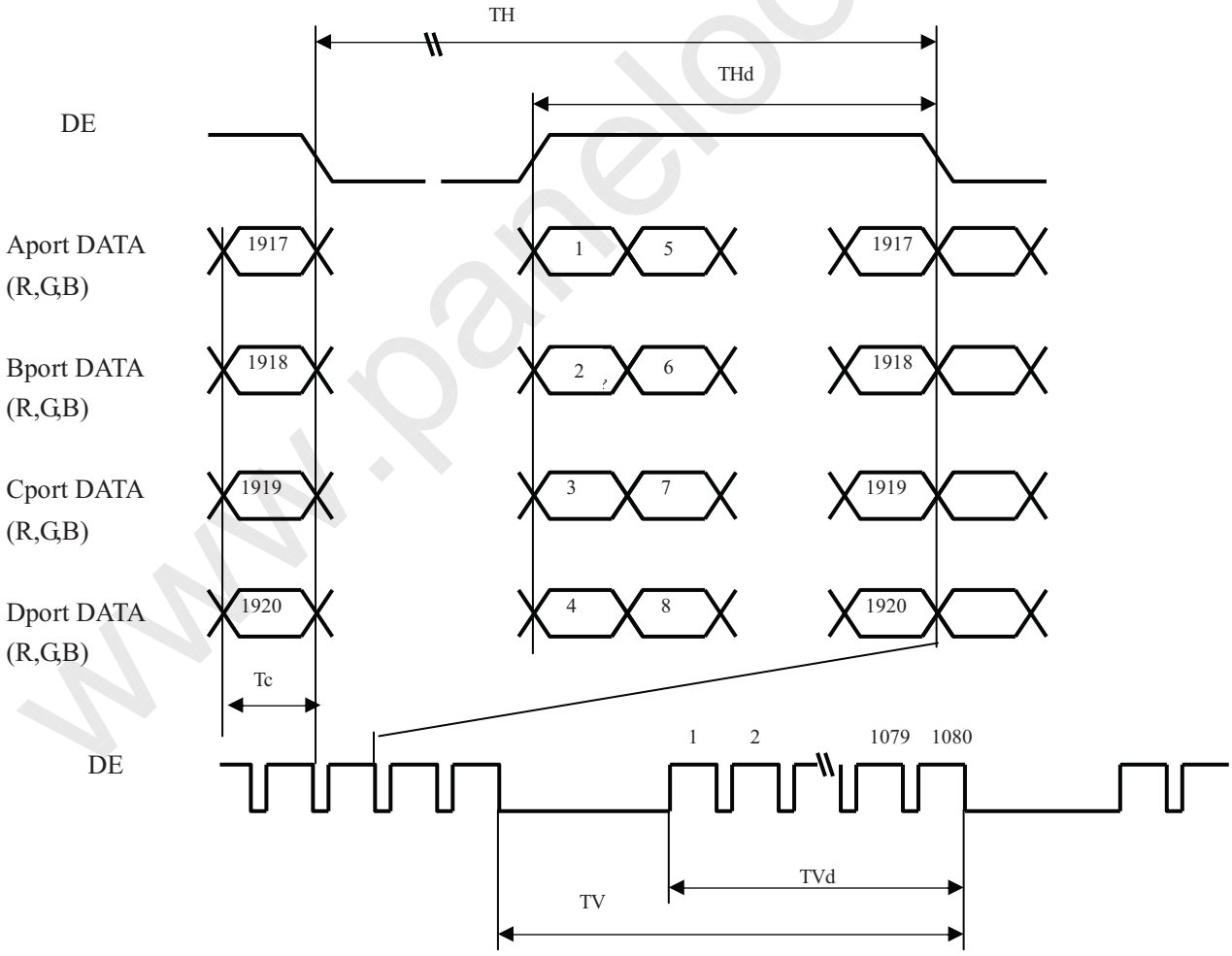
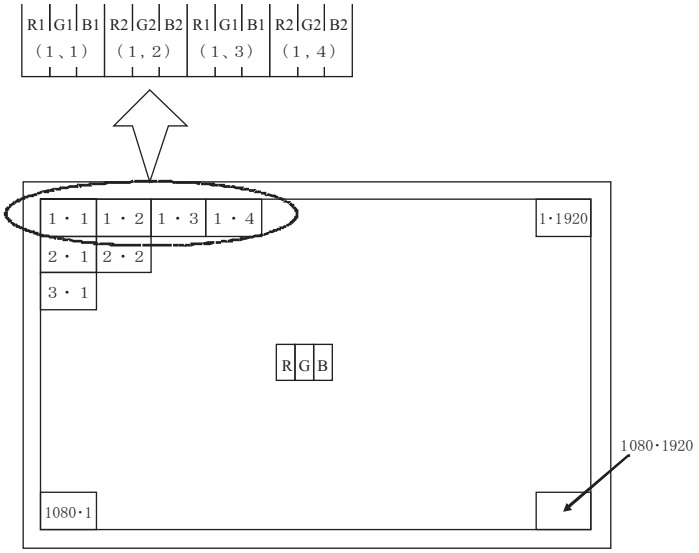


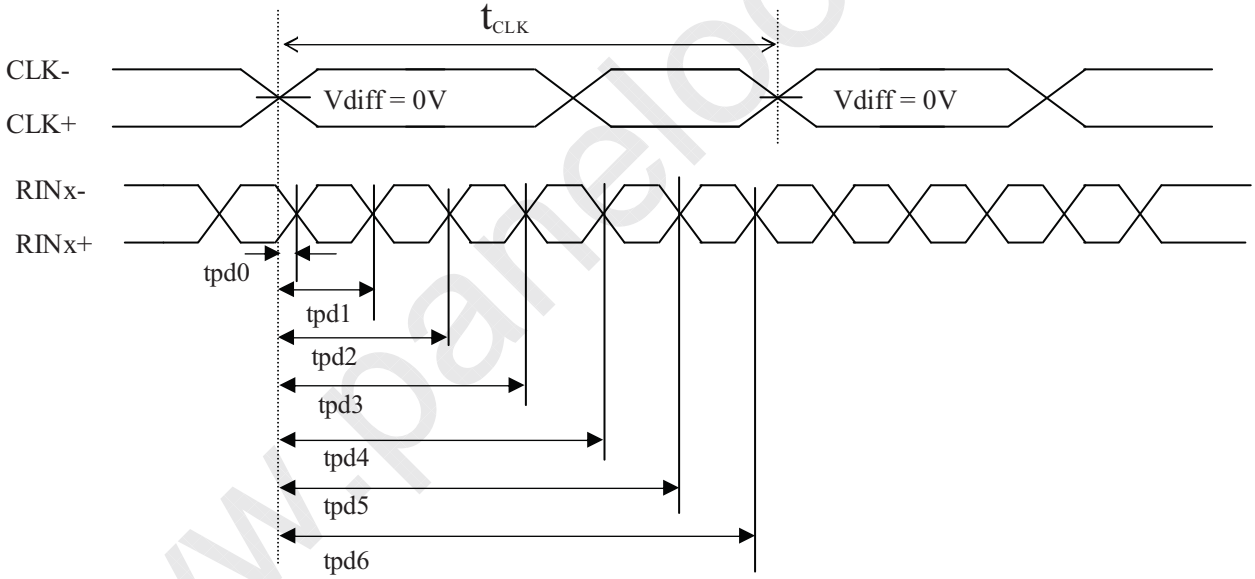
Fig.2 Timing characteristics of input signal

7.2. Input data signal and display position on the screen



Display position of Dat (V,H)

7-3. LVDS signal characteristics



	The item	Symbol	min.	typ.	max.	unit
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	-0.25	0	0.25	ns
	Delay time, CLK rising edge to serial bit position 1	tpd1	1*t_{CLK}/7-0.25	1* t_{CLK} /7	1* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 2	tpd2	2* t_{CLK} /7-0.25	2* t_{CLK} /7	2* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 3	tpd3	3* t_{CLK} /7-0.25	3* t_{CLK} /7	3* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 4	tpd4	4* t_{CLK} /7-0.25	4* t_{CLK} /7	4* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 5	tpd5	5* t_{CLK} /7-0.25	5* t_{CLK} /7	5* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 6	tpd6	6* t_{CLK} 7-0.25	6* t_{CLK} /7	6* t_{CLK} /7+0.25	

8. Input Signal, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray scale	Data signal																															
		Gray Scale	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	GS1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	⇩	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage.

Each basic color can be displayed in 1024 gray scales from 10 bits data signals. According to the combination of total 30 bits data signals, one billion-color display can be achieved on the screen.

9. Optical characteristics

Ta=25°C, Vcc=12.0V, V_{INV} =24.0V, Pdim=100%, Timing : 120Hz (typ. value)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21 θ22	CR≧10	70	88	-	Deg.	[Note1,4]
	Vertical	θ11 θ12		70	88	-	Deg.	
Contrast ratio		CRn	θ=0 deg.	1300	2000	-		[Note2,4]
Response time		τ_{DRV}		-	4	8	ms	[Note3,4,5]
MPRT(BET)		-		-	12	-	ms	[Note7]
Chromaticity	White	x		0.246	0.276	0.306	-	[Note4]
		y		0.251	0.281	0.311	-	
	Red	x		0.612	0.642	0.672	-	
		y		0.306	0.336	0.366	-	
	Green	x		0.249	0.279	0.309	-	
		y		0.571	0.601	0.631	-	
	Blue	x		0.115	0.145	0.175	-	
		y		0.037	0.067	0.097	-	
Gamma		-		-	2.2	-	-	
Luminance	White	Y_L		400	500	-	cd/m^2	
	Black	Y_{LB}		-	0.25	0.55		
Luminance uniformity	White	δw				1.25		[Note 6]
	Black	δb		-	-	(1.60)	-	

Measurement condition: Set the value of Pdim to maximum luminance of white.

*The measurement shall be executed 60 minutes after lighting at rating.

[Note] The optical characteristics are measured using the following equipment.

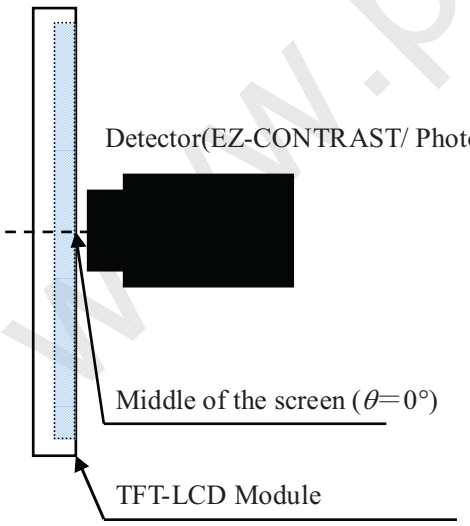


Fig.4-1 Measurement of viewing angle range and Response time.
Viewing angle range: EZ-CONTRAST
Response time: Photodiode

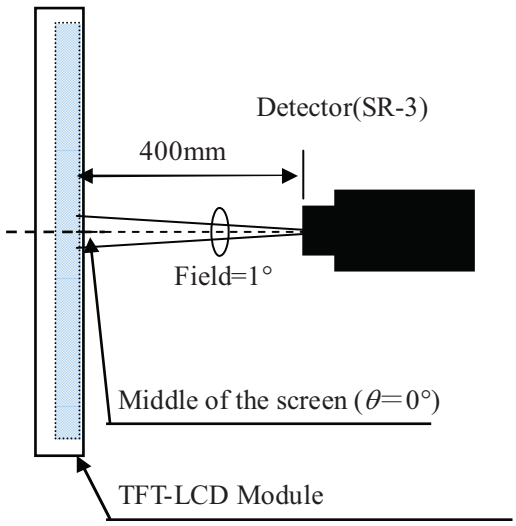
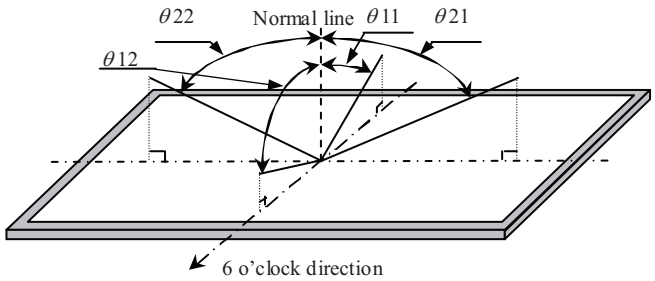


Fig.4-2 Measurement of Contrast, Luminance, Chromaticity.

[Note 1] Definitions of viewing angle range :



[Note 2] Definition of contrast ratio :

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

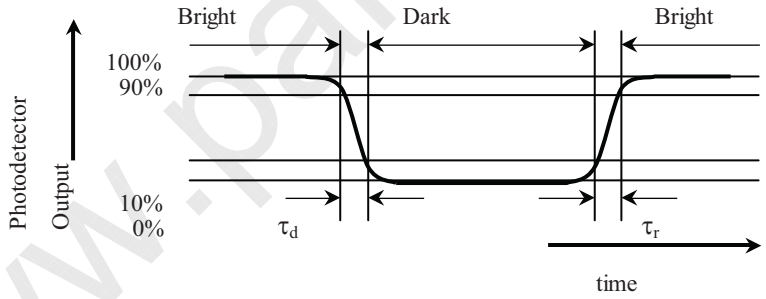
[Note 3] Definition of response time

The response time (τ_d and τ_r) is defined as the following figure and shall be measured by switching the input signal for "any level of gray (0%, 25%, 50%, 75% and 100%)" and "any level of gray (0%, 25%, 50%, 75% and 100%)".

	0%	25%	50%	75%	100%
0%		tr:0%-25%	tr:0%-50%	tr:0%-75%	tr:0%-100%
25%	td: 25%-0%		tr: 25%-50%	tr25%-75%	tr: 25%-100%
50%	td: 50%-0%	td: 50%-25%		tr: 50%-75%	tr: 50%-100%
75%	td: 75%-0%	td: 75%-25%	td: 75%-50%		tr: 75%-100%
100%	td: 100%-0%	td: 100%-25%	td: 100%-50%	td:100%-75%	

t* : x-y … response time from level of gray(x) to level of gray(y)

$\tau_r = \Sigma(tr:x\text{-}y)/10$, $\tau_d = \Sigma(td:x\text{-}y)/10$



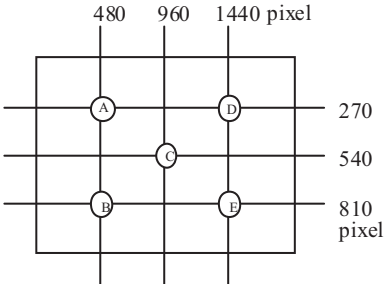
[Note 4] This shall be measured at center of the screen.

[Note 5] This value is valid when O/S driving is used at typical input time value.

[Note 6] Definition of white uniformity ;

White uniformity is defined as the following with five measurements. (A~E)

$$\delta w = \frac{\text{Maximum luminance of five points (brightness)}}{\text{Minimum luminance of five points (brightness)}}$$



[Note 7] Moving Picture Response Time (BET);

MPRT (BET) is measured by MPRT-1000 (OTSUKA ELECTRONICS co,ltd.)

10. Handling Precautions of the module

a) Be sure to turn off the power supply when inserting or disconnecting the cable.

b) This product is using the parts (inverter, CCFT etc), which generate the high voltage. Therefore, during operating, please don't touch these parts.

c) Brightness control voltage is switched for "ON" and "OFF", as shown in Fig.4. Voltage difference generated by this switching, ΔV_{INV}, may affect a sound output, etc. when the power supply is shared between the inverter and its surrounding circuit. So, separate the power supply of the inverter circuit with the one of its surrounding circuit.

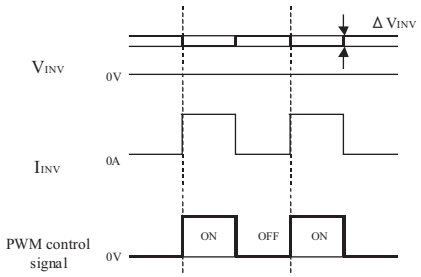


Fig.4 Brightness control voltage.

d) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.

e) Since the front polarizer is easily damaged, pay attention not to scratch it.

f) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.

g) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

h) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

i) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.

j) The module has some printed circuit boards (PCBs) on the back side, take care to keep them form any stress or pressure when handling or installing the module; otherwise some of electronic parts on the PCBs may be damaged.

k) Observe all other precautionary requirements in handling components.

l) When some pressure is added onto the module from rear side constantly, it causes display non-uniformity issue, functional defect, etc. So, please avoid such design.

m) When giving a touch to the panel at power on supply, it may cause some kinds of degradation. In that case, once turn off the power supply, and turn on after several seconds again, and that is disappear.

n) When handling LCD modules and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the LCD modules.

o) This LCD module is designed to prevent dust from entering into it. However, there would be a possibility to have a bad effect on display performance in case of having dust inside of LCD module. Therefore, please ensure to design your TV set to keep dust away around LCD module.

p) This LCD module passes over the rust.

q) Please fix the module on the point we recommend. If you fix the module another points, it is not possible to guarantee. (See the figure A.) ▲A-1

11. Packing form

a) Piling number of cartons : 2 maximum
b) Packing quantity in one carton : 8pcs.
c) Carton size : 1320(W)×1110(D)×950(H) [mm]
d) Total mass of one carton filled with full modules : 172kg (Max.)

12. Reliability test items

No.	Test item	Condition
1	High temperature storage test	Ta=60°C 240h
2	Low temperature storage test	Ta=-25°C 240h
3	High temperature and high humidity operation test	Ta=40°C ; 95%RH 240h (No condensation)
4	High temperature operation test	Ta=50°C 240h
5	Low temperature operation test	Ta=0°C 240h
6	Vibration test (non-operation)	Frequency: 10~57Hz/Vibration width (one side): 0.075mm : 58~500Hz/Acceleration: 9.8 m/s² Sweep time: 11 minutes Test period: 3 hours (1h for each direction of X, Y, Z)
7	Shock test (non-operation)	Maximum acceleration: 294m/s² Pulse width: 11ms, sinusoidal half wave Direction: +/-X, +/-Y, +/-Z, once for each direction.
8	ESD	* At the following conditions, it is a thing without incorrect operation and destruction. (1)Non-operation: Contact electric discharge ±10kV Non-contact electric discharge ±20kV (2)Operation Contact electric discharge ±8kV Non-contact electric discharge ±15kV Conditions: 150pF, 330ohm

[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

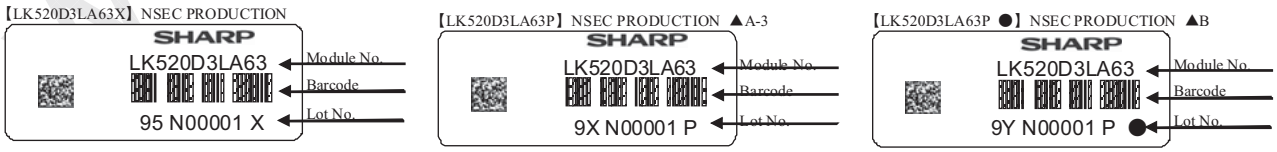
[Note]

These items apply to the single module.

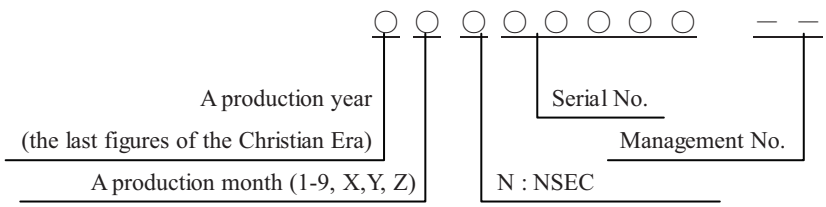
13. Others

1) Lot No. Label ;

The label that displays SHARP, product model LK520D3LA63, a product number is stuck on the lower right BL chassis 「 O 」.



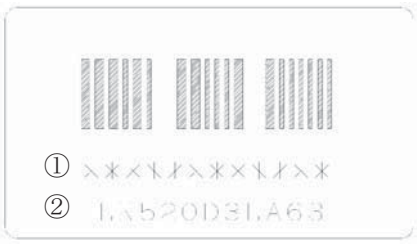
How to express Lot No.



2) User barcode label ▲B

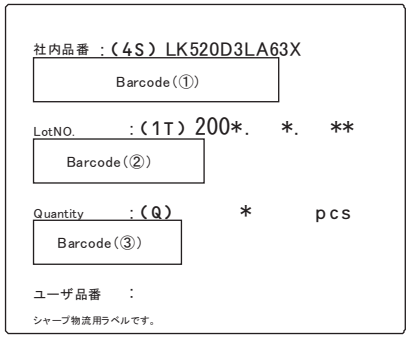
This label is stuck on the upper right BL chassis「 T 」.

Model Name	①	②
LK520D3LA63X	932226810682	LK520D3LA63
LK520D3LA63P	932227411682	LK520D3LA63(Suffix:P)
LK520D3LA63P●	932227411682	LK520D3LA63(Suffix:P)

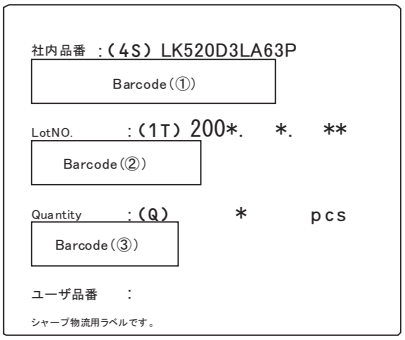


3) Packing Label

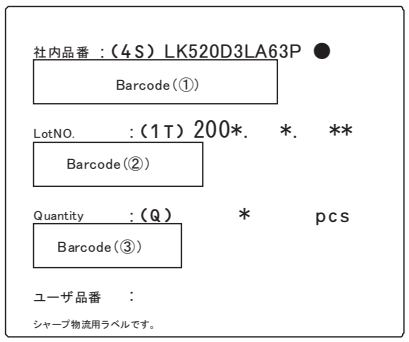
【LK520D3LA63X】NSEC PRODUCTION



【LK520D3LA63P】NSEC PRODUCTION ▲A-3



【LK520D3LA63P●】NSEC PRODUCTION ▲B



① Management No.
② Lot No. (Date)
③ Quantity

4) Adjusting volume has been set optimally before shipment, so do not change any adjusted value.
If adjusted value is changed, the specification may not be satisfied.

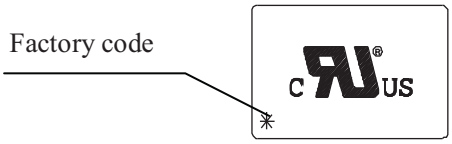
5) Disassembling the module can cause permanent damage and should be strictly avoided.

6) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

7) The chemical compound, which causes the destruction of ozone layer, is not being used.

8) Cold cathode fluorescent lamp in LCD PANEL contains a small amount of mercury. Please follow local ordinances or regulations for disposal. This sentence is displayed on the backside of the module.

9) This LCD module is appropriate to UL. Below figure shows the UL label.



10) When any question or issue occurs, it shall be solved by mutual discussion.

11) This LCD module is corresponded to RoHS. ‘’R.C.’’ label on the side of packing case shows it.

14. Carton storage conditions

Temperature	0°C to 40°C
Humidity	95%RH or less
Reference condition	: 20°C to 35°C, 85%RH or less (summer) : 5°C to 15°C, 85%RH or less (winter) • the total storage time (40°C, 95%RH) : 240H or less
Sunlight	Be sure to shelter a product from the direct sunlight.
Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Notes	Be sure to put cartons on palette or base, don't put it on floor, and store them with removing from wall. Please take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
Storage life	1 year

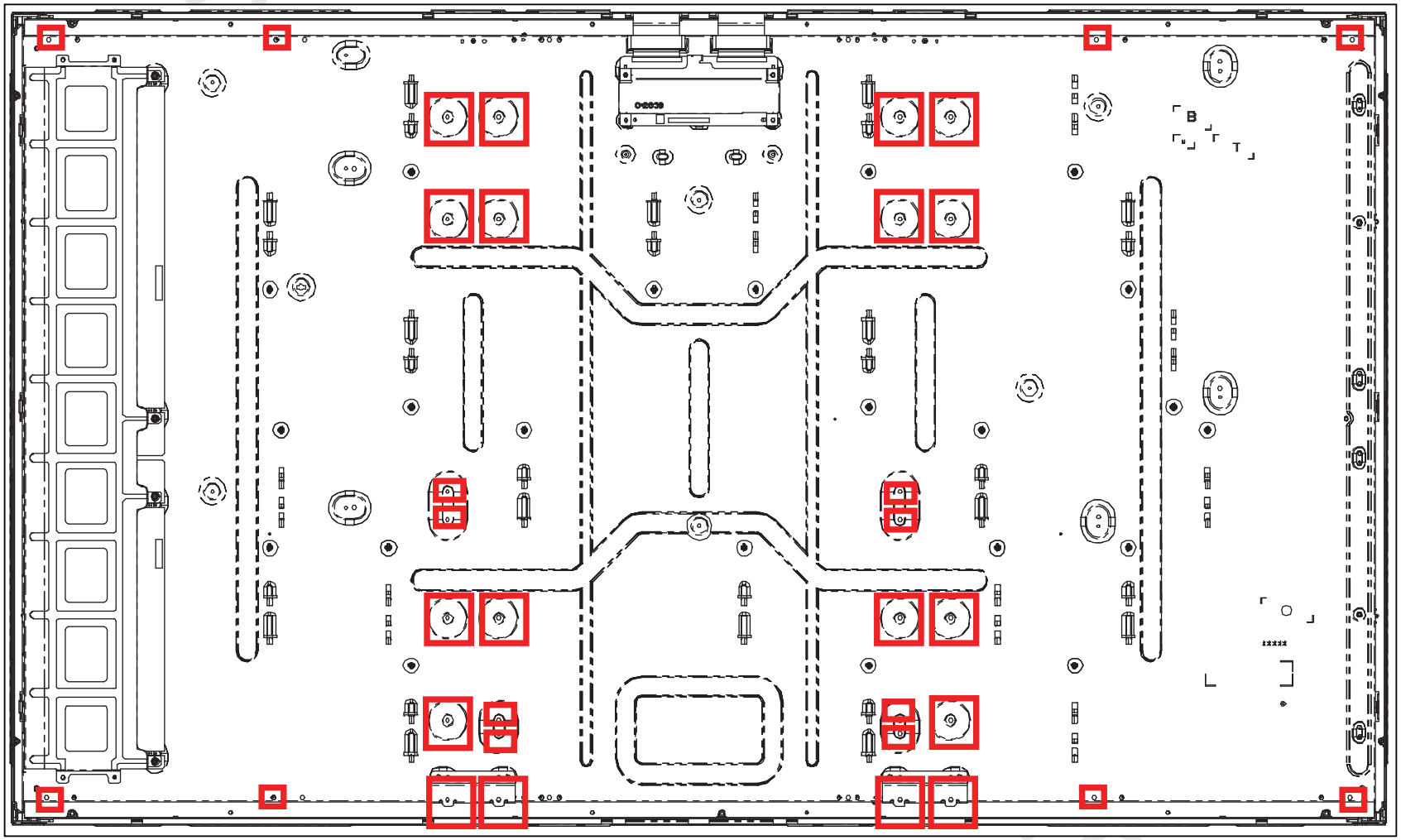
15. Records of design change

1) Change the inverter as countermeasures for shutdown from July 2009. [AVC-G1-09-0461] ▲A-2
2) Change the inverter, cancel of soft start, from October 2009. [AVC-G3-09-0297A] ▲A-2

16. Model list ▲B

Model name	Notes	Application time
LK520D3LA63X	Original model	
LK520D3LA63P	Design change model [AVC-G3-09-0297A]	Oct. 2009 ~
LK520D3LA63P●	C-PWB : for LA63X Other parts : LA63P	Nov. 2009

Figure A : Recommended Fixing Point ▲A-1



: fixing point

- We will guarantee 30G at fixing with screw above 34 points.

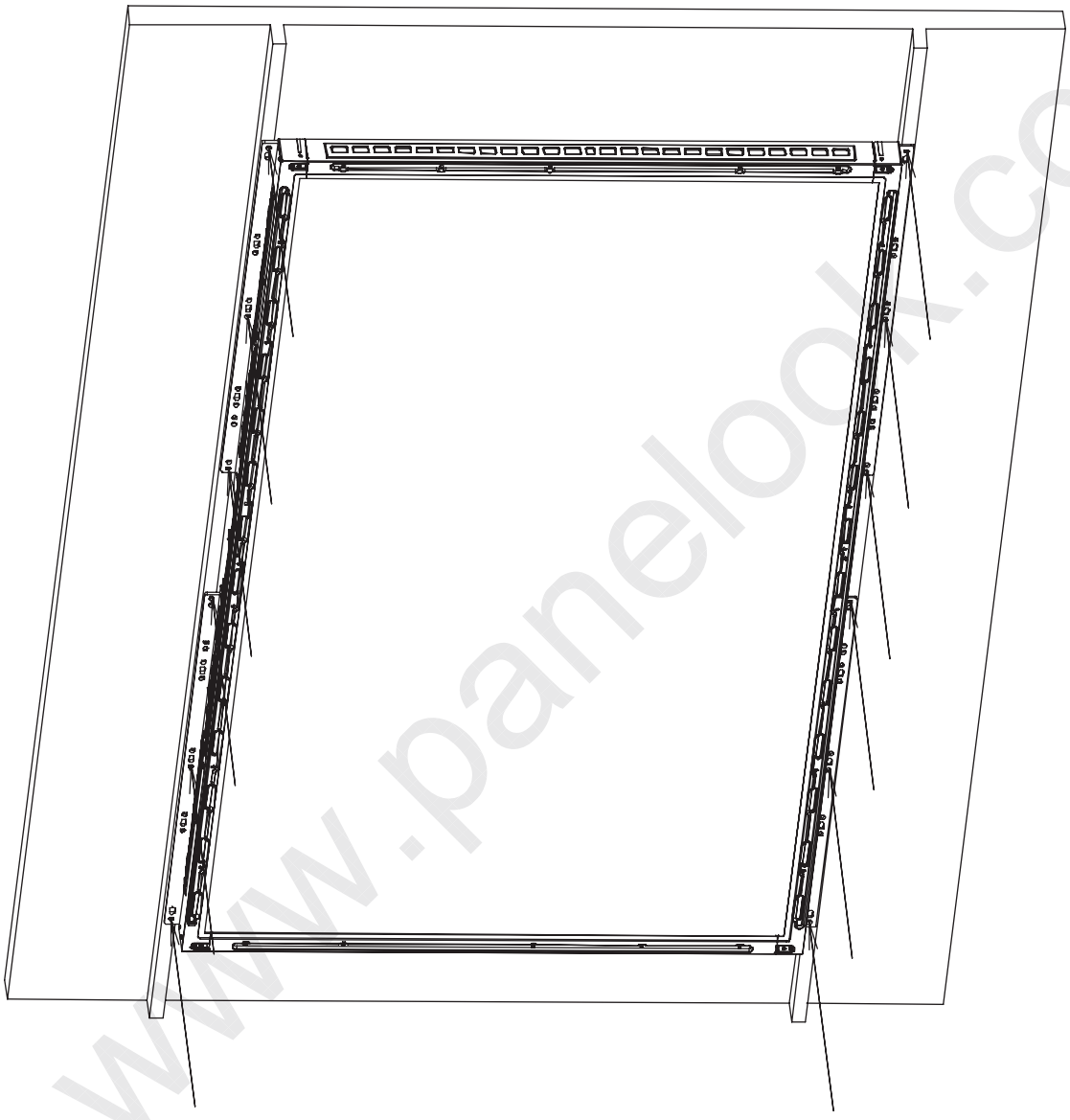
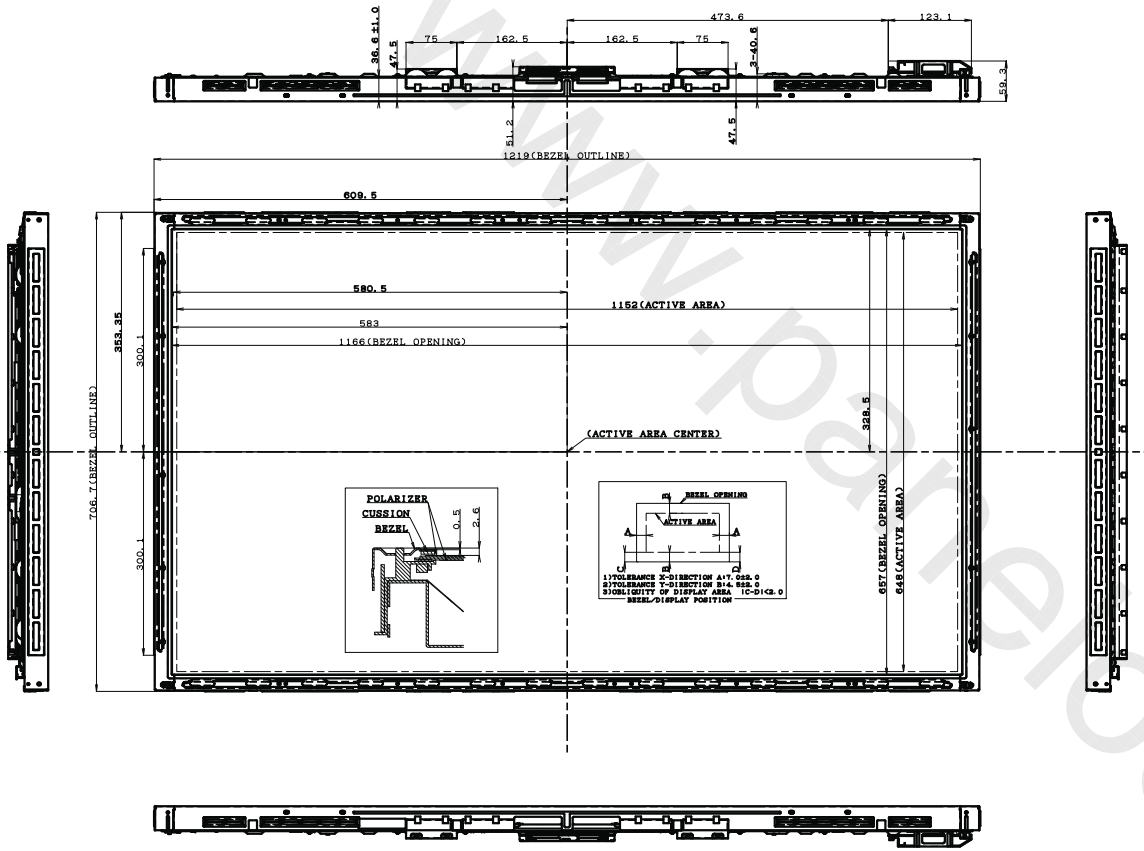
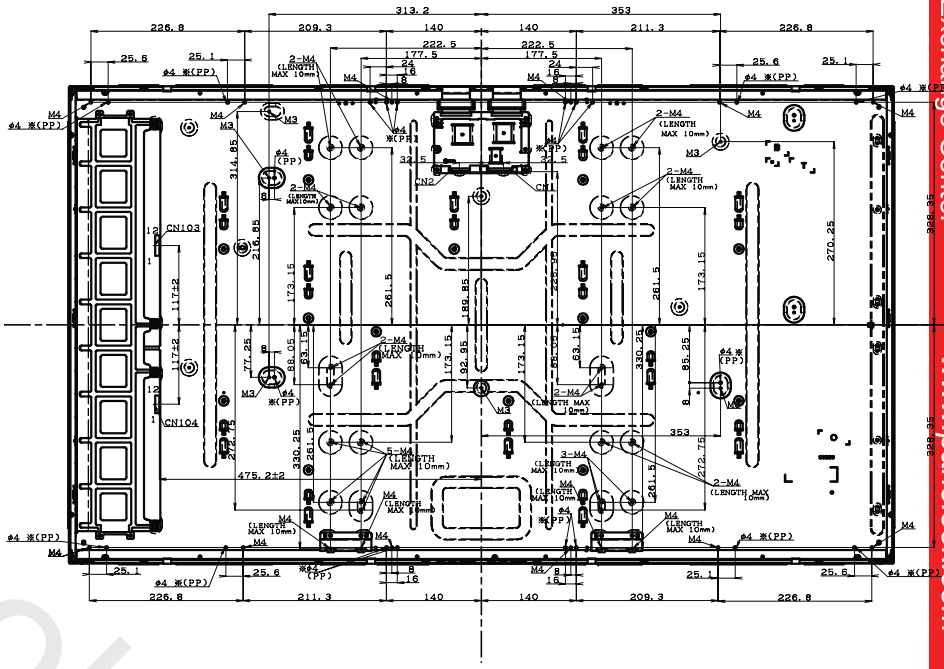


Figure of Shock test's jig
Module fixed position (M5 Bolt × 12)





2009.02.05

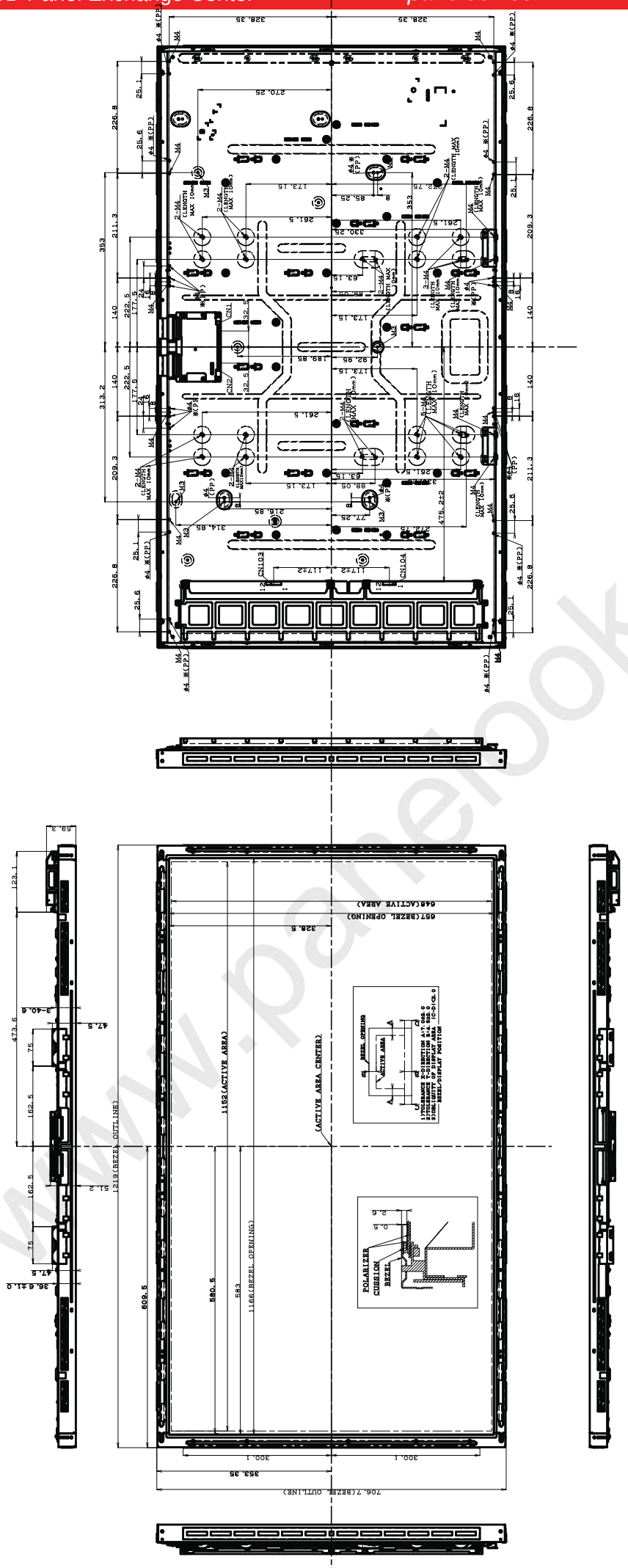
NOTE)

1. UNSPECIFIED TOLERANCE TO BE ±1.7
2. RIGHT AND LEFT SIDEPIECE IS SYMMETRIC SHAPE
3. M3 means M3 tapping hole.
4. M4 means M4 tapping hole.

※ PP=A POSITIONING PROJECTION

TFT-LCD MODULE OUTLINE DIMENSIONS

LK520D3LA63X



TFT-LCD MODULE OUTLINE DIMENSIONS

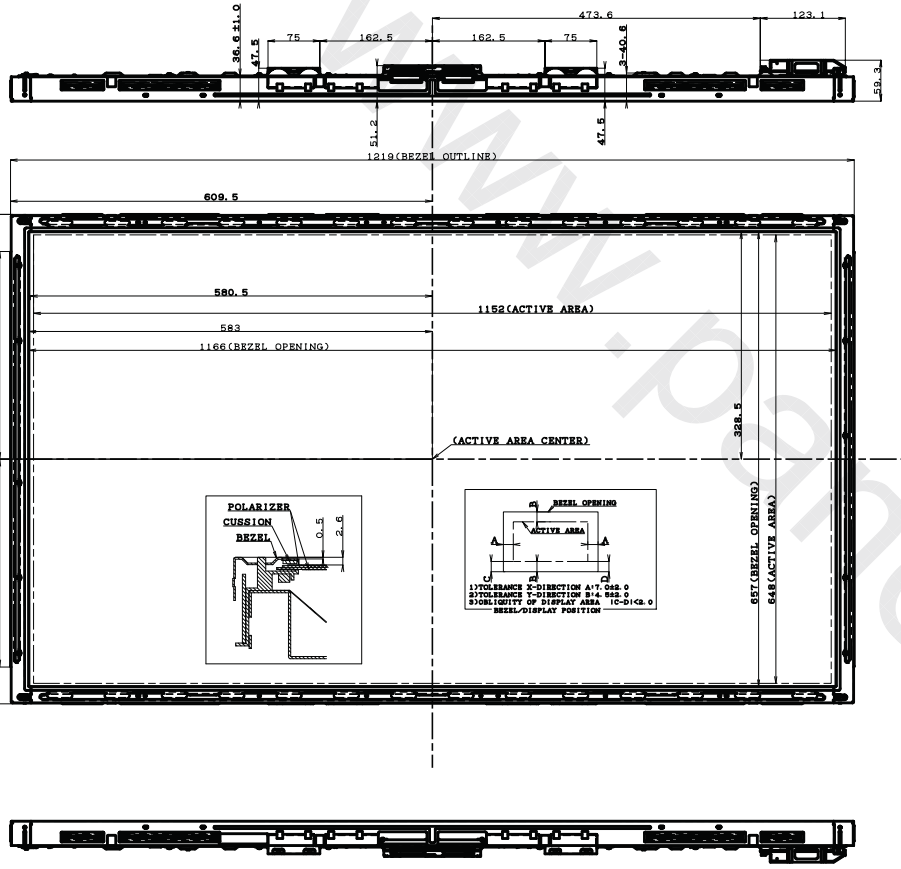
LK520D3LA63P △A3

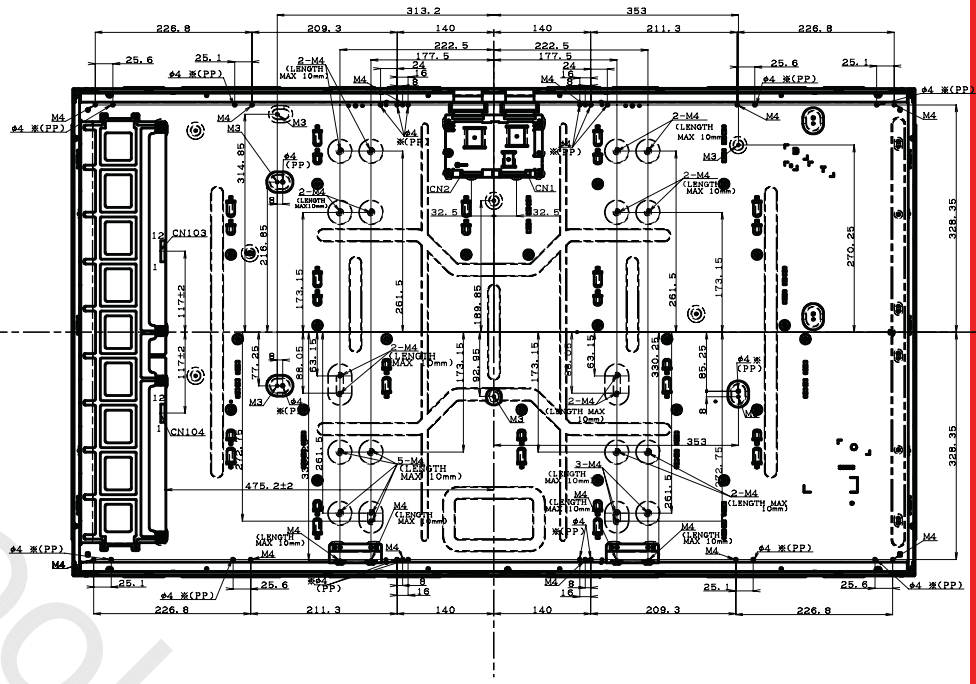
2009.07.17

NOTE)

1. UNSPECIFIED TOLERANCE TO BE ±1.7
2. RIGHT AND LEFT SIDEPIECE IS SYMMETRIC SHAPE
3. M3 means M3 tapping hole.
4. M4 means M4 tapping hole.

※ PP=A POSITIONING PROJECTION





2009.10.28

NOTE)

1. UNSPECIFIED TOLERANCE TO BE ±1.7
2. RIGHT AND LEFT SIDEPIECE IS SYMMETRIC SHAPE
3. M3 means M3 tapping hole.
4. M4 means M4 tapping hole.

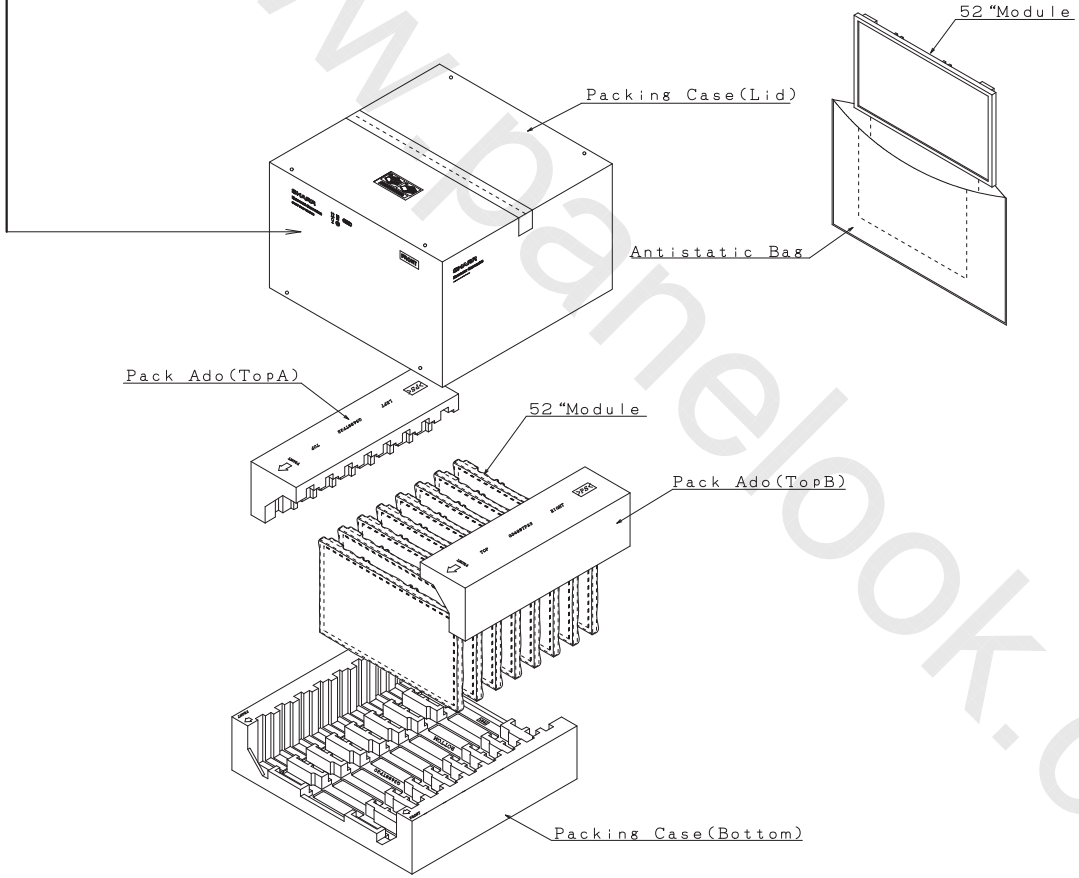
※ PP=A POSITIONING PROJECTION

TFT-LCD MODULE OUTLINE DIMENSIONS

LK520D3LA63P● △B

R.C.

There is R.C. marking on the this side.



Parts Name	Material
Packing Case(Lid)	Cardboard
Pack Ado(Bottom)	PS
Pack Ado(TopA)	PS
Pack Ado(TopB)	PS
Wooden Palette	Ply woods
Antistatic Bag	PE