

1. Application

This specification applies to the color 64.5" TFT-LCD module LK645D3LZ9S.

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2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT ($\underline{\text{Thin }}\underline{\text{Film }}\underline{\text{Transistor}}$). It is composed of a color TFT-LCD panel, driver ICs, control circuit, power supply circuit, inverter circuit and back light system etc. Graphics and texts can be displayed on a $1920 \times \text{RGB} \times 1080$ dots panel with about 1073 million colors by using LVDS ($\underline{\text{Low }}\underline{\text{Voltage }}\underline{\text{Differential }}\underline{\text{Signaling}}$) to interface, +12V of DC supply voltages.

This module also includes the DC/AC inverter to drive the CCFTs. (+60V/+12 of DC supply voltage)

And in order to improve the response time of LCD, this module applies the Over Shoot driving (O/S driving) technology for the control circuit. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With this technology, image signals can be set so that liquid crystal response completes within one frame. As a result, motion blur reduces and clearer display performance can be realized.

This LCD module also adopts Double Frame Rate driving method. With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.

3. Mechanical Specifications

Parameter	Specifications	Unit
Dignlay cigo	163.9 (Diagonal)	cm
Display size	64.5 (Diagonal)	inch
Active area	1428.48(H) x 803.52 (V)	mm
Pixel Format	1920(H) x 1080(V)	missal
Fixel Politiat	(1pixel = R + G + B dot)	pixel
Pixel pitch	0.744(H) x 0.744 (V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Unit Outline Dimensions (*1)	1498(W) x 874.4 (H) x60.8 (D)	mm
Mass	32.5+/- 1.0	kg
Surface treatment	Anti glare, low reflection coating Hard coating: 2H	

^(*1) Outline dimensions are shown in Fig.1-1,1-2.



4. Input Terminals

4-1. TFT panel driving

CN1 (Interface signals and +12V DC power supply) (Shown in Fig.1-2)

Using connector : FI-RE51S-HF (Japan Aviation Electronics Ind., Ltd.)

Mating connector : FI-RE51HL, FI-RE51CL (Japan Aviation Electronics Ind., Ltd.)

Mating	LVDS transmit	ter :THC63LVD1023(THine) or equivalent of	levice
Pin No.	Symbol	Function	Remark
1	GND		
2	TEMP1	Data1 of panel surface temperature [Note3]	Internally Pull up(by 10kΩ)
3	TEMP2	Data2 of panel surface temperature [Note3]	Internally Pull up(by 10kΩ)
4	TEMP3	Data3 of panel surface temperature [Note3]	Internally Pull up(by 10kΩ)
5	FRAME	Frame frequency setting H: 120Hz,L: 100Hz	Internally Pull down(by 10kΩ)
6	O/S_set	O/S operating setting [Note3]	Internally Pull up(by 10kΩ)
7	SELLVDS	Select LVDS data order [Note1]	Internally Pull up(by 10kΩ)
8	Reserved		Don't use(must be open)
9	R/L	Horizontal shift direction [Note2]	Internally Pull down(by 10kΩ)
10	Reserved		Don't use(must be open)
11	GND		
12	AIN0-	Aport (-)LVDS CH0 differential data input	
13	AIN0+	Aport (+)LVDS CH0 differential data input	
14	AIN1-	Aport (-)LVDS CH1 differential data input	
15	AIN1+	Aport (+)LVDS CH1 differential data input	
16	AIN2-	Aport (-)LVDS CH2 differential data input	
17	AIN2+	Aport (+)LVDS CH2 differential data input	
18	GND		
19	ACK-	Aport LVDS Clock signal(-)	
20	ACK+	Aport LVDS Clock signal(+)	
21	GND		
22	AIN3-	Aport (-)LVDS CH3 differential data input	
23	AIN3+	Aport (+)LVDS CH3 differential data input	
24	AIN4-	Aport (-)LVDS CH4 differential data input	
26	AIN4+	Aport (+)LVDS CH4 differential data input	
27	GND GND		
28	BIN0-	Bport (-)LVDS CH0 differential data input	<u> </u>
29	BIN0+	Bport (+)LVDS CH0 differential data input	
30	BIN1-	Bport (-)LVDS CH1 differential data input	
31	BIN1+	Bport (+)LVDS CH1 differential data input	
32	BIN2-	Bport (-)LVDS CH2 differential data input	
33	BIN2+	Bport (+)LVDS CH2 differential data input	
34	GND	The state of the s	
35	BCK-	Bport LVDS Clock signal(-)	
36	BCK+	Bport LVDS Clock signal(+)	
37	GND		
38	BIN3-	Bport (-)LVDS CH3 differential data input	
39	BIN3+	Bport (+)LVDS CH3 differential data input	
40	BIN4-	Bport (-)LVDS CH4 differential data input	
41	BIN4+	Bport (+)LVDS CH4 differential data input	
42	GND	GND	
43	GND	GND	
44	GND	GND	
45	GND	GND	



46	GND	GND	
47	Reserved		Don't use(must be open)
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

CN2 (Interface signals) (Shown in Fig1-2)

Using connector : FI-RE41S-HF (Japan Aviation Electronics Ind., Ltd.)

Matin FI-RE41HI FI-RE41CI (Japan Aviation Electronics Ind. Ltd.)

onnector	: FI-RE41HL, FI-RE41CL (Japan Aviation	
Symbol	l	Remark
Reserved (VCC)	(+12V Power Supply)	
Reserved		Don't use(must be open
Reserved		Don't use(must be open
Reserved		
Reserved		
CIN0-		
CIN0+		
CIN1-	Cport (-)LVDS CH1 differential data input	
CIN1+	Cport (+)LVDS CH1 differential data input	
CIN2-	Cport (-)LVDS CH2 differential data input	
CIN2+	Cport (+)LVDS CH2 differential data input	
GND		
CCK-	Cport LVDS Clock signal(-)	
CCK+	Cport LVDS Clock signal(+)	
GND		
CIN3-	Cport (-)LVDS CH3 differential data input	
CIN3+	Cport (+)LVDS CH3 differential data input	
CIN4-		
CIN4+		
GND		
	Dport (-)LVDS CH0 differential data input	
	1 ^ \	
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
	Dnort LVDS Clock signal(-)	
	port Dr Do Grook organit ()	
	Dnort (-)I VDS CH3 differential data input	
	<u> </u>	
		
GND	Dport (+)L v D3 C114 differential data hiput	
I I I I I I I I I I I I I I I I I I I	1	1
	Symbol Reserved (VCC) Reserved (VCC) Reserved (VCC) Reserved (VCC) Reserved Reserved Reserved Reserved Reserved Reserved CIN0- CIN0- CIN0- CIN1- CIN1- CIN2- CIN2- CIN2+ GND CCK- CCK+ GND CIN3- CIN3- CIN4- CIN4- CIN4- CIN4- GND DIN0- DIN0- DIN0- DIN0- DIN1- DIN1- DIN1- DIN1- DIN1- DIN1- DIN2- DIN2- GND DCK- DCK+ GND DCK- DCK+ GND DIN3- DIN3- DIN3- DIN4- DIN4- DIN4-	Reserved (VCC) (+12V Power Supply) Reserved Reserved Reserved Reserved Reserved Reserved CIN0- Cport (-)LVDS CH0 differential data input CIN0- Cport (+)LVDS CH0 differential data input CIN1- Cport (-)LVDS CH1 differential data input CIN1- Cport (-)LVDS CH1 differential data input CIN2- Cport (-)LVDS CH2 differential data input CIN2- Cport (-)LVDS CH2 differential data input CIN2- Cport (-)LVDS CH2 differential data input GND CCK- Cport LVDS Clock signal(-) CCK- Cport LVDS Clock signal(+) GND CIN3- Cport (-)LVDS CH3 differential data input CIN4- Cport (-)LVDS CH4 differential data input CIN4- Cport (-)LVDS CH4 differential data input GND GND GND DIN0- Dport (-)LVDS CH4 differential data input DIN1- Dport (-)LVDS CH1 differential data input DIN1- Dport (-)LVDS CH1 differential data input DIN1- Dport (-)LVDS CH1 differential data input DIN1- Dport (-)LVDS CH2 differential data input DIN2- Dport (-)LVDS CH3 differential data input DIN3- Dport (-)LVDS CH3 differential data input DIN3- Dport (-)LVDS CH3 differential data input DIN3- Dport (-)LVDS CH4 differential data input DIN3- Dport (-)LVDS CH4 differential data input DIN4- Dport (-)LVDS CH4 differential data input

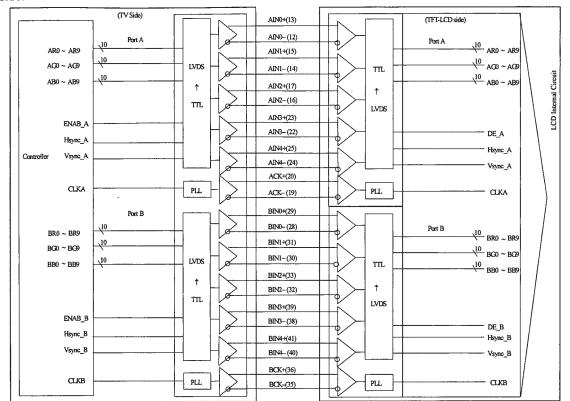
[note] GND of a liquid crystal panel drive part has connected with a module chassis.

[note] L,"0": Low level voltage (GND) H,"1": High level voltage(3.3V)



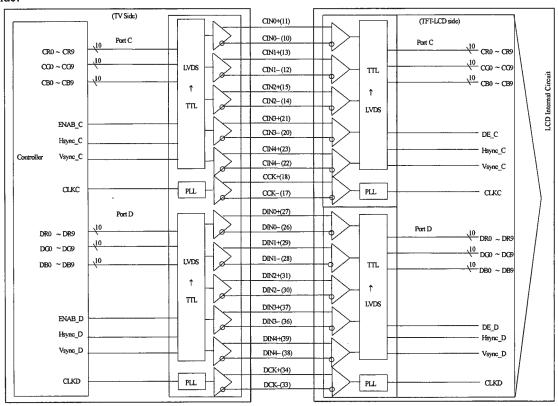
Interface block diagram

CN1 side:



 $Corresponding \ Transmitter: \ THC63LVD1023 \ (THine) \ or \ equivalent \ device.$

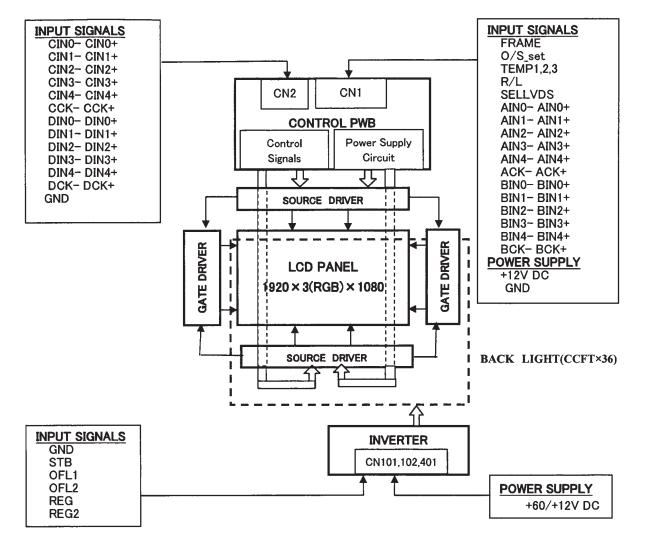
CN2 side:



Corresponding Transmitter: THC63LVD1023 (THine) or equivalent device.

Block Diagram (LCD Module)

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[Note 1]SELLVDS

SELLVDS					
Data	L(GND) *	H(3.3V) * [default]			
TA0	R0(LSB)	R4			
TA1	R1	R5			
TA2	R2	R6			
TA3	R3	R7			
TA4	R4	R8			
TA5	R5	R9(MSB)			
TA6	G0(LSB)	G4			
TB0	G1	G5			
TB1	G2	G6			
TB2	G3	G7			
TB3	G4	G8			
TB4	G5	G9(MSB)			
TB5	B0(LSB)	B4			
TB6	B1	B5			
TC0	B2	B6			
TC1	В3	B7			
TC2	B4	B8			
TC3	B5	B9(MSB)			
TC4	(HSYNC)**	(HSYNC)**			
TC5	(VSYNC)**	(VSYNC)**			
TC6	DE(*)	DE(*)			
TD0	R6	R2			
TD1	R7	R3			
TD2	G6	G2			
TD3	G7	G3			
TD4	В6	B2			
TD5	B7	B3			
TD6	N/A	N/A			
TE0	R8	R0(LSB)			
TE1	R9(MSB)	R1			
TE2	G8	G0(LSB)			
TE3	G9(MSB)	G1			
TE4	B8	B0(LSB)			
TE5	B9(MSB)	B1			
TE6	N/A	N/A			

^{*}SELLVDS=H JEIDA Mode

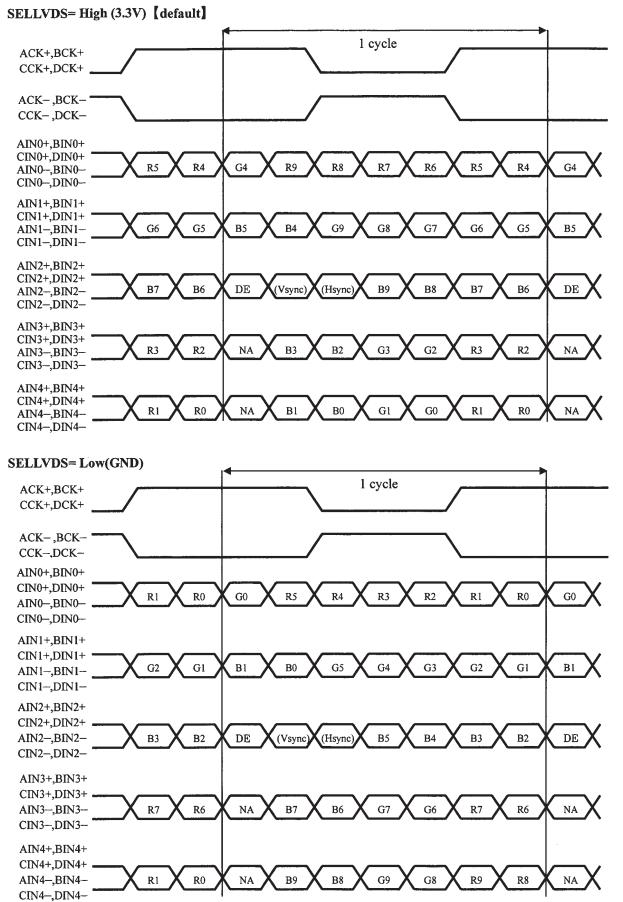
NA: Not Available

^{*}SELLVDS=L VESA Mode

^(*)Since the display position is prescribed by the rise of DE(Display Enable)signal, please do not fix DE signal during operation at "High".

^{**}HSYNC and VSYNC are not necessary





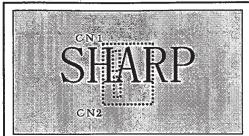
DE: Display Enable, Vsync: Vertical Sync, Hsync: Horizontal Sync

NA: Not Available (Fixed Low)



[Note 2]Display reversal function Normal (Default)

R/L: L (GND)



Horizontal reverse image

R/L: H(3.3V)



[Note 3] O/S Setting

According as the surface temperature of the panel, enter the optimum 3 bit signal into pin No.2,3,4. Measuring the correlation between detected temperature by the sensor on PWB in users side and actual surface temperature of panel at center, convert the temperature detected by the sensor to the surface temperature of panel to enter the 3 bit temperature data.

	Surface temperature of panel							
Pin No.	0-5℃	5-10℃	10-15℃	15 - 20℃	20-25℃	25-30℃	30-35℃	35°C and
								above
4	0	0	0	0	1	1	1	1
3	0	0	1	1	0	0	1	1
2	0	1	0	1	0	1	0	1

^{*0:} Low level voltage (GND) 1: High level voltage(3.3V)

^{*}For overlapping temperatures (such as 5° C, 10° C, 15° C, 20° C, 25° C, 30° C, 35° C) select the optimum parameter, judging from the actual picture image.



4-2. Backlight driving

CN102(Interface signals and +3.3V DC power supply) (Shown in Fig.1-2)

Using connector: S09B-PASK-2 (J.S.T. Mfg Co.,Ltd.)

Mating connector: PAP-09V-S (J.S.T. Mfg Co.,Ltd.)

Pin No. Symbol Function		Function	Remarks		
1	GND	GND			
2	STB	Inverter ON/OFF	[Note 1]		
3	3 OFL1 External PWM Dimming Phase1 (P-PWM)				
4 Reserved Not Connect		Not Connect			
5	ERR	Error Detection. Normal:High/Abnormal:Low	[Note 2]		
6	REG	Internal Oscillation Selection (Must be open or 0V)			
7 REG2 External PWM Dimming Selection (Must		External PWM Dimming Selection (Must be 3.3V)			
8	8 Reserved Not Connect				
9	9 OFL2 External PWM Dimming Phase2 (P-PWM)				

^{*}GND of an inverter board is connected to GND of a module chassis and a liquid crystal panel drive part.

[Note 1] Inverter Control

Input voltage	Function
3.3V	Inverter: ON
0V	Inverter: OFF

[Note 2] Error Detection

Pin No.5 is used for the error detection of the inverter driving.

Output voltage	Inverter Driving
Low	Abnormal
High	Normal

CN101, CN401(+12V, +60V DC power supply) (Shown in Fig.1-2)

Using connector: S3P-VH (J.S.T. Mfg Co.,Ltd.) Mating connector: VHR-3N (J.S.T. Mfg Co.,Ltd.)

Pin No.	Symbol	Function
1	V_{INV1}	60V
2	GND	GND
3	V _{INV2}	12V

^{*}GND of an inverter board is connected to GND of a module chassis.

4-3. The back light system characteristics

The back light system is direct type with 36 CCFTs (Cold Cathode Fluorescent Tube).

The characteristics of the lamp are shown in the following table.

The value mentioned below is at the case of one CCFT.

Item	Symbol	Min.	lyp.	Max.	Unit	Remarks
Life time	TL	-	60000	-	Hour	[Note]
		·				

[Note] • Lamp life time is defined as the time when brightness becomes 50% of the original value in the continuous operation under the condition of Ta=25 °C and brightness control(OFL1,2=100%).

· Above value is applicable when the long side of LCD module is placed horizontally (Landscape position).

(Lamp lifetime may vary if LCD module is in portrait position due to the change of mercury density inside the lamp.)

5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage (for Control)	Vı	Ta=25 °C	-0.3 ~ 3.6	V	[Note 1]
12V supply voltage (for Control)	VCC	Ta=25 °C	0~+14	V	
Input voltage (for Inverter)	STB OFL1, 2	Ta=25 ℃	0~+3.6	V	
60V supply voltage (for Inverter)	V _{INV1}	Ta=25 ℃	0 ~ +70	V	
12V supply voltage (for Inverter)	V _{INV2}	Ta=25 °C	0~ +13.5	V	
Storage temperature	Tstg	-	-25 ~ +60	ပ	D.I. 4. 21
Operation temperature (Ambient)	Тора	-	0 ~ +50	$^{\circ}$	[Note 2]

[Note 1]SELLVDS, R/L, Frame,O/S_set, Temp1, Temp2, Temp3

[Note 2]Humidity 95%RH Max.(Ta \leq 40°C)

Maximum wet-bulb temperature at 39 $^{\circ}\text{C}$ or less.(Ta>40 $^{\circ}\text{C}$) / No condensation.

6. Electrical Characteristics

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6-1. Control circuit driving

Ta=25 ℃

Para	Parameter Parameter			Min.	Тур.	Max.	Uniit	Remark
±12V supply	Light Supply voltage			11.0	12.0	12.6	V	[Note 1]
+12V supply voltage	C	urrent	Icc	-	1.5	2.6	A	[Note 2]
voitage			Iccs	0.3			A	[Note 7]
	Permissible input ripple voltage			-	-	100	mV _{P-P}	Vcc = +12.0V
Differential is	ifferential input High		VTH	-		100	mV	$V_{CM} = +1.2V$
threshold vol	threshold voltage Low		VTL	-100	-	-	mV	[Note]
Input Lo	ow vol	tage	VıL	-	-	0.8	V	[Note 21
Input Hi	igh vo	ltage	Vih	2.0	-	3.6	V	[Note 3]
Input leak	curren	t (Low)	In		_	400	μА	$V_I = 0V$
						100	μπ.	[Note 4]
Input leak current (High)			In	_	_	400	μΑ	$V_I = 3.3V$
						+50	μΛ	[Note 5]
Termin	Terminal resistor			-	100		Ω	Differential input

[Note] Vcm: Common mode voltage of LVDS driver.

[Note 1]

Input voltage sequences

 $0.1 \text{ ms} < t1 \leq 20 \text{ms}$

10 ms < t2

0 ms < t3

0 ms < t4

 $t6 \ge 0s$

t7 ≧ 1s

 $t5 \ge 1s$

t8 ≧ 1ms

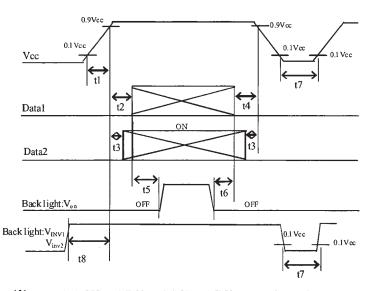
Dip conditions for supply voltage

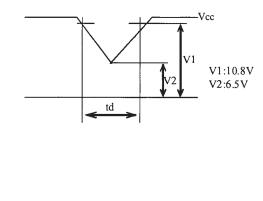
a)
$$6.5V \le Vcc < 10.8V$$

 $td \leq 10ms$

b) Vcc < 6.5V

Dip conditions for supply voltage is based on input voltage sequence.

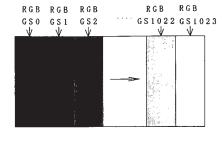




- Matal: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±, CCK±, CIN0±,
 Matal: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, BIN4±, CCK±, CIN0±,
 Matal: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, BIN4±, CCK±, CIN0±,
 Matal: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±, CCK±, CIN0±,
 Matal: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±, CCK±, CIN0±,
 Matal: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, BIN4±, CCK±, CIN0±,
 Matal: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN3±, BIN4±, AIN3±,
 Matal: ACK±, AIN0±, AIN1±,
 Matal: ACK±, AIN0±, AIN1±,
 Matal: ACK±, AIN0±,
 Matal: ACK±, AIN0±,
 Matal: ACK±,
 Matal: ACK CIN1±, CIN2±, CIN3±, CIN4±, DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±
- Data2:R/L,SELLVDS,FRAME,O/S set,TEMP1,2,3

About the relation between data input and back light lighting, please base on the above-mentioned input sequence. When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

[Note 2] Maximum current situation: white (RGB GS1023) (Vcc = +12.0V)Typical current situation: 1024 gray-bar patterns. (Vcc = +12.0V) The explanation of RGB gray scale is seen in section 8.



Vcc = 12.0VCK = 74.25MHz $Th = 7.41 \mu s$

[Note 3] FRAME, O/S set, R/L, SELLVDS, TEMP3, TEMP2, TEMP1

[Note 4] FRAME, R/L

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[Note 5] TEMP3, TEMP2, TEMP1, O/S_set, SELLVDS

[Note 6] ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±, CCK±,CIN0±, CIN1±, CIN2±, CIN3±, CIN4±, DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±

[Note 7] The minimum current value is a value when inputting only voltage (Vcc=+12V) and cutting an incoming signal (CK,ENAB,DATA)



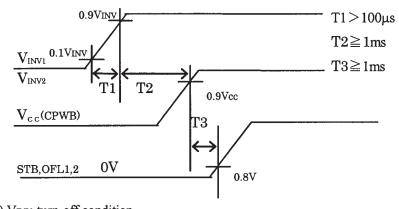
6-2. Inverter driving for back light

The back light system is direct type with 36 CCFTs (Cold Cathode Fluorescent Tube).

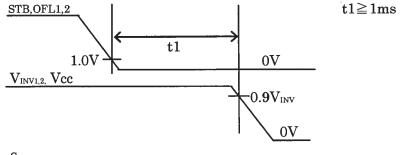
Ta=25℃

	Parameter	Symbol	Min.	Тур.	Max.	Unit	Remark			
	Current dissipation	Inv 1	-	6.2	6.8	A	$V_{INV1} = 60V$			
+60V	Current dissipation	Inv 2	5.4	5.8	6.2	A	STB= 3.3V OFL1,2 = 100%			
	Supply voltage	Vinvi	54.0	60	66.0	V	[Note 1,3]			
+12V	Supply voltage	Vinv2	10.8	12.0	13.2	V	$I_{typ} = 100 \text{mA}$			
Per	missible input ripple voltage	Vrf	-	-	600	mV_{p-p}	$V_{INVI} = +60V$			
Iı	nput voltage (Low)	Vonl	0		0.8	V	STB, OFL1,2			
Ir	nput voltage (High)	V _{onh}	2.4	3.3	3.6	V	[Note 1]			
Bri	ghtness control Duty		20	\rightarrow	100	%	DI . 01			
	vs Brightness level (Reference value)	-	10	→	100	%	[Note 2]			

 $[Note \ 1] \quad 1) V_{INV}\text{-}turn\text{-}on \ condition}$



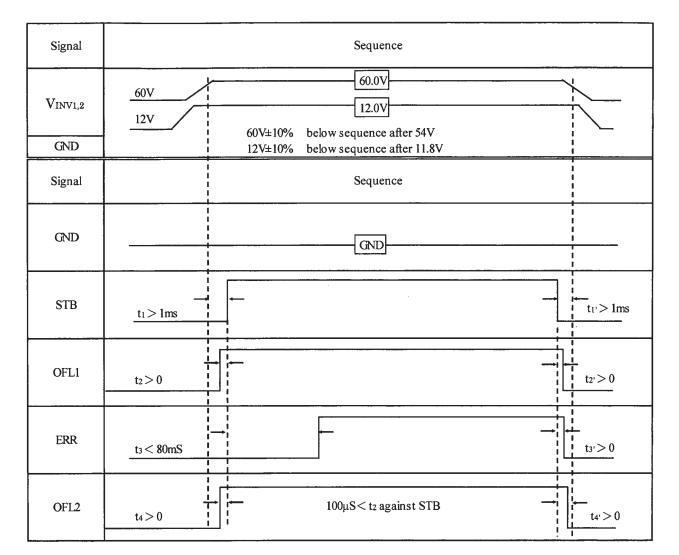
2) Vinv-turn-off condition



3) Power Sequence

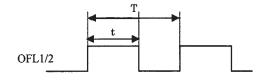
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[Note 2] Brightness Control (Pulse PWM Dimming)

Pin No.3, 9 is used for the control of the PWM duty with input pulse.



 $Ta = 25^{\circ}C$

		MIN	TYP	MAX	Remark
Pulse signal	[Hz]	140	-	350	
DUTY (t/T)	[%]	20	-	100	

[Note] There is a case that lamp mura may happen, depending on ambient temperature, in dimming. Minimum dimming level should be set according to your evaluation of actual display performance. (Minimum duty 60% at below 15°C)

[Note] In case of using Pulse Dimming, be careful so that the OFL1,2 signal (Pin 3,9) doesn't have glitch.

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[Note 3] Current dissipation 1: The regulation value within 120 minutes after the turning on.

(*It doesn't include Rush current.)

Current dissipation 2: The regulation value since then of 120 minutes after the turning on. [Note] The inverter unit is driving at the following drive frequency.

- *The lamp drive frequency: 52kHz±0.5kHz
- *The burst Brightness control drive frequency: 140Hz±10 Hz

The above drive frequency and the module drive frequency are cause and there is possibility that the backlight display problem occurs. When setting the drive frequency of the module, the interference with the above frequency make not occur.



7. Timing characteristics of input signals

7-1. Timing characteristics

Timing diagrams of input signal are shown in Fig.2.

	Symbol	Min.	Тур.	Max.	Unit	Remark		
Clock	Frequency	1/Tc	55	74.25	80	MHz		
	Horizontal period	TH	515	550	825	clock		
1	Horizontal period	111	6.94	7.41	11.1	μs		
Data enable	Horizontal period (High)	THd	480	480	480	clock		
signal	Vertical period	TV	1120	1125	1232	line		
	vertical period	''	73.052	120	120.60	MHz clock µs clock line Hz		
	Vertical period (High)	TVd	1080	1080	1080	line		

[Note] -When vertical period is very long, flicker and etc. may occur.

- -Please turn off the module after it shows the black screen.
- -Please make sure that length of vertical period should become of an integral multiple of horizontal length of period. Otherwise, the screen may not display properly.
- -As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.

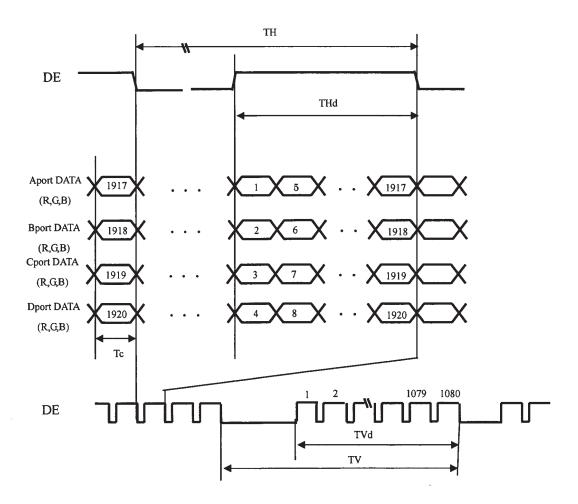


Fig.2 Timing characteristics of input signals



7-2. Input data signal and display position on the screen

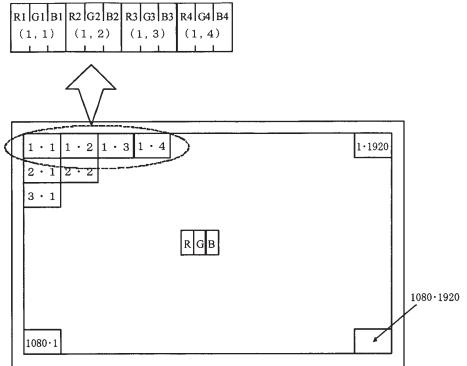


Fig. 3 Display position of Data (V,H)

8. Input Signal, Basic Display Colors and Gray Scale of Each Color

	iput Sigi				P	, _	010									ata																
	Colors & Gray scale	Gray Scale	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	В0	В1	B2	В3	B4	B5	В6	В7	B8	В9
	Black		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	_	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
l a	Green		0	0	0_	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
[3]	Cyan	_	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Basic Color	Red		1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B	Magenta	-	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Ш	Yellow		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ı	1	0	0	0	0	0	0	0	0	0	0
	White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
اچا	Û	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Re	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
le of	Û	→					,	ļ									ļ										,	l				
Sca	Û	+					,	l									1	ļ.									,	<u>ا</u>				
Gray Scale of Red	Brighter	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Û	GS 1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS 1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ន្ទ	Û	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gre	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Jo e	Û	→					,	Į									,	ļ									,	l				
Gray Scale of Green	Û	→						Ļ									ļ	l										<u>ا</u>				
ay S	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
ū	Û	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	G\$1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ا به ا	Û	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Blu	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Û	↓					,	↓										l									,	l				
Scal	Û	\					、	↓_									`	L										l				
ray	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
Ū	Û	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

^{0:} Low level voltage,

Each basic color can be displayed in 1024 gray scales from 10 bits data signals. According to the combination of total 30 bits data signals, about the 1073 million-color display can be achieved on the screen

^{1:} High level voltage.



9. Optical characteristics

 $Ta=25^{\circ}C$, Vcc = 12.0V, $V_{INV1} = 24.0V$, 120Hz-mode, $V_{INV2} = 12.0V$

Parai	neter	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark	
Viewing angle	Horizontal	θ 21 θ 22	CR≧10	80	88	-	Deg.	DV 4 1 43	
range	Vertical	θ 11 θ 12	CR≦ IU	80	88	-	Deg.	[Note1,4]	
Contra	st ratio	CRn		1500	2000	-		[Note2,4] OFL1,2=100%	
Respon	se time	τ DRV			4		ms	[Note3,4,5] OFL1,2=100%	
T	Luminance of white			0.254	0.284	0.314	-		
Lumnanc	e or white	у		0.266	0.296	0.326	-	·	
Tuminan	ice of red	х		0.616	0.646	0.676	-		
Lumman	ice of red	у	θ =0 deg.	0.307	0.337	0.367	-	[Note 4] OFL1,2=100%	
Luminana	e of green	Х		0.251	0.281	0.311	-		
Lummanc	e of green	у		0.577	0.607	0.637	-		
Turninga	T			0.113	0.143	0.173	-		
Luminance of blue		у	y		0.071	0.101	-		
Luminanc	e of white	Y _{Ll}		360	450		cd/m ²	OFL1,2=100% [Note 4]	
Luminance	uniformity	δw		-	-	1.4		[Note 6]	

Measurement condition : Set the value of V_{BRT} to maximum luminance of white.

[Note] The optical characteristics are measured using the following equipment.

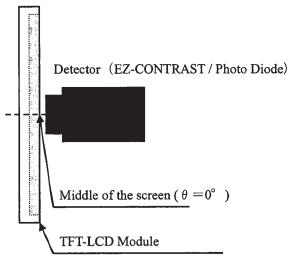


Fig.4-1 Measurement of viewing angle range and response time.

(Viewing angle range : EZ-CONTRAST

Response time: Photo Diode)

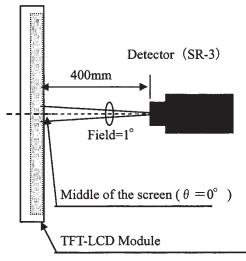


Fig.4-2 Measurement of Contrast, Luminance, Chromaticity .

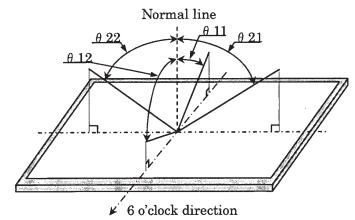
^{*}The measurement shall be executed 120 minutes after lighting at rating.

 $M \sim M + N$

LD-K21207-20

[Note 1]Definitions of viewing angle range :

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[Note 2]Definition of contrast ratio:

The contrast ratio is defined as the following.

[Note 3]Definition of response time

3-1. Response time

The response time (τ_{Drv}) is defined as the following figure and shall be measured by switching the input signal for "five luminance ratio(0%, 25%, 50%, 75%, 100%)" and "five luminance ratio(0%, 25%, 50%, 75%, 100%)".

	0%	25%	50%	75%	100%
0%		tr:0%-25%	tr:0%-50%	tr:0%-75%	tr:0%-100%
25%	td:25%-0%		tr:25%-50%	tr:25%-75%	tr:25%-100%
50%	td:50%-0%	td:50%-25%		tr:50%-75%	tr:50%-100%
75%	td:75%-0%	td:75%-25%	td:75%-50%		tr:75%-100%
100%	td:100%-0%	td:100%-25%	td:100%-50%	td:100%-75%	

t*:x-y...response time from level of gray(x) to level of gray(y)

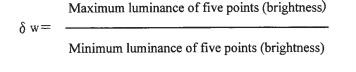
$$\tau_{Drv} = \Sigma(t^*:x-y)/20$$

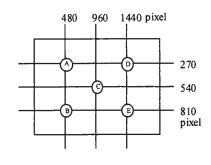
[Note 4] This shall be measured at center of the screen.

[Note 5] Response time is the value when O/S driving is used at typical input time value .

[Note 6] Definition of white uniformity;

White uniformity is defined as the following with five measurements. (A \sim E)





10. Handling Precautions of the module

- a) Be sure to turn off the power supply when inserting or disconnecting the cable.
- b) This product is using the parts (inverter, CCFT etc), which generate the high voltage. Therefore, during operating, please don't touch these parts.
- c) Brightness control voltage is switched for "ON" and "OFF", as shown in Fig.5. Voltage difference generated by this switching, Δ VINV, may affect a sound output, etc. when the power supply is shared between the inverter and its surrounding circuit. So, separate the power supply of the inverter circuit with the one of its surrounding circuit.

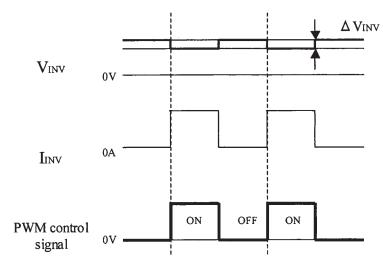


Fig.5 Brightness control voltage.

- d) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.
- e) Since the front polarizer is easily damaged, pay attention not to scratch it.
- f) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
- g) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- h) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
- Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.
- j) The module has some printed circuit boards (PCBs) on the back side, take care to keep them form any stress or pressure when handling or installing the module; otherwise some of electronic parts on the PCBs may be damaged.
- k) Observe all other precautionary requirements in handling components.
- When some pressure is added onto the module from rear side constantly, it causes display non-uniformity issue, functional defect, etc. So, please avoid such design.
- m) When giving a touch to the panel at power on supply, it may cause some kinds of degradation. In that case, once turn off the power supply, and turn on after several seconds again, and that is disappear.
- n) When handling LCD modules and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the LCD modules.



- Lamps of the backlight are placed horizontally to the long side of LCD module. So make sure that the LCD
 module are placed horizontally (landscape position), as lifetime of backlight becomes shorter if placed at
 atilt.
- p) Make sure that the LCD module is operated within specified temperature and humidity. Measures against dust, water, vibration, and heat radiation, etc. are required at the cabinet or equipment side. And image retention may occur if same fixed pattern is displayed for a long time. In some cases, it may not disappear.

Please consider the design and operating environment

11. Packing form

- a) Piling number of cartons: 2 maximum (Don't load on top of anything if the carton is not filled with full modules)
- b) Packing quantity in one carton: 4 pcs.
- c) Carton size: 1620 (W) \times 600 (D) \times 1078 (H)
- d) Total mass of one carton filled with full modules: 148kg(typ)
- e) Packing Form are shown in Fig 6.

12. Reliability test item

Ittiai	omly test item						
No.	Test item	Condition					
1	High temperature storage test	Ta=60°C 240h					
2	Low temperature storage test	Ta=-25℃ 240h					
3	High temperature and high humidity operation test	Ta=40°C; 95%RH 240h (No condensation)					
4	High temperature operation test	Ta=50°C 240h					
5	Low temperature operation test	Ta=0°C 240h					
6	Vibration test (non-operation)	Frequency: 10~57Hz/Vibration width (one side): 0.075mm : 57~500Hz/Acceleration: 9.8 m/s ² Sweep time: 11 minutes Test period: 3 hours (1h for each direction of X, Y, Z)					
7	Shock test (non-operation)	Maximum acceleration: 294m/s ² Pulse width: 11ms, sinusoidal half wave Direction: +/-X, +/-Y, +/-Z, once for each direction.					
8	ESD	At the following conditions, it is a thing without incorrect operation and destruction. (1)Non-operation: Contact electric discharge +/-10kV Non-contact electric discharge+/-20kV (2)Operation Contact electric discharge +/-8kV Non-contact electric discharge +/-15kV Conditions: 150pF、330ohm					

[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

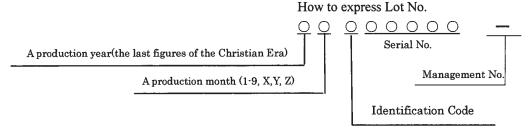


13. Others

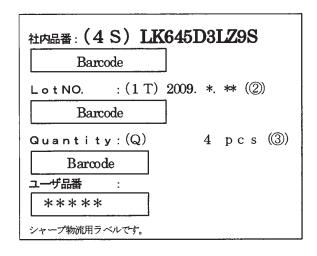
1)Lot No. Label;

The label that displays SHARP, product model (LK645D3LZ9S), a product number is stuck on the back of the module.





2) Packing Label



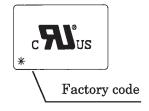
- ① Management No. (LK645D3LZ9S)
- ② Lot No. (Date)
- ③ Quantity

- 3) Adjusting volume have been set optimally before shipment, so do not change any adjusted value. If adjusted value is changed, the specification may not be satisfied.
- 4) Disassembling the module can cause permanent damage and should be strictly avoided.
- 5) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
- 6) The chemical compound, which causes the destruction of ozone layer, is not being used.
- 7) Cold cathode fluorescent lamp in LCD PANEL contains a small amount of mercury. Please follow local ordinances or regulations for disposal. It is displaying the label in the module back.

COLD CATHODE FLUORESCENT LAMP IN LCD PANEL CONTAINS A SMALL AMOUNT OF MERCURY, PLEASE FOLLOW LOCAL ORDINANCES OR REGULATION FOR DISPOSAL 当該液晶ディスプレイパネルは蛍光管が組み込まれていますので、地方自冶体の条例、または、規則に従って廃棄ください。



8) This LCD is appropriate to UL. Below figure shows the UL label.



- 9) This module is corresponded to RoHS
- 10) The chemical compound, which causes the destruction of ozone layer, is not being used.
- 11) Rust on the module is not taken up a problem.
- 12) Appearance quality and standard are referred to the outgoing incoming inspections.
- 13) Rust on the module is not taken up a problem.

14. Carton storage condition

Temperature

0°C to 40°C

Humidity

95%RH or less

Reference condition : 20°C to 35°C, 85%RH or less (summer)

: 5°C to 15°C, 85%RH or less (winter)

• the total storage time (40°C,95%RH): 240h or less

Sunlight

Be sure to shelter a product from the direct sunlight.

Atmosphere

Harmful gas, such as acid and alkali which bites electronic components and/or

wires must not be detected.

Notes

Be sure to put cartons on palette or base, don't put it on floor, and store them with

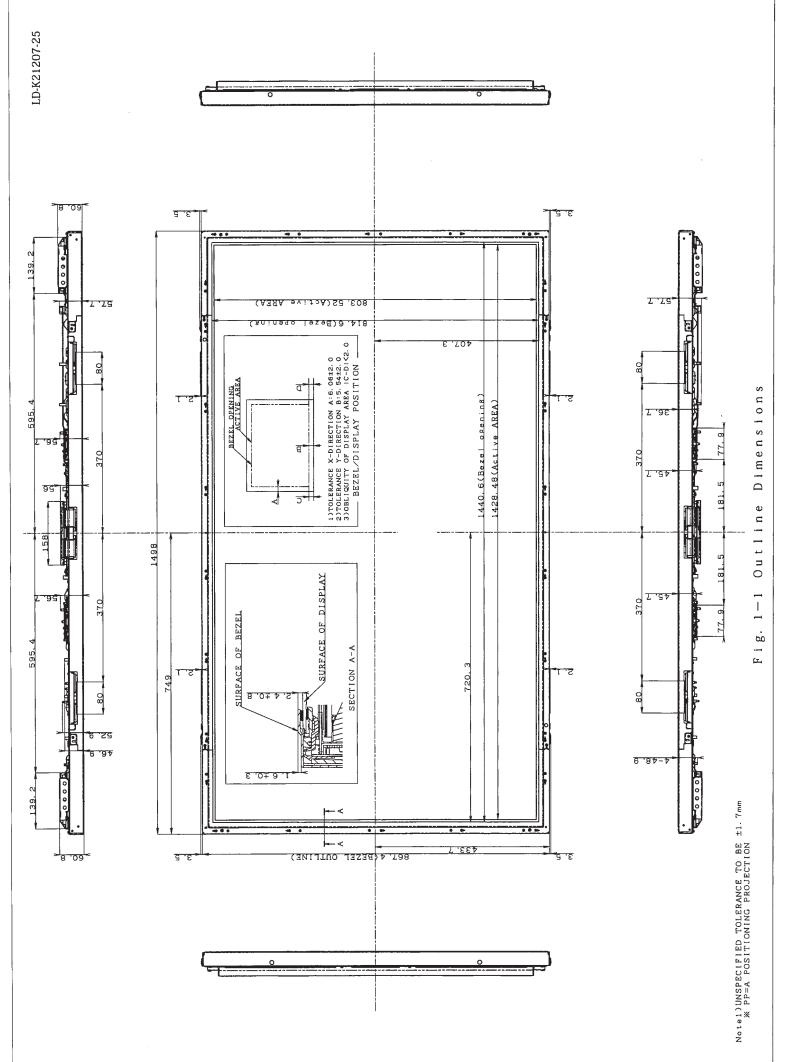
removing from wall

Please take care of ventilation in storehouse and around cartons, and control

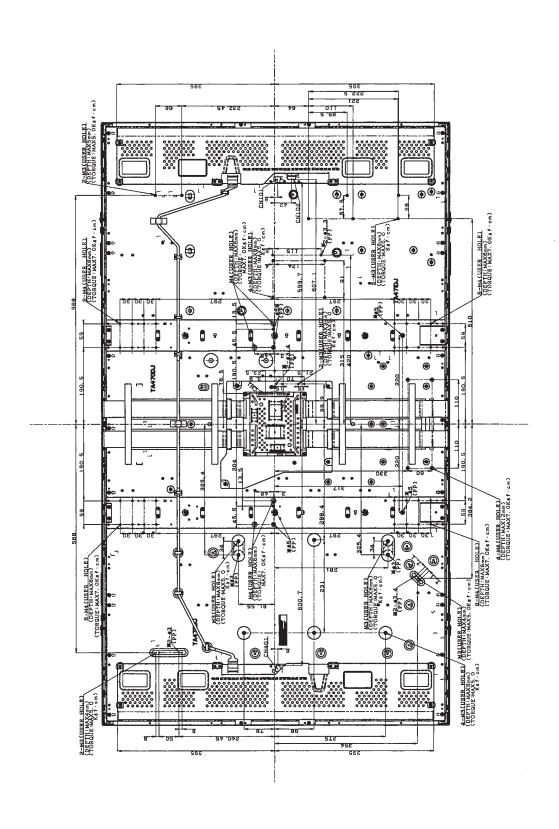
changing temperature is within limits of natural environment

Storage life

1 year



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Dimensions Fig. 1-2 Outline

Notel)UNSPECIFIED TOLERANCE TO BE ±1.7mm ** PP=A POSITIONING PROJECTION

LD-K21206-27

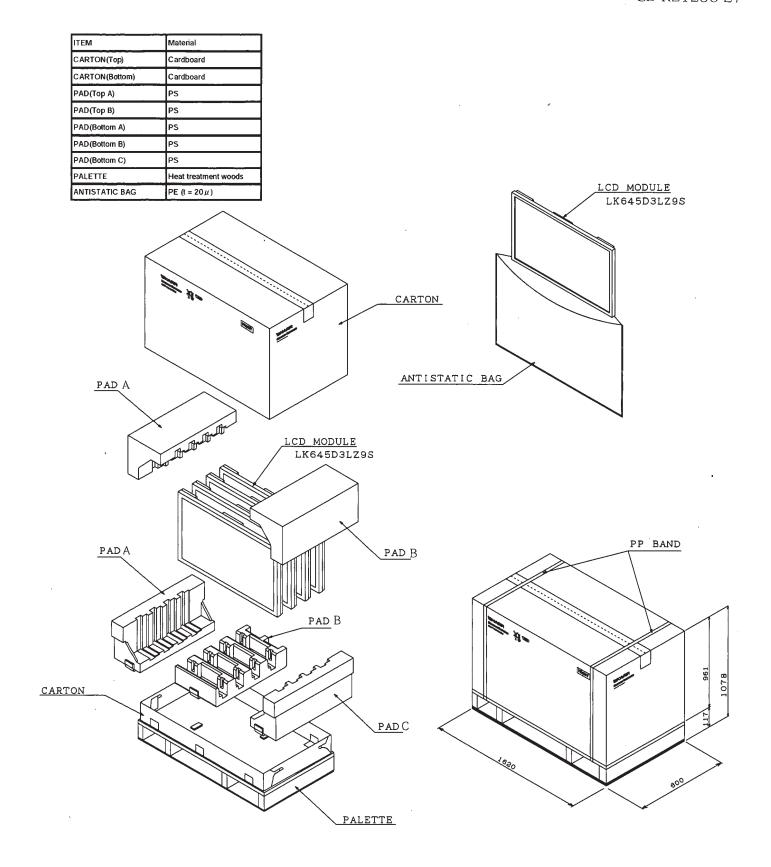


Fig. 6 Packing Form