PREPARED BY: DATE	SHARP	SPEC No.: LD-K23730
		FILE No.:
APPROVED BY: DATE		ISSUE: Aug. 8, 2011
		PAGE:20 pages

LIQUID CRYSTAL DISPLAY DIVISION
LARGE LIQUID CRYSTAL DISPLAY BUSSINESS GROUP
SHARP CORPORATION

SPECIFICATION

DEVICE SPECIFICATION FOR

TFT-LCD Module

Model No. LK695D3LA08

CUSTOMER'S APPROVAL

DATE

PRESENTED

BY ______________________

BY K. Tanaka

K.Tanaka
General Manager
DEVELOPMENT DEPT.3
LIQUID CRYSTAL DISPLAY DIVISION
LARGE LIQUID CRYSTAL DISPLAY BUSSINESS GROUP
SHARP CORPORATION

RECORDS OF REVISION

MODEL No. : LK695D3LA08

TL No. : LD-K23730

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-K23730	2011.8.8	-	-	-	1st ISSUE

1. Application

This specification applies to the color 69.5" TFT-LCD Module LK695D3LA08.

* This specification is proprietary products of SHARP CORPORATION ("SHARP") and includes materials protected under copyright of SHARP. Do not reproduce or cause any third party to reproduce them in any form or by any means, electronic or mechanical, for any purpose, in whole or in part, without the express written permission of SHARP.

* In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

* Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

* SHARP assumes no responsibility for any damage resulting from the use of the device that does not comply with the instructions and the precautions specified in these specification.

* Contact and consult with a SHARP sales representative for any questions about this device.

2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, control circuit, power supply circuit, LED drive circuit and back light system etc. Graphics and texts can be displayed on a 1920×RGBY×1080 dots panel with one billion colors by using LVDS (Low Voltage Differential Signaling) to interface, +12V of DC supply voltages.

This module includes the LED backlight system. (Typ. +183.1V of DC supply voltage)

And in order to improve the response time of LCD, this module applies the Over Shoot driving (O/S driving) technology for the control circuit .In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With this technology, image signals can be set so that liquid crystal response completes within one frame. As a result, motion blur reduces and clearer display performance can be realized.

This LCD module also adopts 120Hz Frame Rate driving method.

With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.

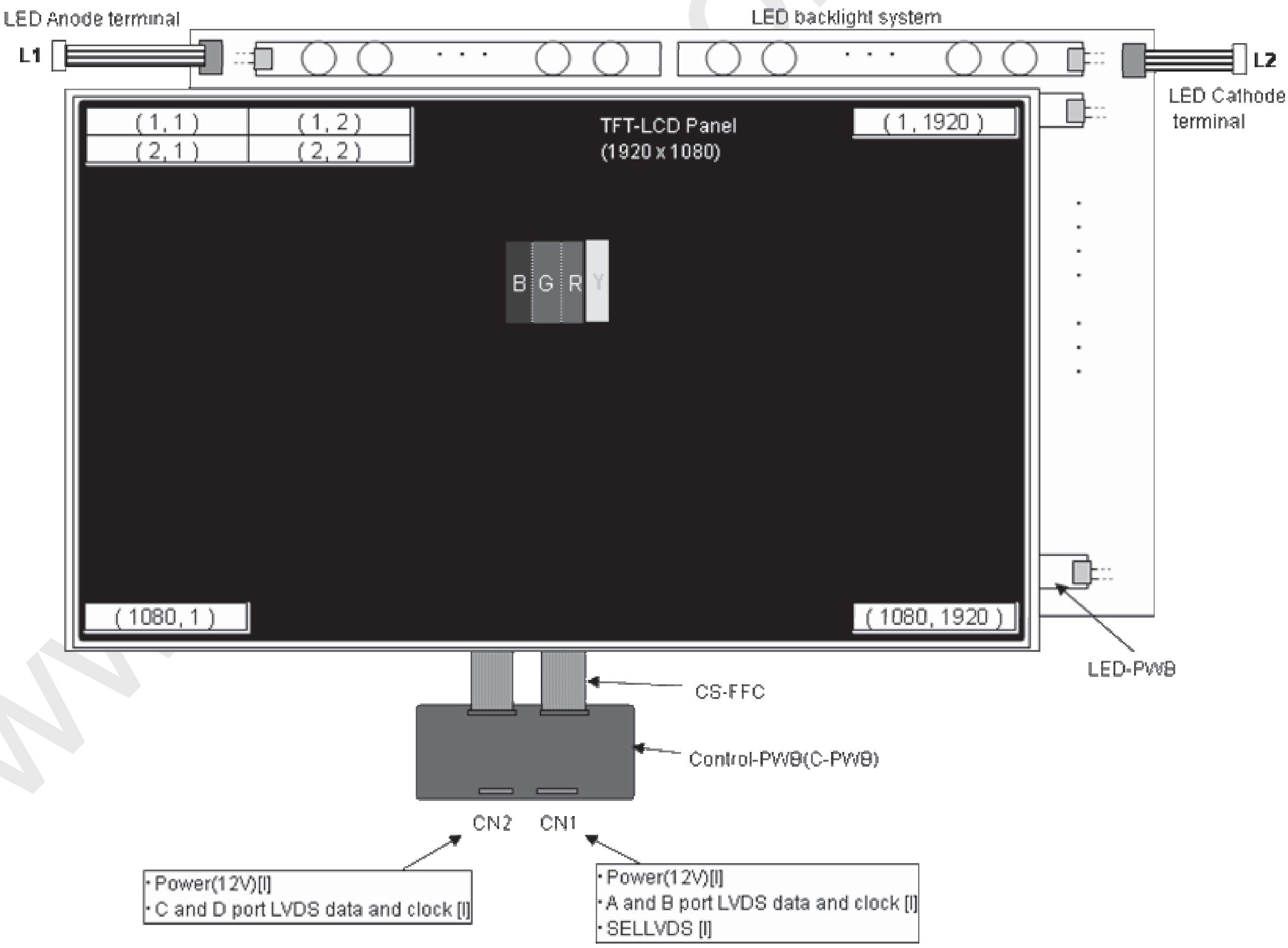
3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	176.563 (Diagonal)	cm
	69.513 (Diagonal)	inch
Active area	1538.880 (H) x 865.620 (V)	mm
Pixel Format	1920 (H) x 1080 (V) (1pixel = R + G + B +Y dot)	pixel
Pixel pitch	0.802 (H) x 0.802 (V)	mm
Pixel configuration	R, G, B, Y vertical stripe	
Display mode	Normally black	
Open Cell Outline Dimensions	1593.4(H) x 924.2(V) x 33.9(D)	mm
Mass	28.5±0.5	kg
Surface treatment	Low-Haze Anti glare Hard coating: 2H and more	

(*1) Outline dimensions are shown in p.19 (excluding protruding portion)

4. Input Terminals

4.1. Interface and block diagram



4.2. TFT panel driving

CN1 (Interface signals and +12V DC power supply)

Using connector : 91213-0510Y (ACES)

Mating connector : 91214-05130 (ACES), FI-RNE51HL/FI-RNE51CL(JAE)

Mating LVDS transmitter : THC63LVD1023 or equivalent device

Pin No.	Symbol	Function	Remark
1	GND		
2	Reserved	It is required to set non-connection(OPEN)	
3	Reserved	It is required to set non-connection(OPEN)	
4	Reserved	It is required to set non-connection(OPEN)	
5	FRAME	Frame frequency setting H:120Hz L: 100Hz	Pull down: (GND) [Note2]
6	Reserved	It is required to set non-connection(OPEN)	
7	SELLVDS	Select LVDS data order [Note3]	Pull down: (GND) [Note2]
8	Reserved	It is required to set non-connection(OPEN)	
9	Reserved	It is required to set non-connection(OPEN)	
10	Reserved	It is required to set non-connection(OPEN)	
11	GND		
12	AIN0-	Aport (-)LVDS CH0 differential data input	
13	AIN0+	Aport (+)LVDS CH0 differential data input	
14	AIN1-	Aport (-)LVDS CH1 differential data input	
15	AIN1+	Aport (+)LVDS CH1 differential data input	
16	AIN2-	Aport (-)LVDS CH2 differential data input	
17	AIN2+	Aport (+)LVDS CH2 differential data input	
18	GND		
19	ACK-	Aport LVDS Clock signal(-)	
20	ACK+	Aport LVDS Clock signal(+)	
21	GND		
22	AIN3-	Aport (-)LVDS CH3 differential data input	
23	AIN3+	Aport (+)LVDS CH3 differential data input	
24	AIN4-	Aport (-)LVDS CH4 differential data input	
25	AIN4+	Aport (+)LVDS CH4 differential data input	
26	GND		
27	GND		
28	BIN0-	Bport (-)LVDS CH0 differential data input	
29	BIN0+	Bport (+)LVDS CH0 differential data input	
30	BIN1-	Bport (-)LVDS CH1 differential data input	
31	BIN1+	Bport (+)LVDS CH1 differential data input	
32	BIN2-	Bport (-)LVDS CH2 differential data input	
33	BIN2+	Bport (+)LVDS CH2 differential data input	
34	GND		
35	BCK-	Bport LVDS Clock signal(-)	
36	BCK+	Bport LVDS Clock signal(+)	
37	GND		
38	BIN3-	Bport (-)LVDS CH3 differential data input	
39	BIN3+	Bport (+)LVDS CH3 differential data input	
40	BIN4-	Bport (-)LVDS CH4 differential data input	
41	BIN4+	Bport (+)LVDS CH4 differential data input	
42	GND		
43	GND		
44	GND		
45	GND		
46	GND		
47	VCC	+12V Power Supply	
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

CN2 (Interface signals and +12V DC power supply)

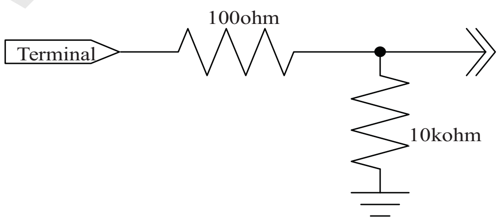
Using connector : 91213-0410Y (ACES)

Mating connector : 91214-04130 (ACES), FI-RNE41HL/FI-RNE41CL(JAE)

Pin No.	Symbol	Function	Remark
1	VCC	+12V Power Supply	
2	VCC	+12V Power Supply	
3	VCC	+12V Power Supply	
4	VCC	+12V Power Supply	
5	Reserved		
6	Reserved		
7	Reserved		
8	Reserved		
9	GND		
10	CIN0-	Cport (-)LVDS CH0 differential data input	
11	CIN0+	Cport (+)LVDS CH0 differential data input	
12	CIN1-	Cport (-)LVDS CH1 differential data input	
13	CIN1+	Cport (+)LVDS CH1 differential data input	
14	CIN2-	Cport (-)LVDS CH2 differential data input	
15	CIN2+	Cport (+)LVDS CH2 differential data input	
16	GND		
17	CCK-	Cport LVDS Clock signal(-)	
18	CCK+	Cport LVDS Clock signal(+)	
19	GND		
20	CIN3-	Cport (-)LVDS CH3 differential data input	
21	CIN3+	Cport (+)LVDS CH3 differential data input	
22	CIN4-	Cport (-)LVDS CH4 differential data input	
23	CIN4+	Cport (+)LVDS CH4 differential data input	
24	GND		
25	GND		
26	DIN0-	Dport (-)LVDS CH0 differential data input	
27	DIN0+	Dport (+)LVDS CH0 differential data input	
28	DIN1-	Dport (-)LVDS CH1 differential data input	
29	DIN1+	Dport (+)LVDS CH1 differential data input	
30	DIN2-	Dport (-)LVDS CH2 differential data input	
31	DIN2+	Dport (+)LVDS CH2 differential data input	
32	GND		
33	DCK-	Dport LVDS Clock signal(-)	
34	DCK+	Dport LVDS Clock signal(+)	
35	GND		
36	DIN3-	Dport (-)LVDS CH3 differential data input	
37	DIN3+	Dport (+)LVDS CH3 differential data input	
38	DIN4-	Dport (-)LVDS CH4 differential data input	
39	DIN4+	Dport (+)LVDS CH4 differential data input	
40	GND		
41	GND		

[Note1] GND of a liquid crystal panel drive part has connected with a module chassis.

[Note2] The equivalent circuit figure of the terminal.



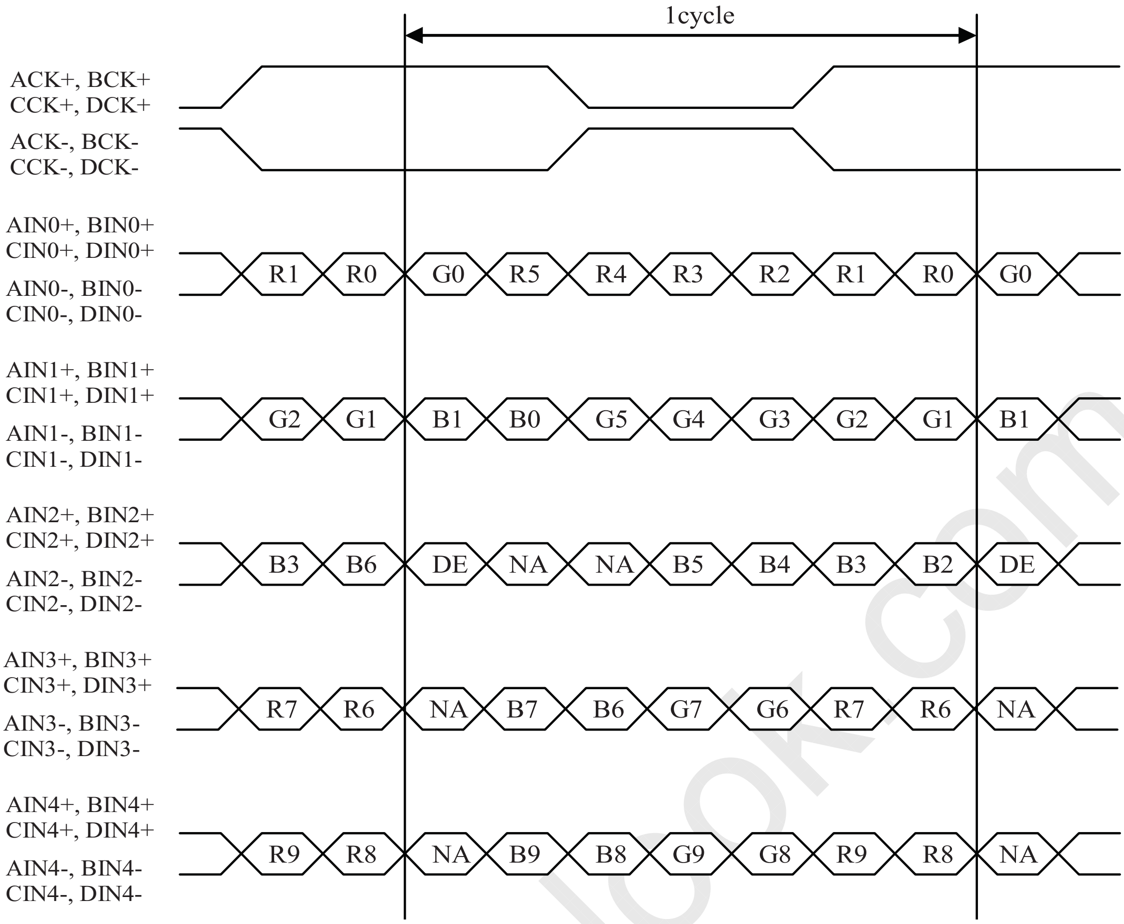
[Note3] LVDS Data order

SELLVDS		
Data	L(GND) or OPEN [VESA]	H(3.3V) [JEIDA]
TA0	R0(LSB)	R4
TA1	R1	R5
TA2	R2	R6
TA3	R3	R7
TA4	R4	R8
TA5	R5	R9(MSB)
TA6	G0(LSB)	G4
TB0	G1	G5
TB1	G2	G6
TB2	G3	G7
TB3	G4	G8
TB4	G5	G9(MSB)
TB5	B0(LSB)	B4
TB6	B1	B5
TC0	B2	B6
TC1	B3	B7
TC2	B4	B8
TC3	B5	B9(MSB)
TC4	NA	NA
TC5	NA	NA
TC6	DE(*)	DE(*)
TD0	R6	R2
TD1	R7	R3
TD2	G6	G2
TD3	G7	G3
TD4	B6	B2
TD5	B7	B3
TD6	N/A	N/A
TE0	R8	R0(LSB)
TE1	R9(MSB)	R1
TE2	G8	G0(LSB)
TE3	G9(MSB)	G1
TE4	B8	B0(LSB)
TE5	B9(MSB)	B1
TE6	N/A	N/A

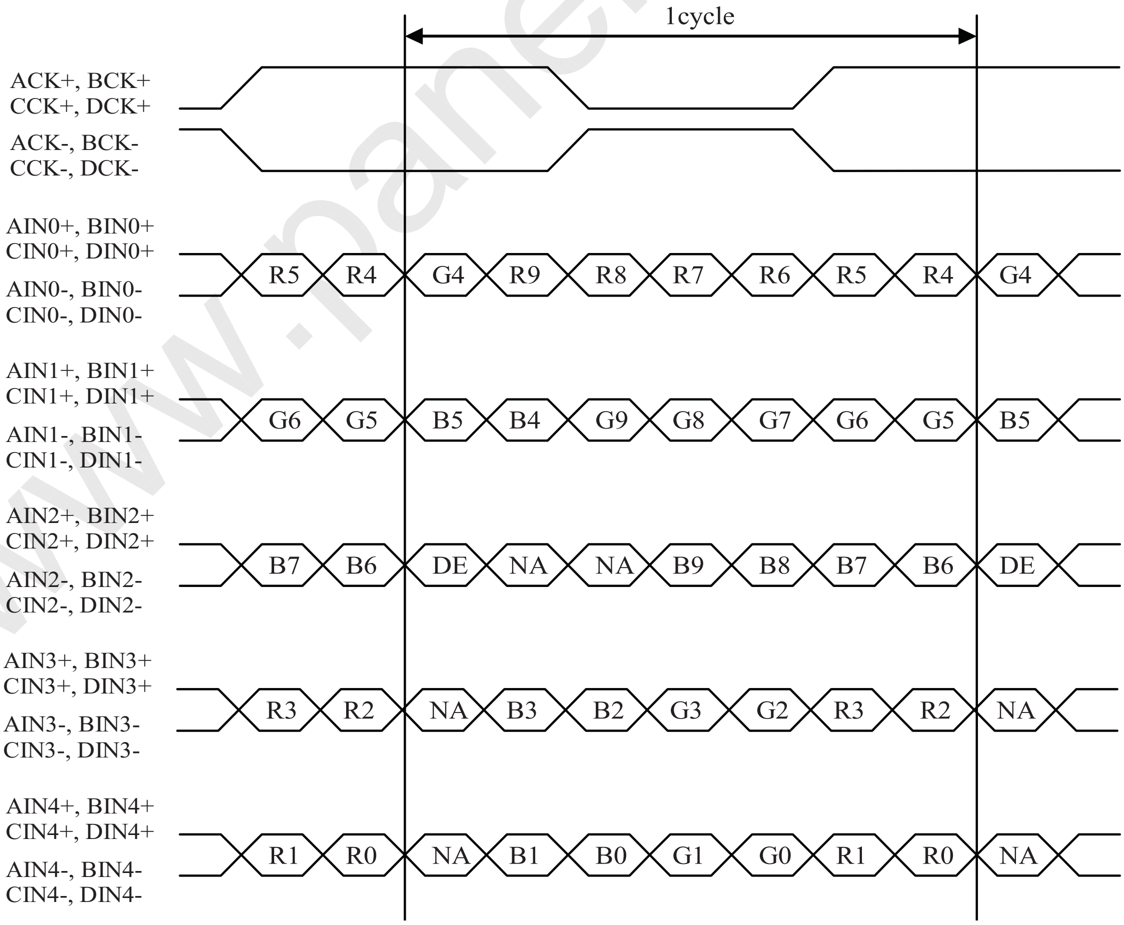
NA: Not Available
(*)Since the display position is prescribed by the rise of DE(Display Enable) signal, please do not fix DE signal during operation at ”High”.

LD-K23730-6

SELLVDS= Low (GND) or OPEN



SELLVDS= High (3.3V)



DE: Display Enable, NA: Not Available (Fixed Low)

4.3. Backlight driving

L1 Using connector: SMH200-H20S (YEON-HO)
Mating terminal: YST200-C1 (YEON-HO)

L2 Using connector: SMH200-H18S (YEON-HO)
Mating terminal: YST200-C1 (YEON-HO)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	ANODE	LED Anode terminal (DC 57mA)	1	CATHODE	GND
2	ANODE	LED Anode terminal (DC 57mA)	2	CATHODE	GND
3	ANODE	LED Anode terminal (DC 57mA)	3	CATHODE	GND
4	ANODE	LED Anode terminal (DC 57mA)	4	CATHODE	GND
5	ANODE	LED Anode terminal (DC 57mA)	5	CATHODE	GND
6	ANODE	LED Anode terminal (DC 57mA)	6	CATHODE	GND
7	ANODE	LED Anode terminal (DC 57mA)	7	CATHODE	GND
8	ANODE	LED Anode terminal (DC 57mA)	8	CATHODE	GND
9	ANODE	LED Anode terminal (DC 57mA)	9	CATHODE	GND
10	ANODE	LED Anode terminal (DC 57mA)	10	CATHODE	GND
11	ANODE	LED Anode terminal (DC 57mA)	11	CATHODE	GND
12	ANODE	LED Anode terminal (DC 57mA)	12	CATHODE	GND
13	ANODE	LED Anode terminal (DC 57mA)	13	CATHODE	GND
14	ANODE	LED Anode terminal (DC 57mA)	14	CATHODE	GND
15	NC	N.C	15	NC	N.C
16	NC	N.C	16	NC	N.C
17	NC	N.C	17	NC	N.C
18	NC	N.C	18	NC	N.C
19	NC	N.C			
20	NC	N.C			

4.4 The back light system characteristics

The characteristics of the LED are shown in the following table.The value mentioned below is at the case of One LED.

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Life time	T_{LED}	-	60,000	-	Hour	25℃ [Note.1]

[Note1] LED life time is the expectation value calculated from lifetime data of maker report. It is defined as the time when brightness becomes 50% of the original value in the continuous operation under the condition of Ta=25℃.

5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage (for C-PWB)	V_I	Ta=25°C	-0.3 ~ 3.6	V	[Note 1]
12V supply voltage (for C-PWB)	VCC	Ta=25°C	0 ~ + 14	V	
LED supply reverse voltage (for LED 1line)	V_{LED}	Ta=25 °C	150	V	
LED supply current (for LED 1line)	I_{LED}	Ta=25 °C	120	mA	
Storage temperature	Tstg	-	-25 ~ +60	°C	[Note 2]
Operation temperature (Ambient)	Topa	-	0 ~ +50	°C	

[Note 1] SELLVDS、FRAME

[Note 2] Humidity 95%RH Max.(Ta≦40°C)
Maximum wet-bulb temperature at 39 °C or less.(Ta>40°C)
No condensation.

6. Electrical Characteristics

6.1. Control circuit driving

Ta=25 °C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+12V supply voltage	Supply voltage	Vcc	11.4	12	12.6	V	[Note 1]
	Current dissipation	Icc	-	0.75	2.0	A	[Note 2]
	Inrush current	I_{RUSH}	-	4.4	5.5	A	t1=500us [Note 5]
Permissible input ripple voltage		V_{RP}	-	-	100	mV_{P-P}	Vcc = +12.0V
Differential input threshold voltage	High	V_{TH}	-	-	100	mV	V_{CM} = +1.2V [Note 4]
	Low	V_{TL}	-100	-	-	mV	
Input Low voltage		V_{IL}	0	-	1.0	V	[Note 3]
Input High voltage		V_{IH}	2.3	-	3.3	V	
Input leak current (Low)		I_{IL}	-	-	40	μA	V_I = 0V [Note 3]
Input leak current (High)		I_{IH}	-	-	400	μA	V_I = 3.3V [Note 3]
Terminal resistor		R_T	-	100	-	Ω	Differential input

[Note]V_{CM}: Common mode voltage of LVDS driver.

[Note1]

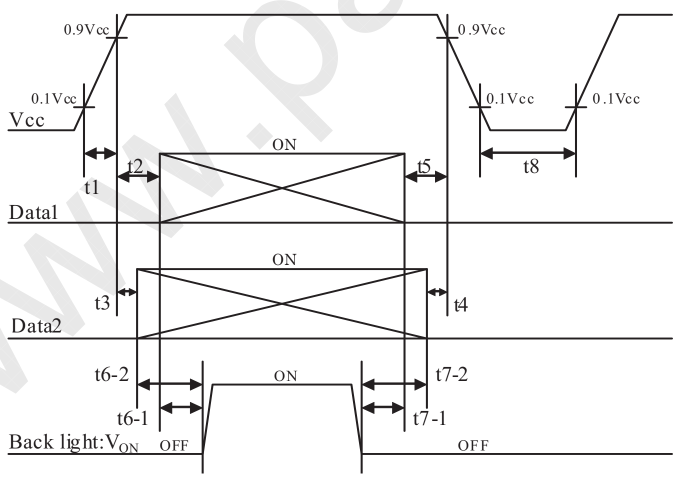
Input voltage sequences

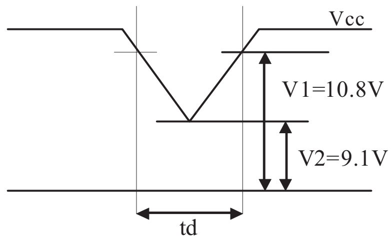
50us < t1 < 20ms
20ms < t2 < 5s
1s < t3 < 5s
0 < t4 < 1s
0 < t5 < 1s
1s < t6-1
1s < t6-2
0 < t7-1
0 < t7-2
1s < t8

Dip conditions for supply voltage

a) V2 ≦ Vcc < V1
td < 10ms

b) Vcc < V2
This case is based on input voltage sequences.





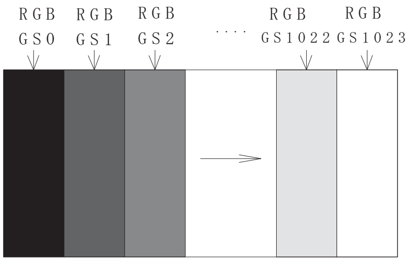
※ Data1: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±, CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±, DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±
*V_{CM} voltage pursues the sequence mentioned above

※ Data2: SELLVDS, FRAME

[Note]About the relation between data input and back light lighting, please base on the above-mentioned input sequence. When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

[Note 2] Typical current situation: 1024 gray-bar patterns. (Vcc = +12.0V)

The explanation of RGB gray scale is seen in section 8.

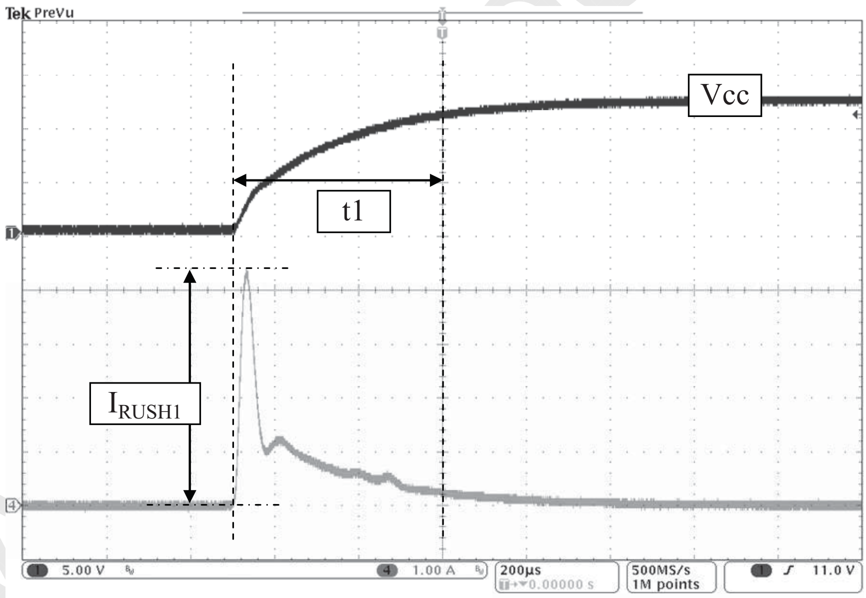


Vcc=+12.0V
CK=74.25MHz
Th=7.41μs
TV=120Hz

[Note 3] SELLVDS, FRAME

[Note 4] ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±,BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±
CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±,DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±

[Note 5] Vcc12V inrush current waveform



6.2. LED driving for back light

The back light system is direct light type with LEDs . Ta=25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Operating Voltage	V_{LED}	174.1	183.1	192.1	V	@ I_{LED1} =57mA
LED Operating Current (LED 1line)	I_{LED1}	-	57	-	mA	per LED 1 line [Note1]
LED Operating Current (Total input/ module)	I_{LED14}	-	798	-	mA	57mA× LED 14 lines [None2]

[None1] Pin1, Pin2,Pin3, …, Pin14 (L1 terminal)

I_{LED1} is a current per LED 1 line between L1 anode and L2 cathode.

*Please decrease LED heat enough when the LED current is increased more than TYP value.

Please keep 85℃ or less the temperature of the terminal of LED.

[Note2] V_{LED} is a potential difference between the anode and the cathode of each LED PWB.

Ta = 25℃, Measurement after 100ms has passed since power supply was turned on.

*The products are sensitive to the static electricity and care shall be fully taken when handling the products. Particularly in case that an over-voltage which exceeds the Absolute Maximum Rating of the products shall be applied, the overflowed energy may cause damages to, or possibly result in destruction of the products. Please take absolutely secured countermeasures against static electricity and surge when handling the products.

7. Timing characteristics of input signals

7.1. Timing characteristics

Timing diagrams of input signal are shown in Fig.2.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Clock	Frequency	1/Tc	69.0	74.25	80.0	MHz	
Data enable signal	Horizontal period	TH	525	550	650	clock	
			7.1	7.41	8.0	μs	
	Horizontal period (High)	THd	480	480	480	clock	
	Vertical period	TV	1110	1125	1400	line	
			94	120	122	Hz	
	Vertical period (High)	TVd	1080	1080	1080	line	

[Note]-When vertical period is very long, flicker and etc. may occur.

-Please turn off the module after it shows the black screen.

-Please make sure that length of vertical period should become of an integral multiple of horizontal length of period. Otherwise, the screen may not display properly.

-As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.

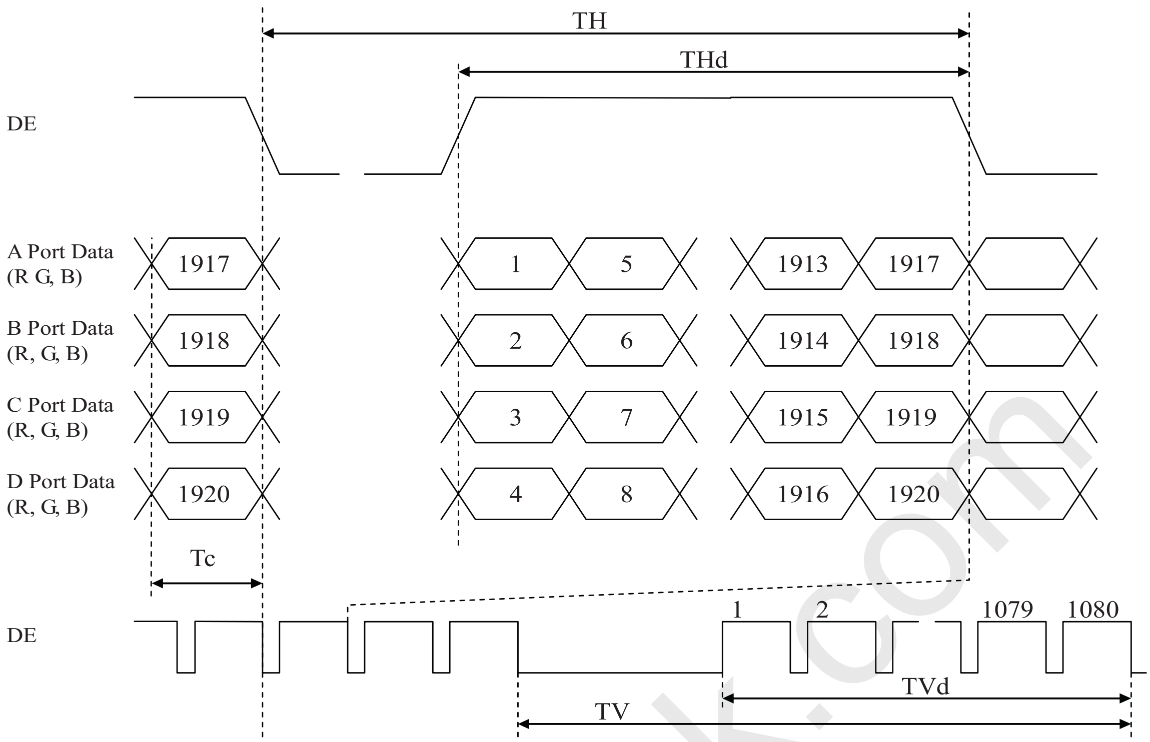
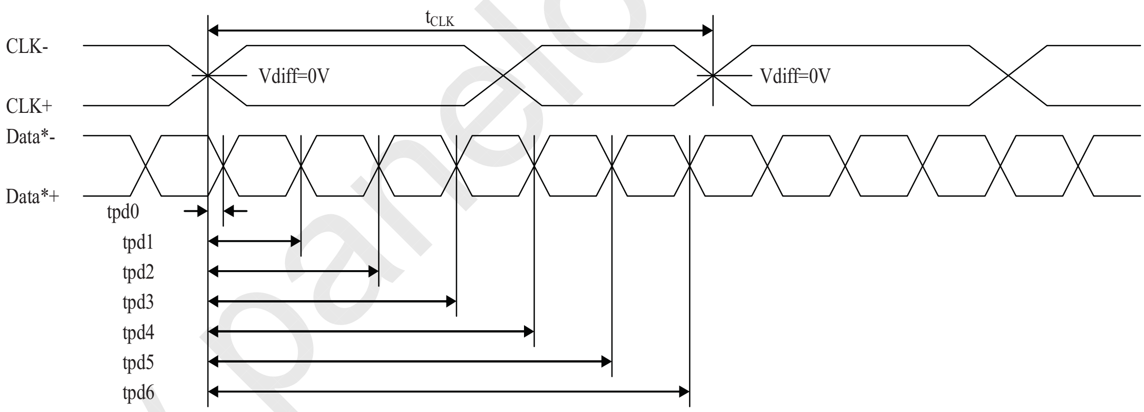


Fig.2 Timing diagram of input signal

7.2. LVDS signal characteristics



Item		Symbol	Min.	Typ.	Max.	Unit
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	-0.25	0	0.25	ns
	Delay time, CLK rising edge to serial bit position 1	tpd1	$1*t_{CLK}/7-0.25$	$1*t_{CLK}/7$	$1*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 2	tpd2	$2*t_{CLK}/7-0.25$	$2*t_{CLK}/7$	$2*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 3	tpd3	$3*t_{CLK}/7-0.25$	$3*t_{CLK}/7$	$3*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 4	tpd4	$4*t_{CLK}/7-0.25$	$4*t_{CLK}/7$	$4*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 5	tpd5	$5*t_{CLK}/7-0.25$	$5*t_{CLK}/7$	$5*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 6	tpd6	$6*t_{CLK}7-0.25$	$6*t_{CLK}/7$	$6*t_{CLK}/7+0.25$	

8. Input signal, basic display colors and gray scale of each color

Colors & Gray Scale			Data signal																													
			R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	---	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	GS1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	---	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
	---	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

- 0: Low level voltage / 1: High level voltage
- Each basic color can be displayed in 1024 gray scales from 10 bits data signals. According to the combination of total 30 bits data signals, one billion-color display can be achieved on the screen.

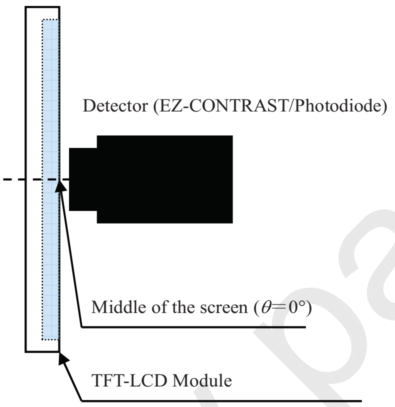
9. Optical characteristics

Ta=25°C, Vcc=12.V, VLED =+183.1V, LED current=798mA, Timing: 120Hz (typ. value)

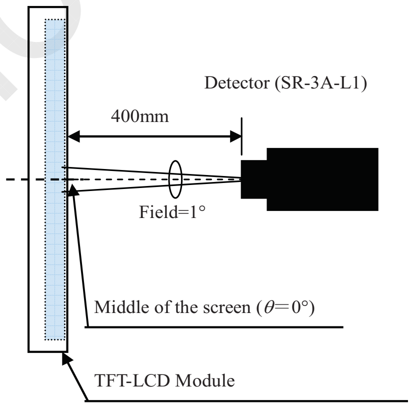
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21 θ22	CR≧10	70	88	-	Deg.	[Note1,4]
	Vertical	θ11 θ12		70	88	-	Deg.	
Contrast ratio		CRn	θ=0 deg.		5000	-	-	[Note2,4]
Response time		τrd		-	4	-	ms	[Note3,4,5]
Chromaticity	White	x		Typ.-0.03	(0.280)	Typ.+0.03	-	[Note4]
		y		Typ.-0.03	(0.290)	Typ.+0.03	-	
	Red	x		Typ.-0.03	(0.651)	Typ.+0.03	-	
		y		Typ.-0.03	(0.335)	Typ.+0.03	-	
	Green	x		Typ.-0.03	(0.283)	Typ.+0.03	-	
		y		Typ.-0.03	(0.696)	Typ.+0.03	-	
	Blue	x		Typ.-0.03	(0.152)	Typ.+0.03	-	
		y		Typ.-0.03	(0.049)	Typ.+0.03	-	
Luminance	White	Y_L		300	350	-	cd/m^2	
Luminance uniformity	White	δw		-	-	1.43		[Note6]

- Measurement condition: Set the value of backlight control voltage to maximum luminance of white.
- The measurement shall be executed 60 minutes after lighting at rating.

[Note] The optical characteristics are measured using the following equipment.

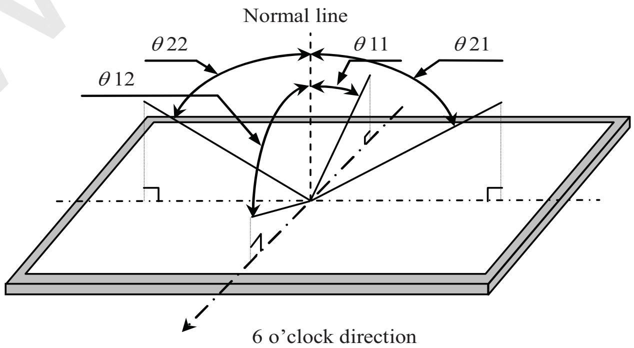


Measurement of viewing angle range and Response time.
-Viewing angle range: EZ-CONTRAST
- Response time: Photodiode



Measurement of Contrast, Luminance, Chromaticity.

[Note1] Definitions of viewing angle range:



[Note2] Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

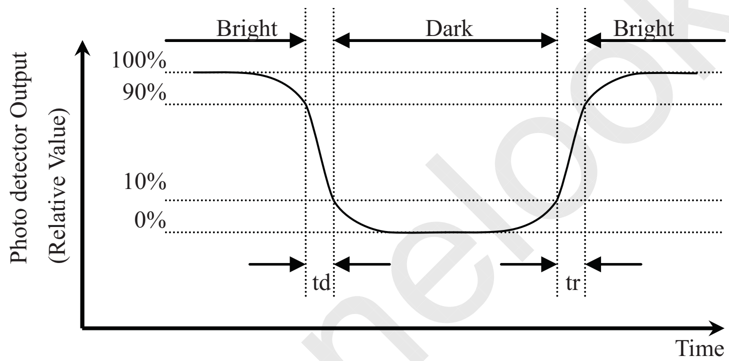
[Note3] Definition of response time

The response time (τ_{rd}) is defined as the following,

$$\tau_{rd} = \{\sum(\text{tr} : \text{x - y}) + \sum(\text{td} : \text{x - y})\}/20$$

τ_{rd} is the average value of the switching time from five gray levels (0%, 25%, 50%, 75% and 100%) to five gray levels (0%, 25%, 50%, 75% and 100%).

		Gray level of End (y)				
		0%	25%	50%	75%	100%
Gray level of Start (x)	0%		tr: 0%-25%	tr: 0%-50%	tr: 0%-75%	tr: 0%-100%
	25%	td: 25%-0%		tr: 25%-50%	tr: 25%-75%	tr: 25%-100%
	50%	td: 50%-0%	td: 50%-25%		tr: 50%-75%	tr: 50%-100%
	75%	td: 75%-0%	td: 75%-25%	td: 75%-50%		tr: 75%-100%
	100%	td: 100%-0%	td: 100%-25%	td: 100%-50%	td: 100%-75%	



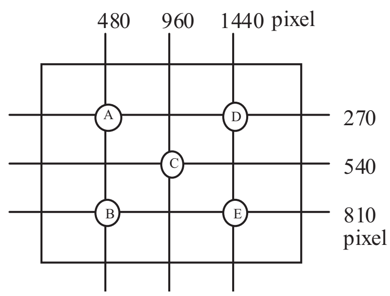
[Note4] This value shall be measured at center of the screen.

[Note5] This value is valid when O/S driving is used at typical input time value.

[Note6] Definition of white uniformity ;

White uniformity is defined as the following with five measurements. (A~E)

$$\delta_W = \frac{\text{Maximum luminance of five points (brightness)}}{\text{Minimum luminance of five points (brightness)}}$$



10. Reliability test item

No.	Test item	Condition
1	High temperature storage test	Ta=60°C 240h
2	Low temperature storage test	Ta=-25°C 240h
3	High temperature and high humidity operation test	Ta=40°C ; 95%RH 240h (No condensation)
4	High temperature operation test	Ta=50°C 240h
5	Low temperature operation test	Ta=0°C 240h
6	Vibration test (non-operation)	Frequency: 10~57Hz/Vibration width (one side): 0.075mm : 58~500Hz/Acceleration: 9.8 m/s^2 Sweep time: 11 minutes Test period: 3 hours (1h for each direction of X, Y, Z)
7	Shock test (non-operation)	Maximum acceleration: $294 m/s^2$ Pulse width: 11ms, sinusoidal half wave Direction: Vertical direction in the front at once.
8	ESD	* At the following conditions, it is a thing without incorrect operation and destruction. (1)Non-operation: Contact electric discharge ±10kV Non-contact electric discharge ±20kV (2)Operation Contact electric discharge ±8kV Non-contact electric discharge ±15kV Conditions: 150pF, 330ohm

[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

11. Packing form

a) Piling number of cartons : 2 Maximum
b) Packing quantity in one carton : 8pcs
c) Carton size : 1772(W)×1140(D)×1166(H)
d) Total mass of one carton filled with full modules : 300kg

12. Carton storage condition

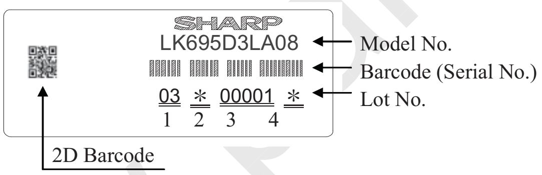
Temperature	0°C to 40°C
Humidity	95% RH or less
Reference condition	20°C to 35°C, 85% RH or less (summer) 5°C to 15°C, 85% RH or less (winter) the total storage time (40°C, 95% RH) : 240h or less
Sunlight	Be sure to shelter a production from the direct sunlight.
Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Notes	Be sure to put cartons on palette or base, don't put it on floor, and store them with removing from wall. Please take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
Storage life	1 year.

13. Label

13.1 Module Serial Label

a) Overview

This label is stuck on the backlight chassis.



b) How to express Lot No.

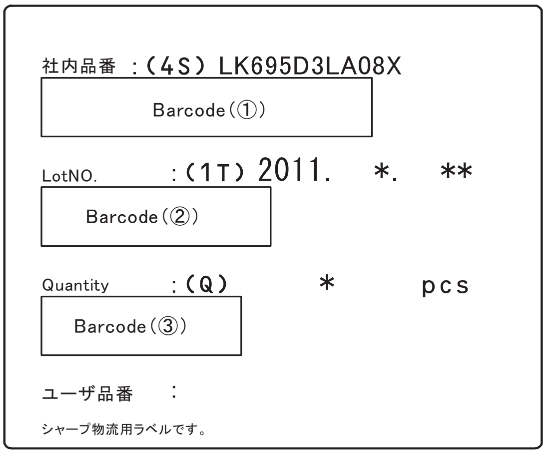
Model No.	1	2	3	4
LK695D3LA08X	(03)	N	(00001)	X

4: Suffix Code
3: Serial No.
2: Factory Code
- N: NSEC
-
1: Production Year & Month

13.2. Packing Label

This label is stuck on the each packing box.

ex) LK695D3LA08X



① Model No.& Suffix Code
② Lot No.
③ Quantity

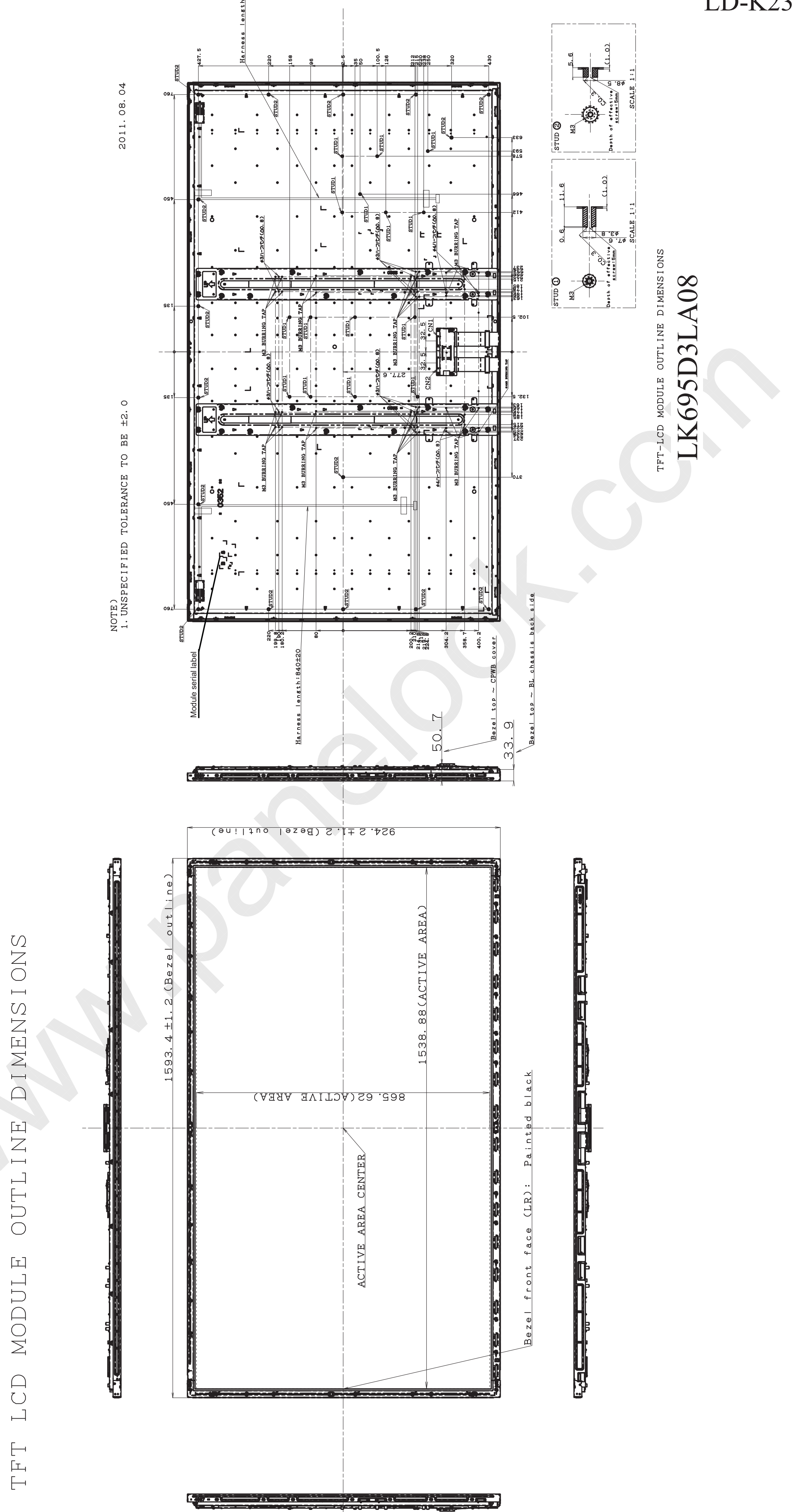
14. Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable.
b) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.
c) Since the front polarizer is easily damaged, pay attention not to scratch it.
d) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
e) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
g) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.
h) The module has some printed circuit boards (PCBs) on the back side, take care to keep them form any stress or pressure when handling or installing the module; otherwise some of electronic parts on the PCBs may be damaged.
i) Observe all other precautionary requirements in handling components.
j) When some pressure is added onto the module from rear side constantly, it causes display non-uniformity issue, functional defect, etc. So, please avoid such design.
k) When giving a touch to the panel at power on supply, it may cause some kinds of degradation. In that case, once turn off the power supply, and turn on after several seconds again, and that is disappear.
l) When handling LCD module and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the LCD modules.
m) This LCD module is designed to prevent dust from entering into it. However, there would be a possibility to have a bad effect on display performance in case of having dust inside of LCD module. Therefore, please ensure to design your TV set to keep dust away around LCD module.
n) This LCD module passes over the rust.
o) Adjusting Vcom has been set optimally before shipment, so do not change any adjusted value. If adjusted value is changed, the specification may not be satisfied.
p) Disassembling the module can cause permanent damage and should be strictly avoided.
q) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
r) The chemical compound, which causes the destruction of ozone layer, is not being used.
s) In any case, please do not resolve this LCD module

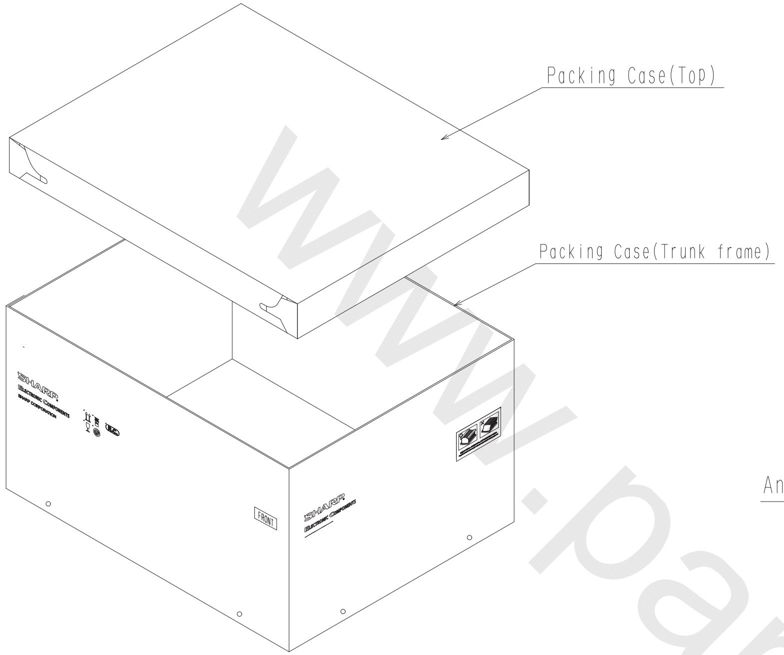
t) This module is corresponded to RoHS.

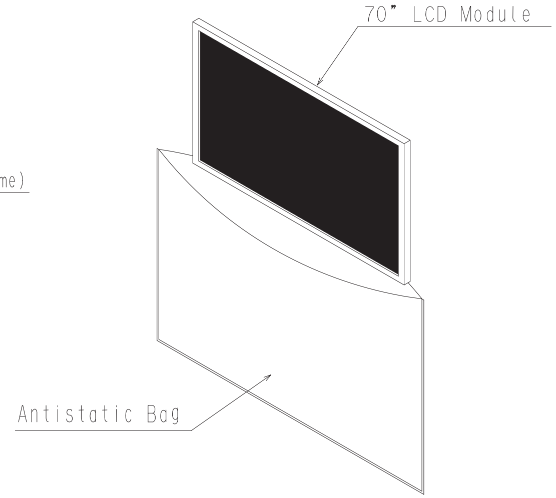
u) When any question or issue occurs, it shall be solved by mutual discussion.

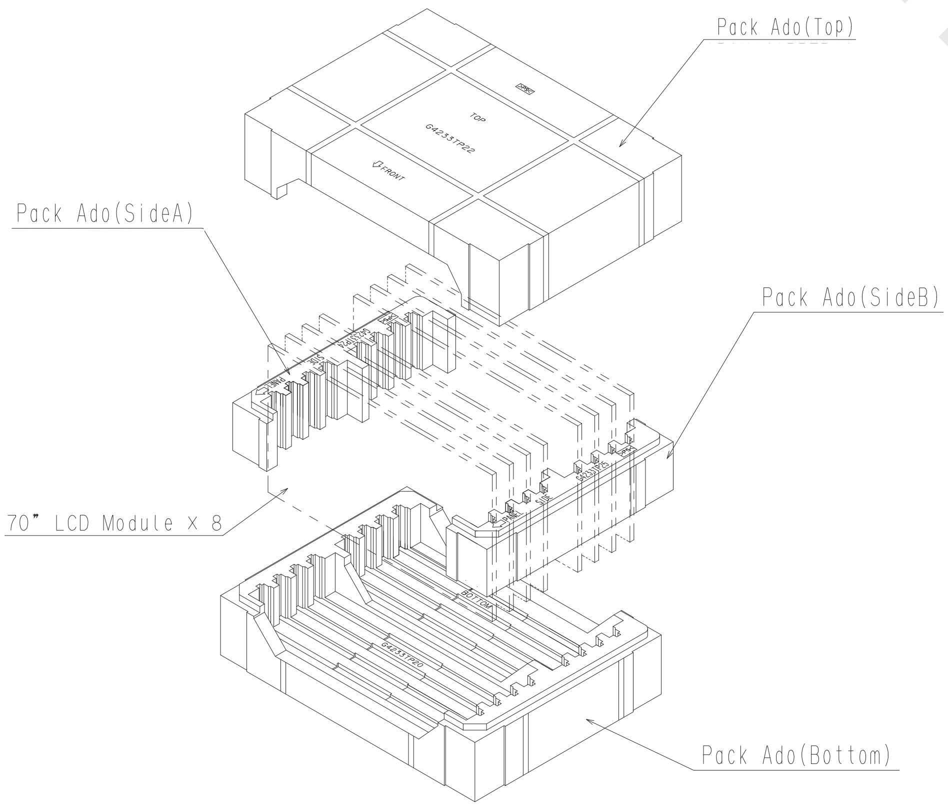
LD-K23730-19

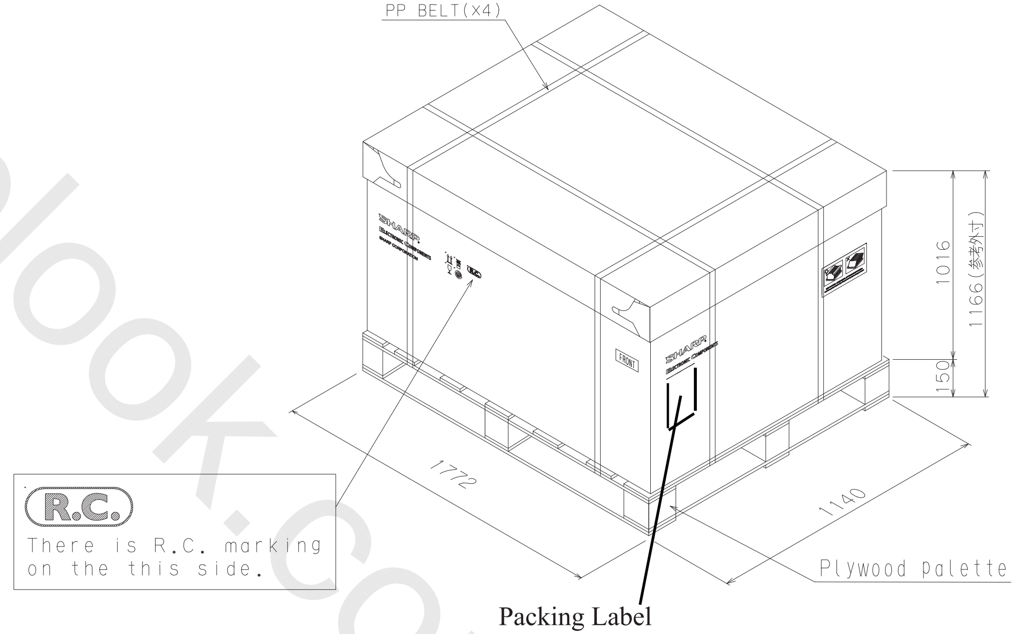

TFT LCD MODULE OUTLINE DIMENSIONS
TFT-LCD MODULE OUTLINE DIMENSIONS
LK695D3LA08
2011.08.04
NOTE)
1. UNSPECIFIED TOLERANCE TO BE ±2.0
924.2±1.2 (Bezel outline)
1593.4±1.2 (Bezel outline)
865.62 (ACTIVE AREA)
1538.88 (ACTIVE AREA)
ACTIVE AREA CENTER
Bezel front face (LR): Painted black
Module serial label
Harness length:840±20
Harness length:908±20
Bezel top ~ CPWB cover
Bezel top ~ BL chassis back side
50.7
33.9
SCALE 1:1
Depth of effective screw:5mm
CN1
CN2

Parts Name	Material
Packing Case(Top)	Cardboard
Pack Ado(Bottom)	PS
Pack Ado(Top)	PS
Pack Ado(SideA)	PS
Pack Ado(SideB)	PS
Packing Case(Trunk frame)	Cardboard
Plywood Palette	Plywoods
Antistatic Bag	PE(t=20μ)









Packing style of LK695D3LA08

LD-K23730-20