LM020L·LM020XMBL

- 16 character x 1 line
- Controller LSI HD44780 is built-in (See page 79).
- +5V single power supply
- Display color: LM020L : Gray
  LM020XMBL : New-gray

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 12T (max.) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 7 dots)	3.07W x 5.73H mm
Character pitch	3.77 mm
Dot size	0.55W x 0.75H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50 40*°C
Storage temperature (Tstg)	–20	70 60*°C

* Shows the value of type LM20XMBL.

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (V_{IH})	2.2 V min.
Input "low" voltage (V_{IL})	0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 2.0 mA max.

POWER SUPPLY FOR LCD DRIVE (Recommended) (V_{DD}-V_O)

Duty = 1/16

Range of $V_{DD}-V_O$	1.5~5.25 V
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA ..... See page 7

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7

Unit: mm

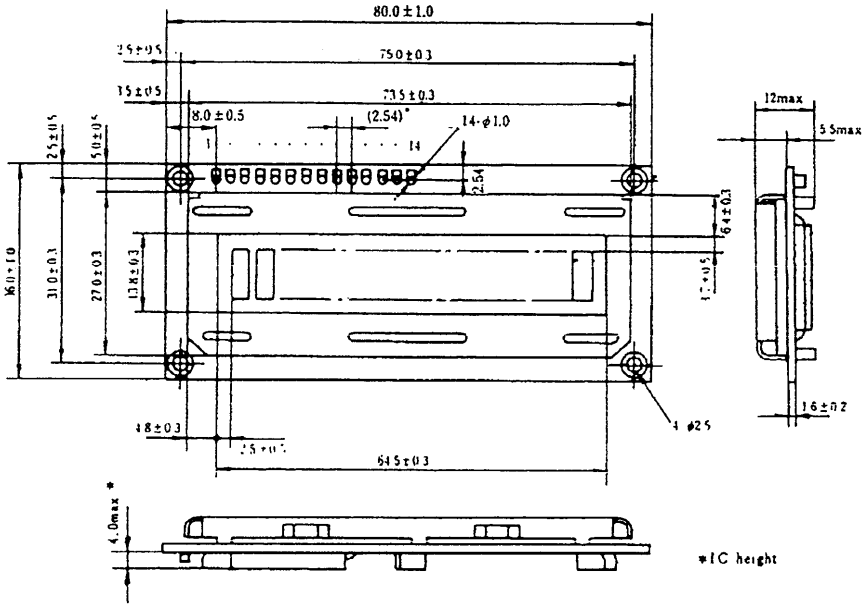


Fig. 1 External dimensions

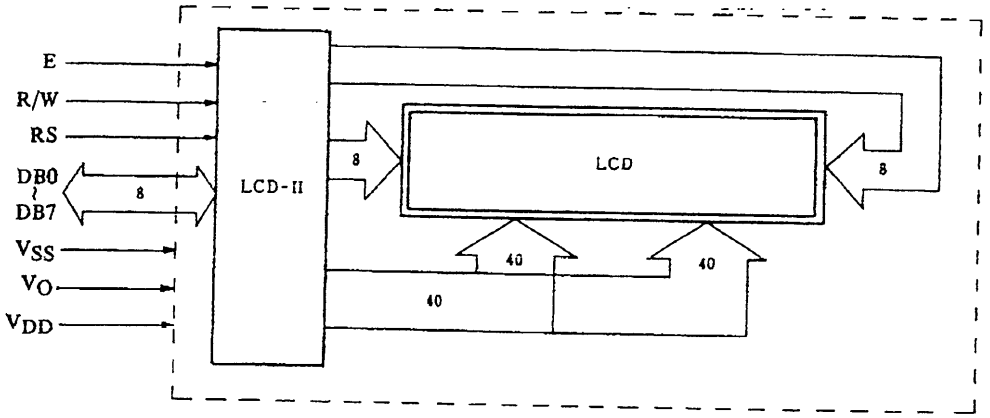


Fig. 2 Block diagram

Unit: mm

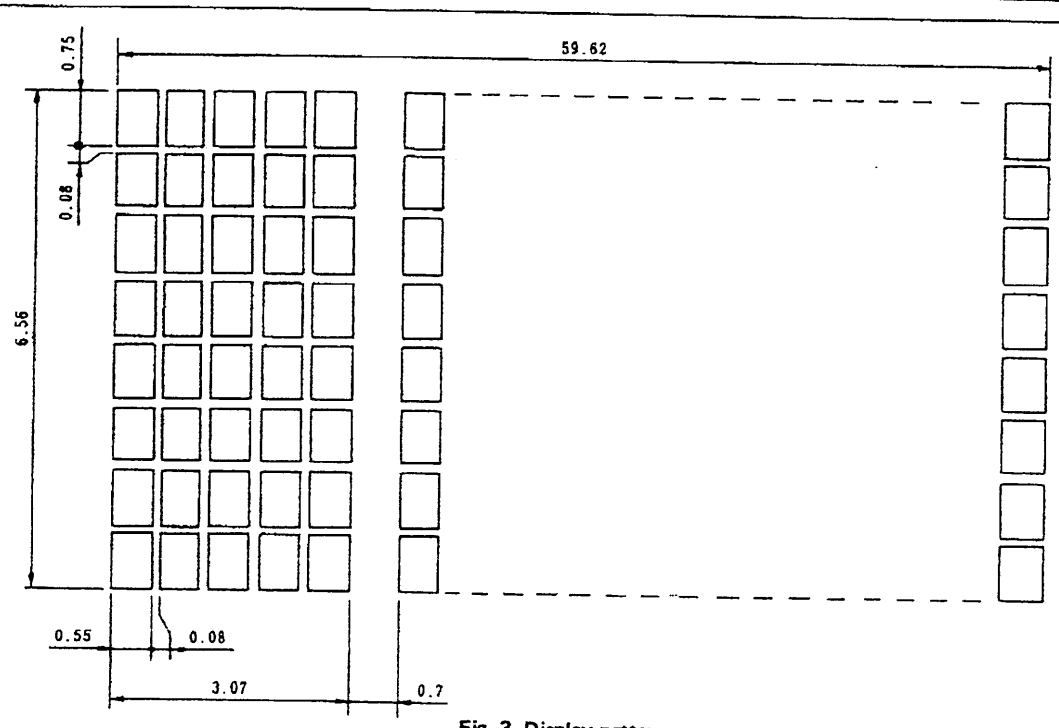


Fig. 3 Display pattern

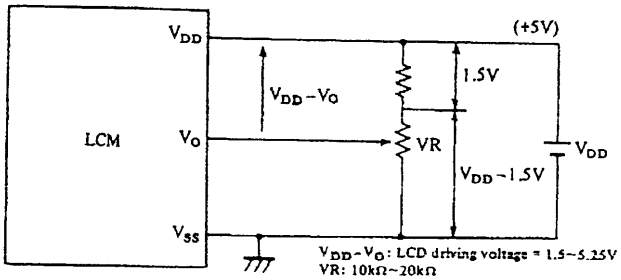


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	PW_{EH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

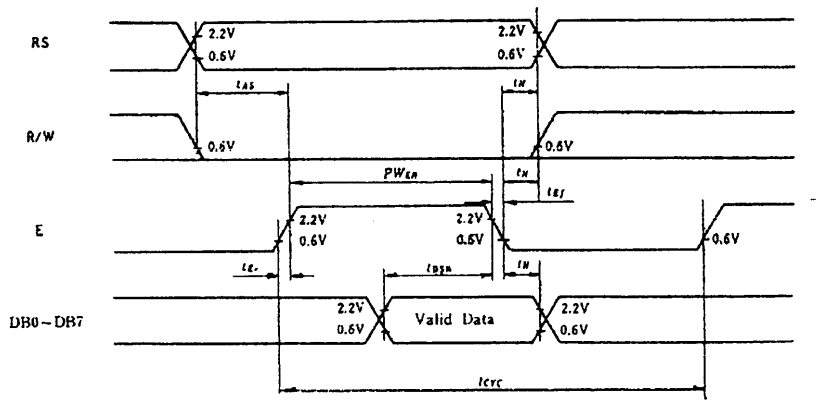


Fig. 5 Interface timing (data write)

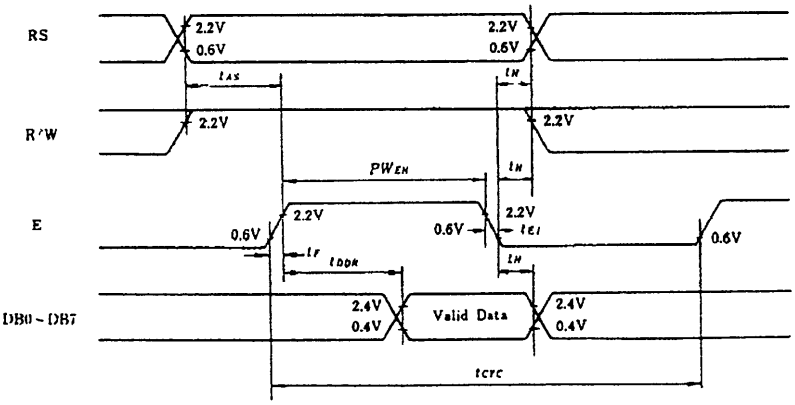


Fig. 6 Interface timing (data read)

HOW TO USE HITACHI'S BUILT-IN CONTROLLER DRIVER

LCD-II(HD44780)LIQUID CRYSTAL CHARACTER DISPLAY

■ INTRODUCTION

The LCD-II (HD44780) is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip.

The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780). If a driver LSI HD44100H is externally connected to the HD44780, up to 80 characters can be displayed.

The LCD-II is produced in the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device with lower power dissipation.

■ FEATURES

- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM . . . . . 80 x 8 bits (80 characters, max.)
- Character generator ROM . . . .
  - Character font 5 x 7 dots: 160 characters
  - Character font 5 x 10 dots: 32 characters
- Both display data and character generator RAMs can be read from the MPU.
- Wide range of instruction functions
  - Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON. (Internal reset circuit)

1. Applicable type

(1) 1 line series
LM054 • LM015 • LM568F • H2570 • LM020L • LM020LN • LM020XMBL • LM087LN • LM070L • LM038 • LM027 • H2571 • H2752 • LM058

(2) 2 line series
LM052L • LM016L • LM016LN • LM016XMBL • LM104L • LM086ALN • LM093LN • LM093XMLN • LM032L • LM032LN • LM032XMBL • LM105L • LM091LN • LM091XMLN • LM060L • LM017L • LM107L • LM107XML • LM018L • LM018LN • LM092LN • LM093XMLN

(3) 4 line series
LM041L • LM044L

2. Connecting MPU with LCM

2.1 Driver circuit block diagram

Figure 1 shows the driver circuit block diagram of LCM with built-in controller LSI. Controller LSI HD44780 (LCD-II) is built-in this LCM. Also extended LCD driver LSI is built in the LCM that displays more than 16 digits.

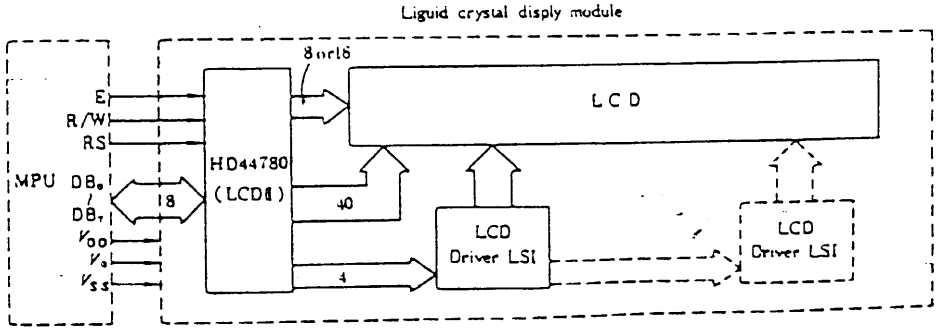


Fig. 1 Driver circuit block diagram

2.2 Interfacing to MPU

In the HD44780, data can be sent in either 4-bit 2-operation or 8-bit 1-operation so it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4-bits long, data is transferred using only 4 buses: $DB_4 \sim DB_7$. $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first, then the lower order 4 bits (content of $DB_0 \sim DB_3$ when interface data is 8 bits long) is transferred. Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit 2-operation will then transfer the busy flag and address counter data.

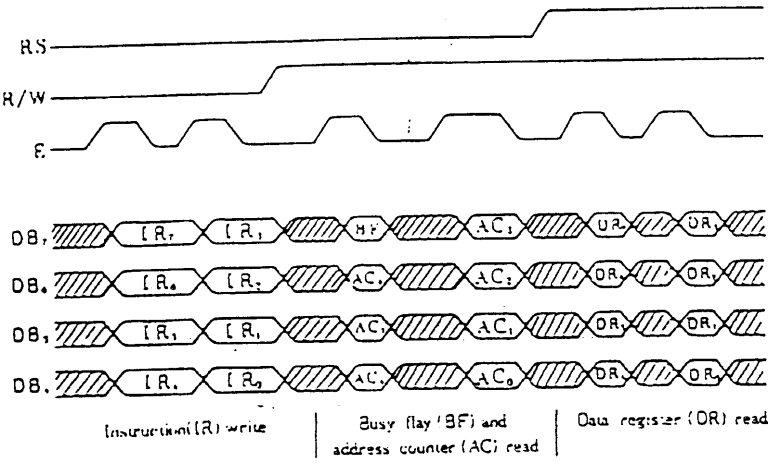


Fig. 2 4-bit data transfer example

(2) When interface data is 8 bit long, data is transferred using the 8 data buses of $DB_0 \sim DB_7$.

2.3 Interface to MPU

(1) Interface to 8-bit MPU

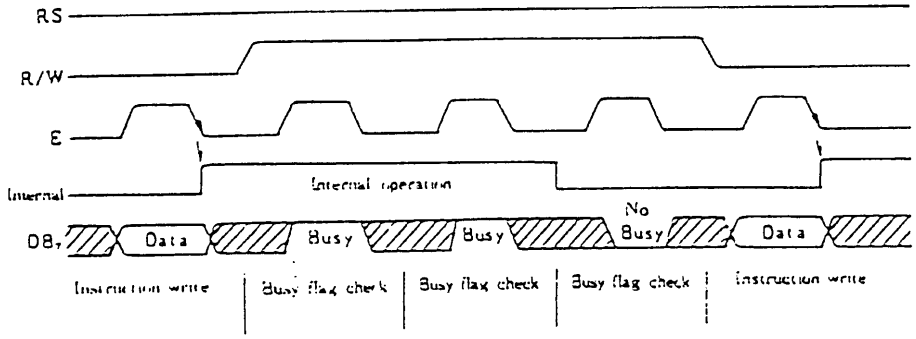


Fig. 3 Example of busy flag check timing sequence

① When connecting to 8-bit MPU through PIA

Fig. 4 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

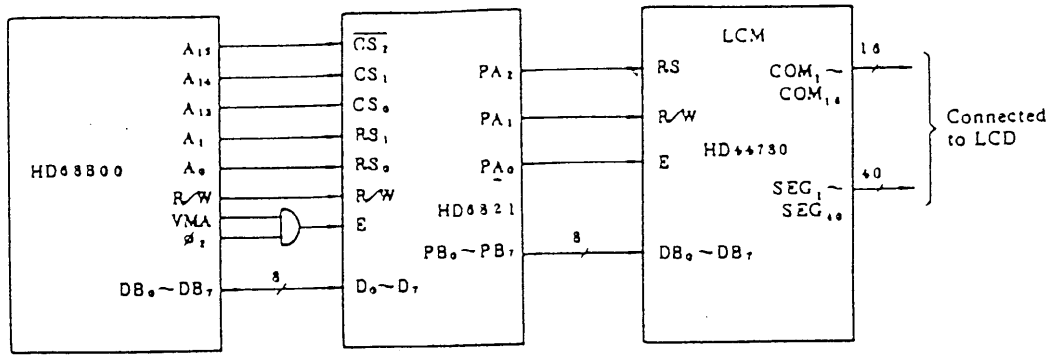
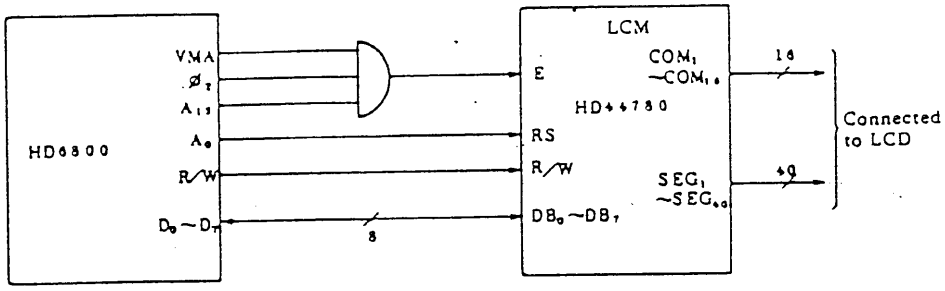
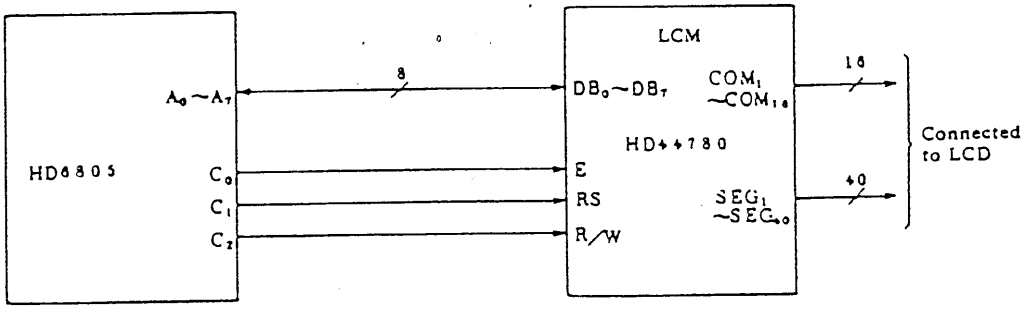


Fig. 4 Example of interface to HD68800 using PIA (HD68821)

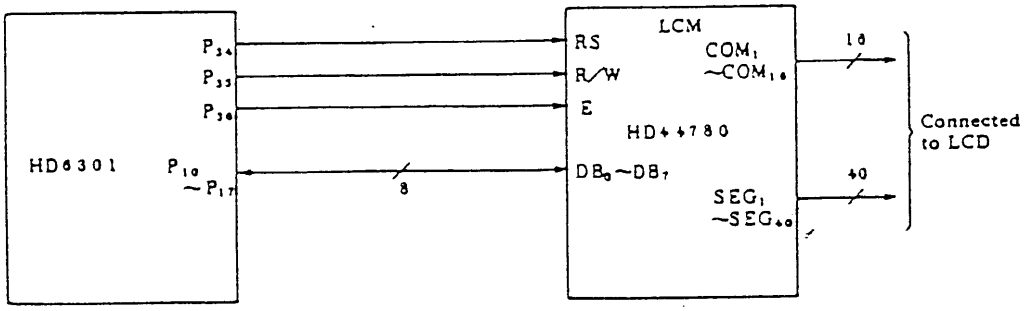
② Connecting directly to the 8 bit MPU bus line



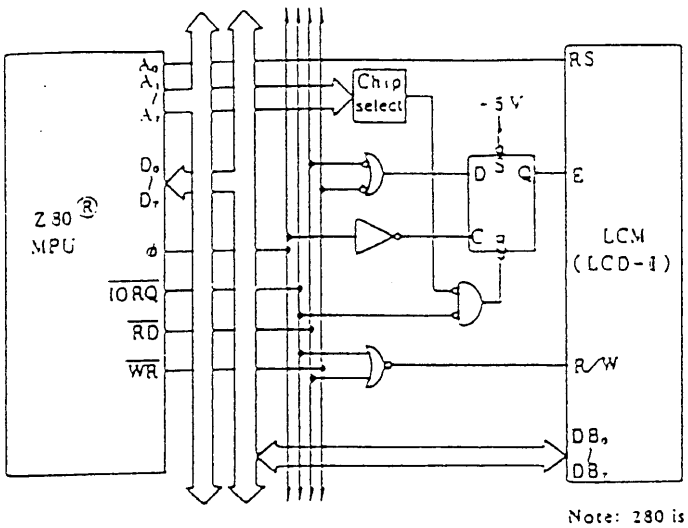
③ Example of interfacing to the HD6805



④ Example of interfacing to the HD6301



⑤ Example of interfacing to Z80 MPU



Note: Z80 is the trademark of ZILOG, U.S.A.

(a) Above circuit is an example of connection with Z80 MPU and HD44780A00 as an I/O equipment. It can be used as a part of memories by using MREQ signal.

(b) A0 signal can be used for RS signal.
A0 = 0: Instruction register is selected.
A0 = 1: Data register is selected.

(c) In order to check busy flag, transfer the data of $DB_0 \sim DB_7$ to A register (accumulator) by executing In/Out instruction. After that, busy flag can be easily checked by examining DB_7.

⑥ Example of interfacing to 80 CPU family

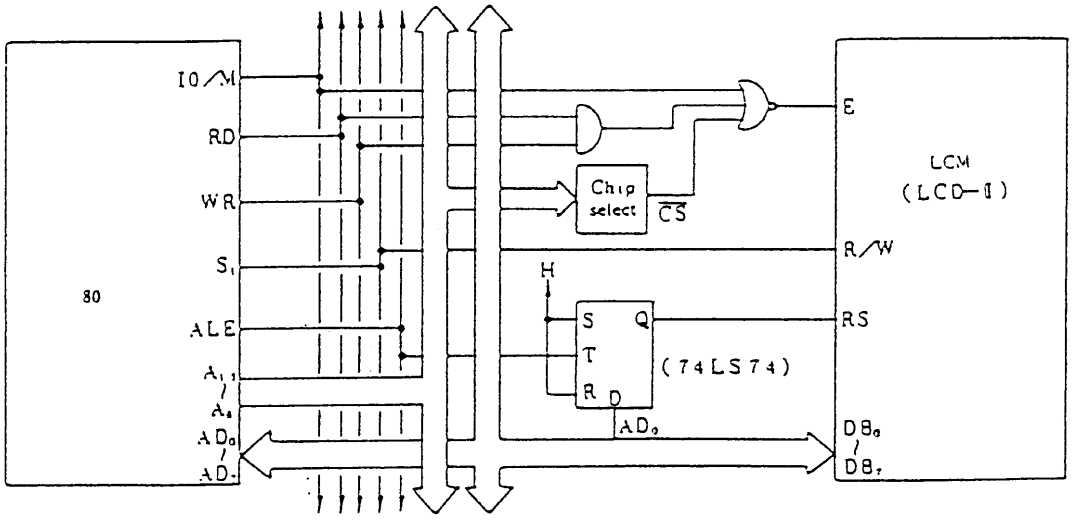


Fig. 5 Example of connection with LCM being used as a part of memories on the determined address.

Figure 5 is an example of connection with LCD module being used as a part of memories on the determined address.
Generates RS signal (Register Select signal) by latching the content of AD_0 at the rising edge of ALE signal. By using this method, you can obtain RS signal from the AD_0 among 8 bit addresses generated at the clock of the first machine cycle. In case of using LCD module as an I/O equipment, chip select signal is necessarily activated when IO/M signal is "High" level.
Furthermore, by using A8 for RS signal, the interface is easily realized.
By both methods, busy flag can be checked by storing status data into A register (Accumulator) and examining the bit 7 by software.

(2) Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See Fig. 6)

Fig. 7 shows an example of interface to the HMCS43C. Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

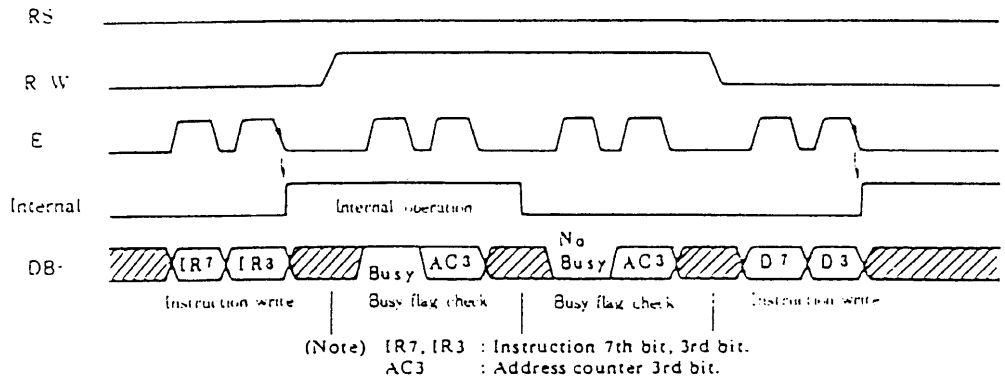


Fig. 6 An example of 4 bit data transfer timing sequence

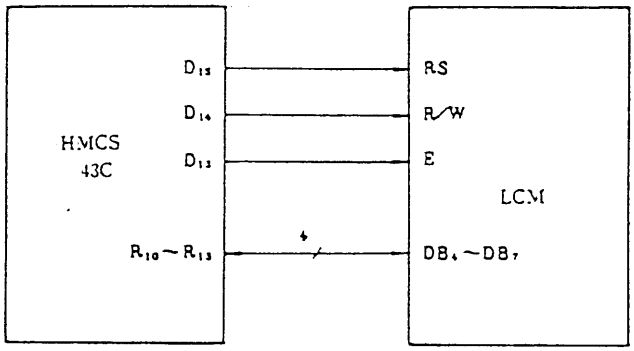


Fig. 7 Example of interface to the HMCS43C

3. Precautions on constituting hardwares

3.1 Chip select

HD44780 has no CS (chip select) terminals. Therefore, when this LSI is connected directly to Data Bus line not through PIA and so on, add the circuit that inhibits the output of Enable signal at the address which is not assigned for HD44780.

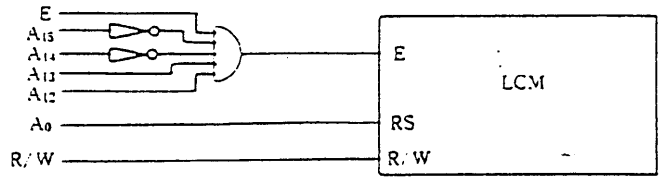


Fig. 8 Example of addresses $(3000)_{16}$ ~ $(3FFF)_{16}$ being assigned for HD44780

3.2 Ability of driving bus line

DB_0 to DB_7 can drive one TTL or capacitance of 130 pF.

The data bus terminals have three-state constructions and remain in high impedance state while Enable signal being low level.

Since the data bus has pull up MOS, it outputs high level voltage during the data bus being opened.

3.3 Power supply voltage for liquid crystal display drive

At Interface of liquid crystal display module, there are three power supply terminals, V_{DD}, GND, and V_0. LCD module is driven by the voltage that is equal to $V_{DD} - V_0$, when supplying power for liquid crystal display drive to V_0 terminal. Since suitable voltage of power supply for LCD shifts according to temperature change adjust supplying power to LCD by referring to Fig. 9 or Fig. 10.

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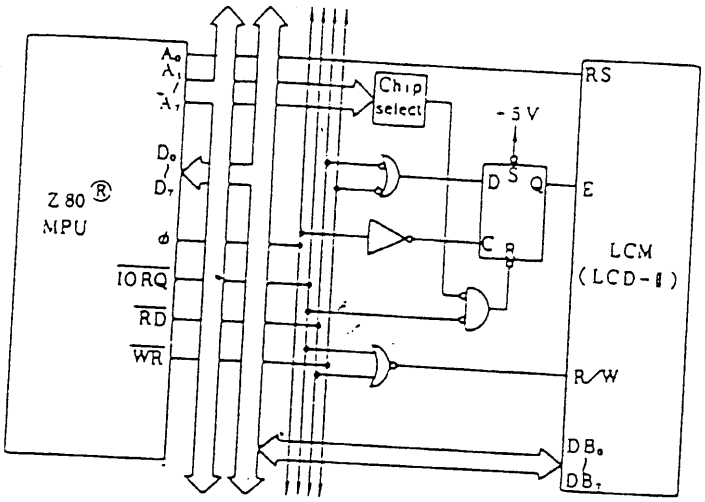

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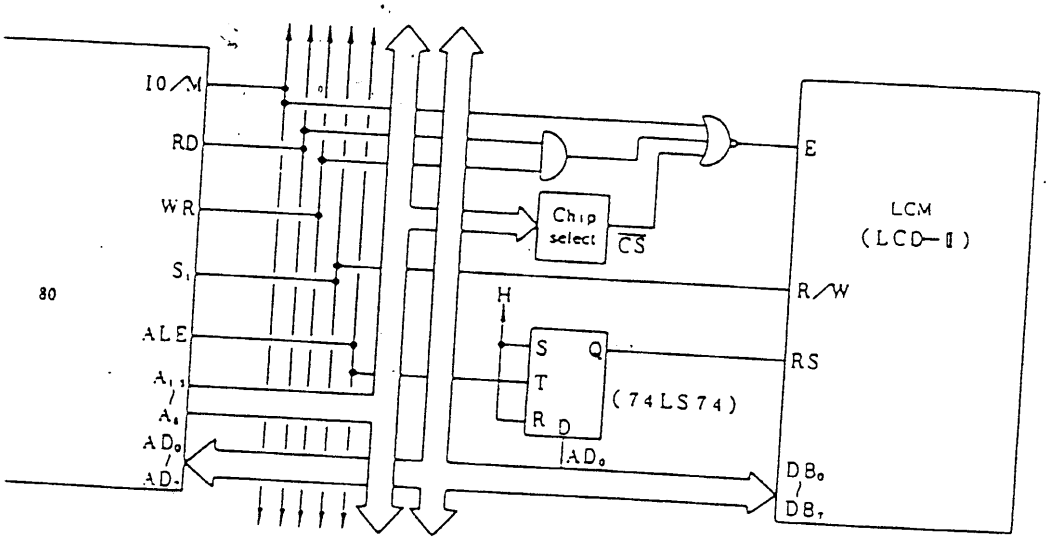

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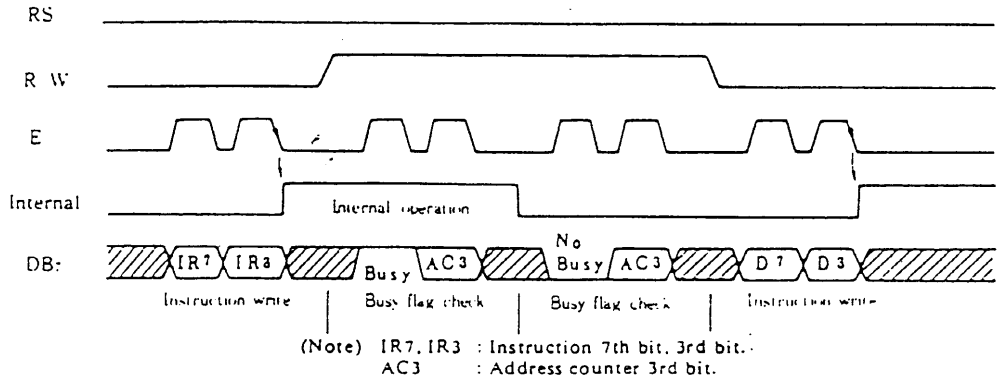

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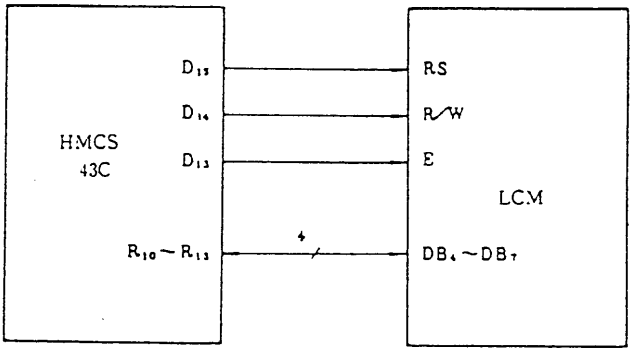

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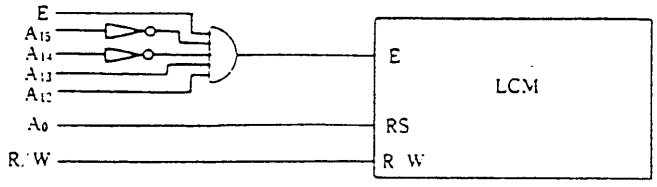

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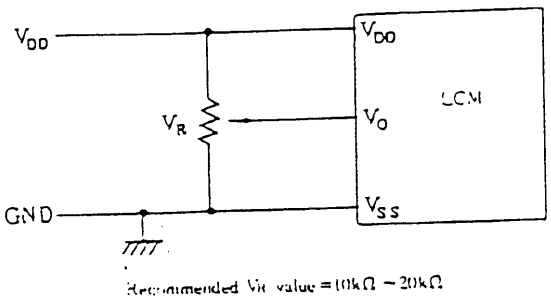
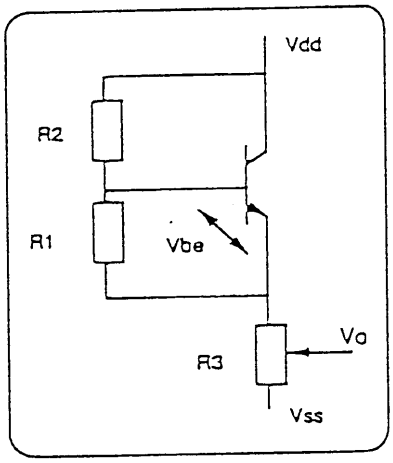
(1) Example of variable driving voltage by a variable resistance (VR)
The driving voltage can be changed by VR to compensate the influence of surrounding temperature.



Recommended VR value = 10kΩ ~ 20kΩ

Fig. 9 Variable driving voltage circuit

LCM TEMPERATURE COMPENSATION CIRCUIT



Vbe will be approximately 0.7v with a temperature coefficient of -2mV/C. The temperature coefficient of most LCD is approximately -14mV/C. If R2 is chosen to be 6 x R1 then the voltage across the transistor will be approx 4.9v with a temp coeff of -14mV/C. R3 can be adjusted to get the exact threshold voltage needed, around 8v for most wide temp LCM. This circuit works onthe principle of the voltage across R2 being controlled by Vbe,this in turn means that the current through this resistor is controlled as is that through R1. Thus the voltage generated across the circuit is controlled by the temperature coefficient of the transistor and closely tracks that of the LCD.

4. Initialization

4.1 Initializing by internal reset circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF = 1) The busy state is 10 ms after V_{CC} rises to 4.5 V.

(1) Display clear
(2) Function set ..... DL = 1 : 8 bit long interface data
N = 0 : 1-line display
F = 0 : 5 x 7 dot character font
(3) Display ON/OFF control ..... D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF
(4) Entry mode set .... I/D = 1 : +1 (increment)
S = 0 : No shift

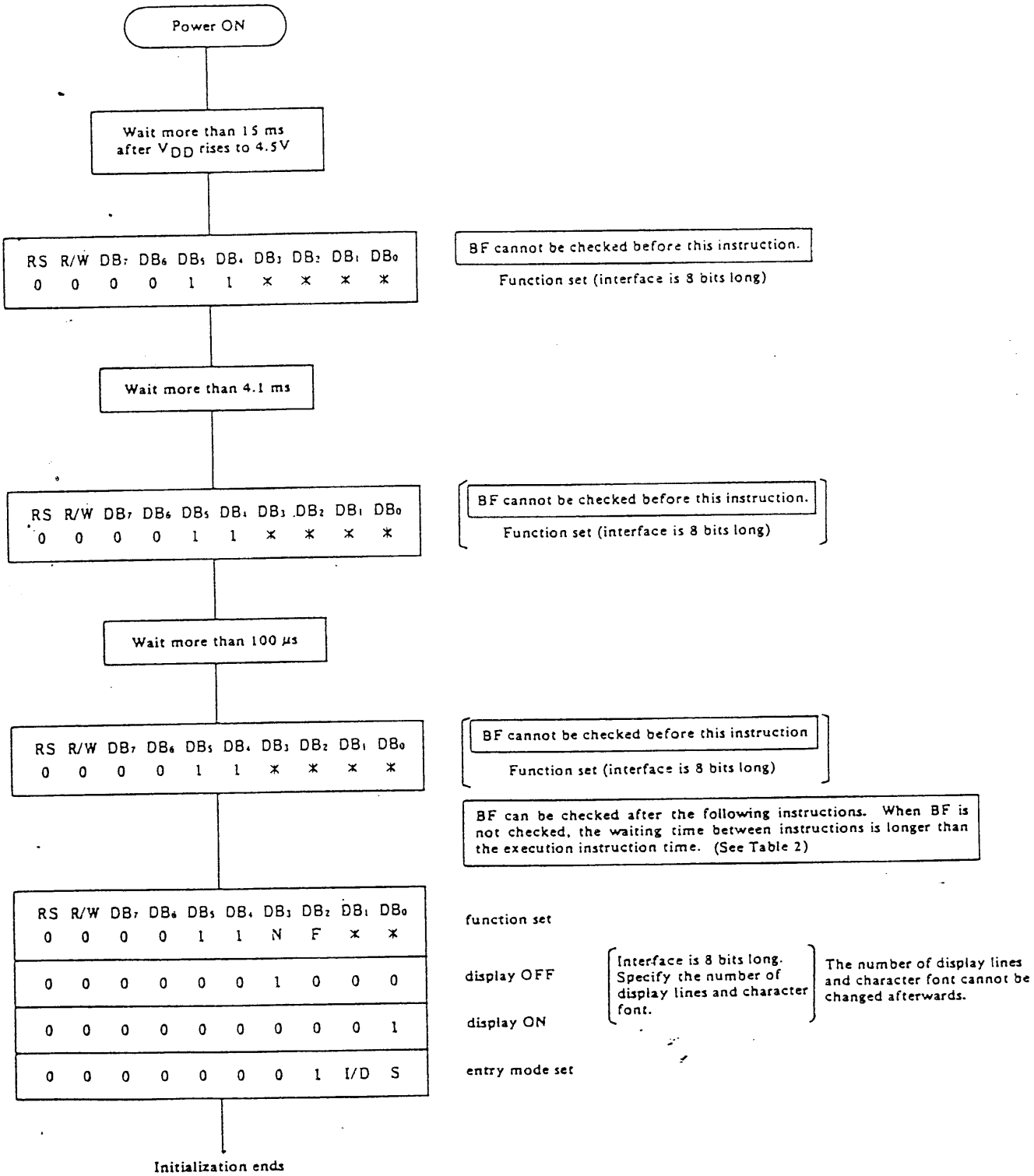
(5) Write DD RAM
When the rise time of power supply (0.2 → 4.5) is out of the range 0.1 ms ~ 10 ms, or when the low level width of power OFF (less than 0.2 V) is less than 1 ms, the internal reset circuit will not operate normally.
In this case, initialization will not be performed normally. Initialize by MPU according to "4.2 initializing by instruction" at the head of program.

4.2 Initializing by instruction

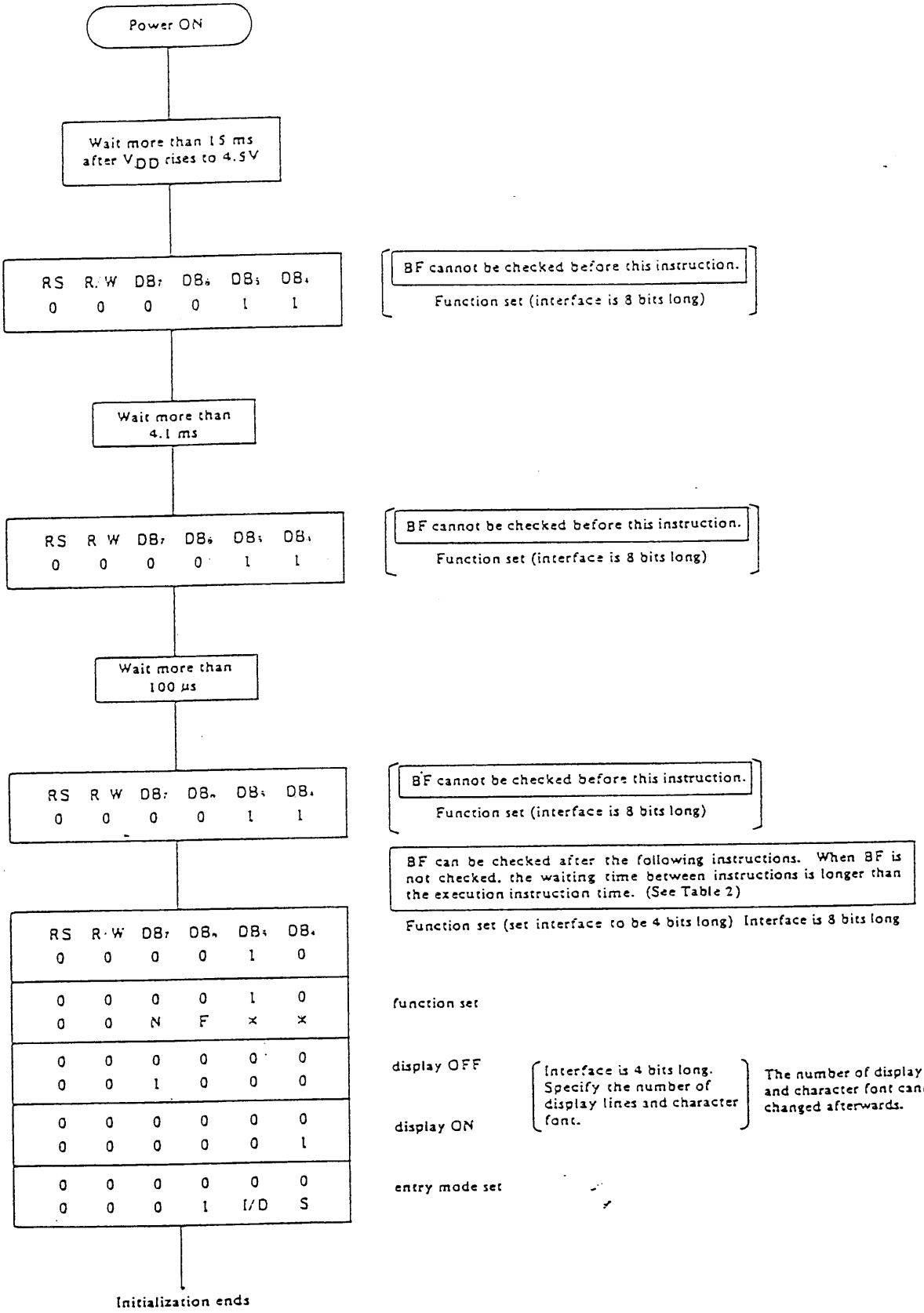
If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

(1) When interface is 8 bits long;



(2) When interface is 4 bits long



5. Instruction

5.1 Outline

Only two HD44780 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \sim DB_7$), and are called instructions, here. Table 2 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate HD44780 functions such as display format, data length, etc.
(2) Give internal RAM addresses.
(3) Perform data transfer with internal RAM
(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by −1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programming efficiency. For an explanation of the shift function in its relation to display, see 5.3.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed.

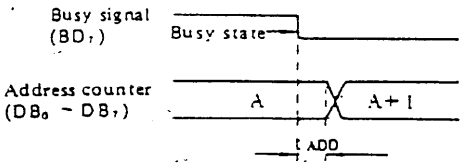
Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "1" before sending an instruction from the MPU.

Note 1

Make sure the HD44780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See Table 2 for a list of each instruction execution time.

Note 2

After executing instruction of writing data to CG/DD RAM or reading data from CG/DD RAM, RAM address counter is automatically incremented by 1 (or decremented by 1). In this case, this shift is executed after Busy Flag is set to "Low". t_{ADD} is stipulated the time from the fall edge of busy flag to the end of address counter's renewal.



t_{ADD} depends on the operating frequency

$$t_{ADD} = \frac{1.5}{f_{CP} \text{ or } f_{osc}} (s)$$

Table 2 Instructions

Instruction	Code										Description	Execution time (when fosc is 250 kHz) Note 1	Execution time (when fosc is 160 kHz) Note 2
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	82 μs ~ 1.64 ms	120 μs ~ 4.9 ms
Return home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6 ms	120 μs ~ 4.8 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 μs	120 μs
Display ON/ OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 μs	120 μs
Cursor and display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents	40 μs	120 μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F).	40 μs	120 μs
Set CG RAM address.	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs	120 μs
Set DD RAM address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs	120 μs
Read busy flag & address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	1μs	1 μs
Write data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs	120 μs
Read data to CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs	120 μs
	I/D = 1: Increment (+1) I/D = 0: Decrement (−1) S = 1: Accompanies display shift. S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right. R/L = 0: Shift to the left. DL = 1: 8 bits DL = 0: 4 bits N = 1: 2 lines N = 0: 1 line F = 1: 5 x 10 dots F = 0: 5 x 7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address Corresponds to cursor address. AC: Address counter used for both of DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fosc is 270 kHz: $40\ \mu s \times \frac{250}{270} = 37\ \mu s$	

*No effect

Notes 1. Applied to models driven by 1/8 duty or 1/11 duty.
2. Applied to models driven by 1/16 duty.

5.2 Description of details

(1) Clear display

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal) (character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return home

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	*

* No effect

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry mode set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S = 0.

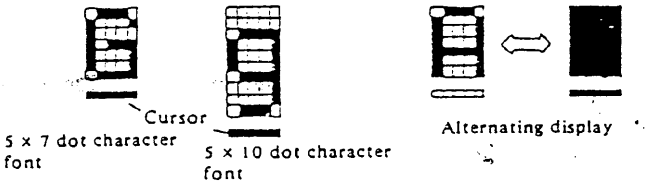
(4) Display ON/OFF control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

D: The display is ON when D = 1 and OFF when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 x 7 dot character font is selected and 5 dots in the 11th line when the 5 x 10 dot character font is selected.

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms interval when f_{CP} or f_{osc} = 250 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of f_{CP} or f_{osc}. $409.6 \times \frac{250}{270} = 379.2$ ms when f_{CP} = 270 kHz.)



(a) Cursor Display Example (b) Blink Display Example

(5) Cursor or display shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* No effect

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* No effect

DL: Sets interface data length. Data is sent or received in 8 bit lengths (DB_7 ~ DB_0) when DL = 1 and in 4 bit lengths (DB_7 ~ DB_4) when DL = 0.
When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy" flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N	F	No. of display lines	Character font	Duty factor	Remarks
0	0	1	5 x 7 dots	1/8	
0	1	1	5 x 10 dots	1/11	
1	*	2	5 x 7 dots	1/16	Cannot display 2 lines with 5 x 10 dot character font.

* No effect

(7) Set CG RAM address

	RS	R/W	DB_7						DB_0
Code	0	0	0	1	A	A	A	A	A	A

← Higher Order Bits Lower Order Bits →

Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM address

	RS	R/W	DB_7						DB_0
Code	0	0	1	A	A	A	A	A	A	A

← Higher Order Bits lower Order Bits →

Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal),
when N = 1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

(9) Read busy flag & address

	RS	R/W	DB_7						DB_0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher Order Bits Lower Order Bits →

Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.

At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

(10) Write data to CG or DD RAM

	RS	R/W	DB_7						DB_0
Code	1	0	0	0	0	0	0	0	0	0

← Higher Order Bits Lower Order Bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

← Higher Order Bits — Lower Order Bits →

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM. The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot than be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

5.3 Instruction and display correspondence

(1) 8-bit operation, 8-digit x 1-line display (using internal reset)

Following table shows an example of 8-bit x 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

8 bit operation, 8-digit 1-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed hereafter.)
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	-HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI_	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "O".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

(2) 4-bit operation, 8-digit x 1-line display (using internal reset)

The program must set functions prior to 4-bit operation. The following table shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to $DB_0 \sim DB_3$, a rewrite is then required. However, since one operation is completed in two access of 4-bit operation, a rewrite is needed as a function (see the following table).

Thus, $DB_4 \sim DB_7$ of the function set is written twice.

4 bit operation, 8-digit 1-line display (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5 x 7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

(3) 8-bit operation, 8-digit x 2-line display

For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See the following table) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second display will only move within each line many times.

8 bit operation, 8-digit x 2-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 1 0 • •		Sets to 8-bit operation and selects 2-line display and 5 x 7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

6. Precaution on programming

(1) Instruction of function set

Perform the function at the head of program that accesses HD44780 before executing all instructions, and not change the data of the Instruction Register in the program. The data of function register can be changed by the program as follows;

a. • Changing of DL (Data Length)
  • Perform the instruction appointed in 4.2 (2), when DL is changed from 8-bit length to 4-bit length mode.
  • Perform the instruction appointed in 4.2 (1), when DL is changed from 4-bit length to 8-bit length mode.

b. • Changing of N (Column Number)
  • Perform the instruction of function set after executing instruction of display clear or display off.

In this case, sequence of AC and DD RAM must be changed. Thus, rewrite the address set register after that.

c. • Changing of F (Font)
  • There is no problem in this case, but for dual-line display, the font mode of 5 x 11 cannot be selected (this mode is forbidden by hardware).

When N or F is changed, power supply voltage for LCD must be changed. If not changed, crosstalk will appear, or contrast will be poor.

(2) Busy flag check

HD44780 is produced in the CMOS process, therefore internal executing time is long. Standard time is 40 $\mu s \sim$ 1.6 ms. (This varies by instruction)

When the high speed MPU controls it, check the busy flag before performing instruction or reading data.

While internal operation is active, Enable signal is not accepted. (Enable signal at reading status register for checking busy flag is accepted) Busy flag signal is output through DB_7, as shown in Table 3, when RS = "0", R/W = "1", and Enable = "1".

(3) Input of unidentified instruction code

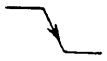
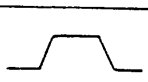
Undefined instruction code of HD44780 is only as follows;

RS	R/W	$DB_7 \sim DB$
0	0	0 ~

(Others are included to defined instruction)

When the undefined instruction code is loaded to HD44780, it accepts the code, but does not change the internal states (RAM and other status of Flags). Busy state, however continues for maximum 40 μs by the acceptance of the code.

Table 3 The relation between the operation and the combination of RS, R/W

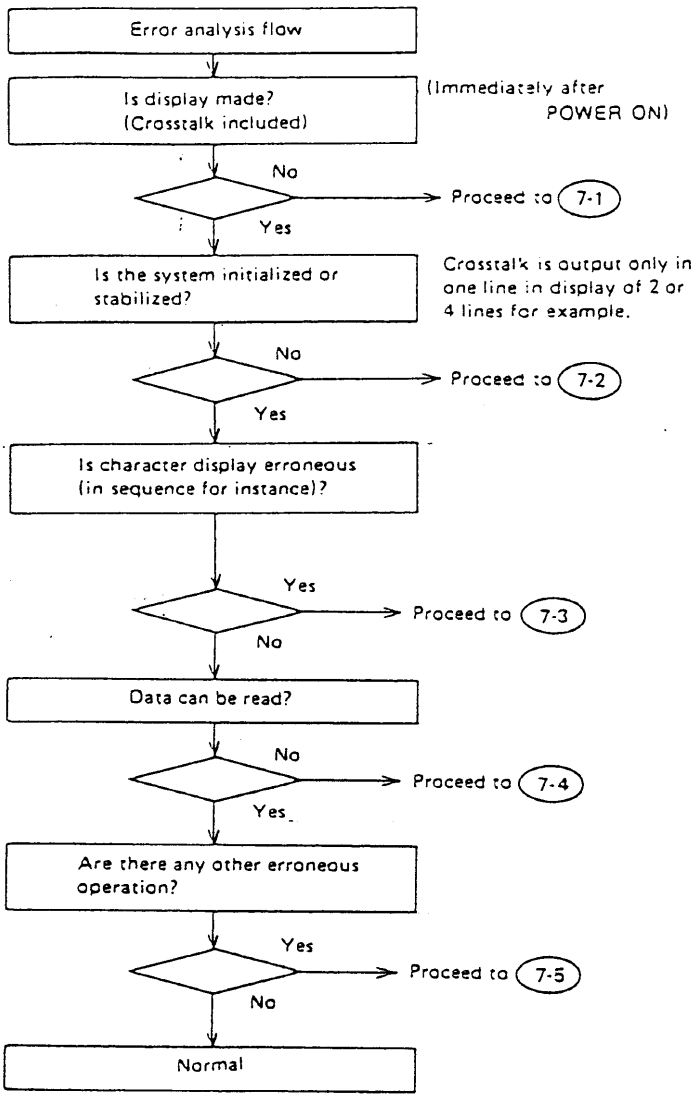
RS	RW	E	OPERATION
0	0		Write instruction code
0	1		Read busy flag and address counter
1	0		Write data
1	1		Read data

When performing data and instruction code by 4 bit, transfer RS, R/W every time.

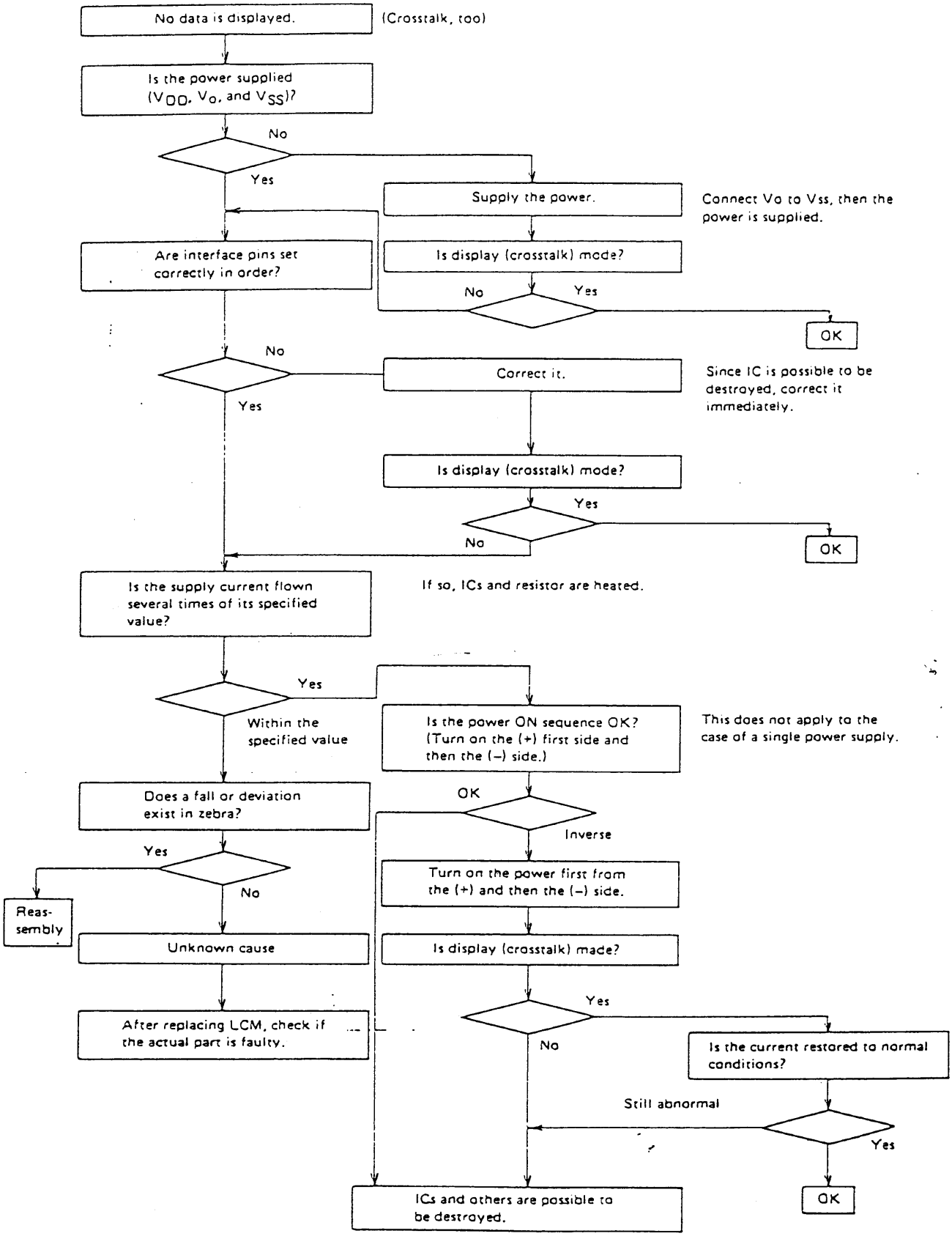
7. How to check trouble

Follow the flowchart below to check errors.

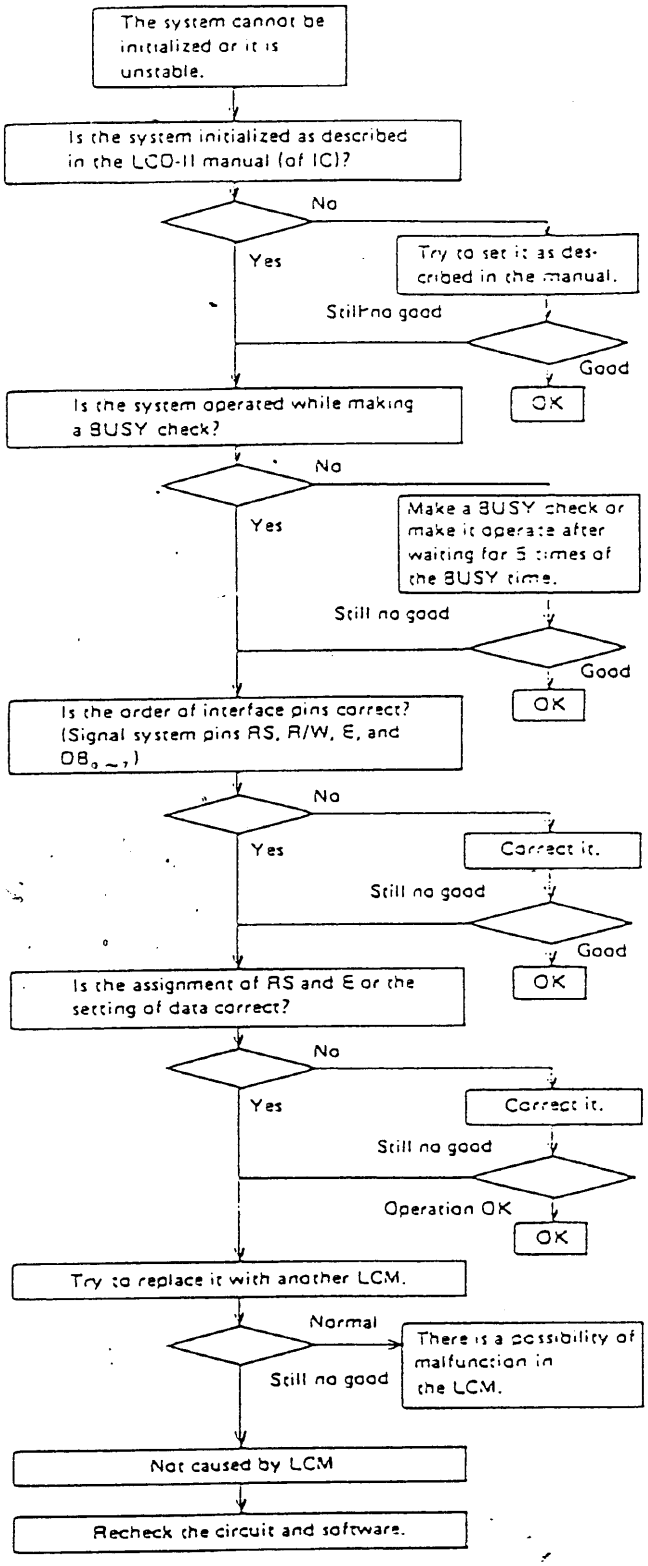
■ Error analysis flowchart



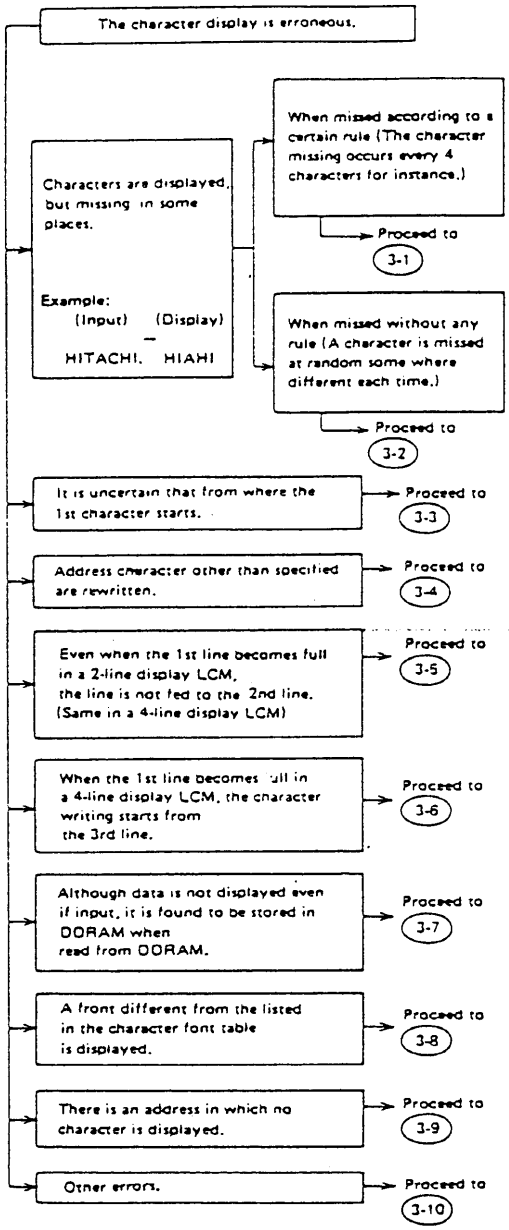
7.1 No data is displayed (Crosstalk too)



7.2 The system cannot be initialized or it is unstable.



7.3 The character display is erroneous.



(3-1)

Data is fed too fast. → Retry it while making a BUSY check. It is still too fast even when the BUSY check is made. → The function of LCD-II is no good.

(3-2)

Data is fed too fast. → Retry it while making a BUSY check.

(3-3)

The address Set command is not included in the initialization.

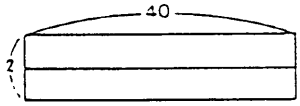
→ Although the address is so designed to be set to "00" at the power ON according to the Power ON Reset function of the LCD-II itself, this Power ON Reset function does not work in some cases according to the power ON conditions.

(3-4)

When no error exists in the software, the function of LCD-II is no good.

(3-5)

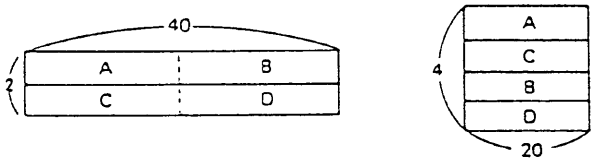
The 2-line display LCM is electrically composed of 40 characters x 2 lines, but it displays 16 characters or 20 characters partly. When 16 characters are written (in the 1st line) and the data at the 17th character is input as it is, it is entered in the 17th character in the 1st line and its is neither displayed on the screen. It is therefore necessary to set the address [LF] between the 16th caracter and 17th character.



[LF] : line feed

(3-6)

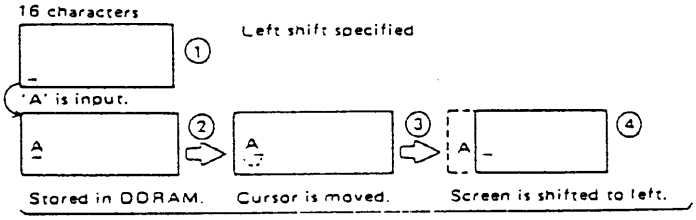
The 4-line display LCM is composed as shown in the right figure. Consequently, when written continuously from the 1st line, the data is written as A → B. When displayed in 4 lines, the data is moved from the 1st line to the 3rd line. It is therefore necessary to set the address of [LF] in this case.



(3-7)

The display ON/OFF flag is turned to the OFF side. (This flag is by no means set unless turned to the ON side.).

When employing the shift function together, the screen is shifted each time a data is written and the data can not be seen on the screen in some cases. It is therefore necessary to correct the application of the shift function.



* Since this operation is carried out in a moment, what can be seen is the status of 1 and 4 only. Although not displayed in appearance, the data is stored in the DDRAM.

(3-8)

Defective CGROM font → IC is faulty.

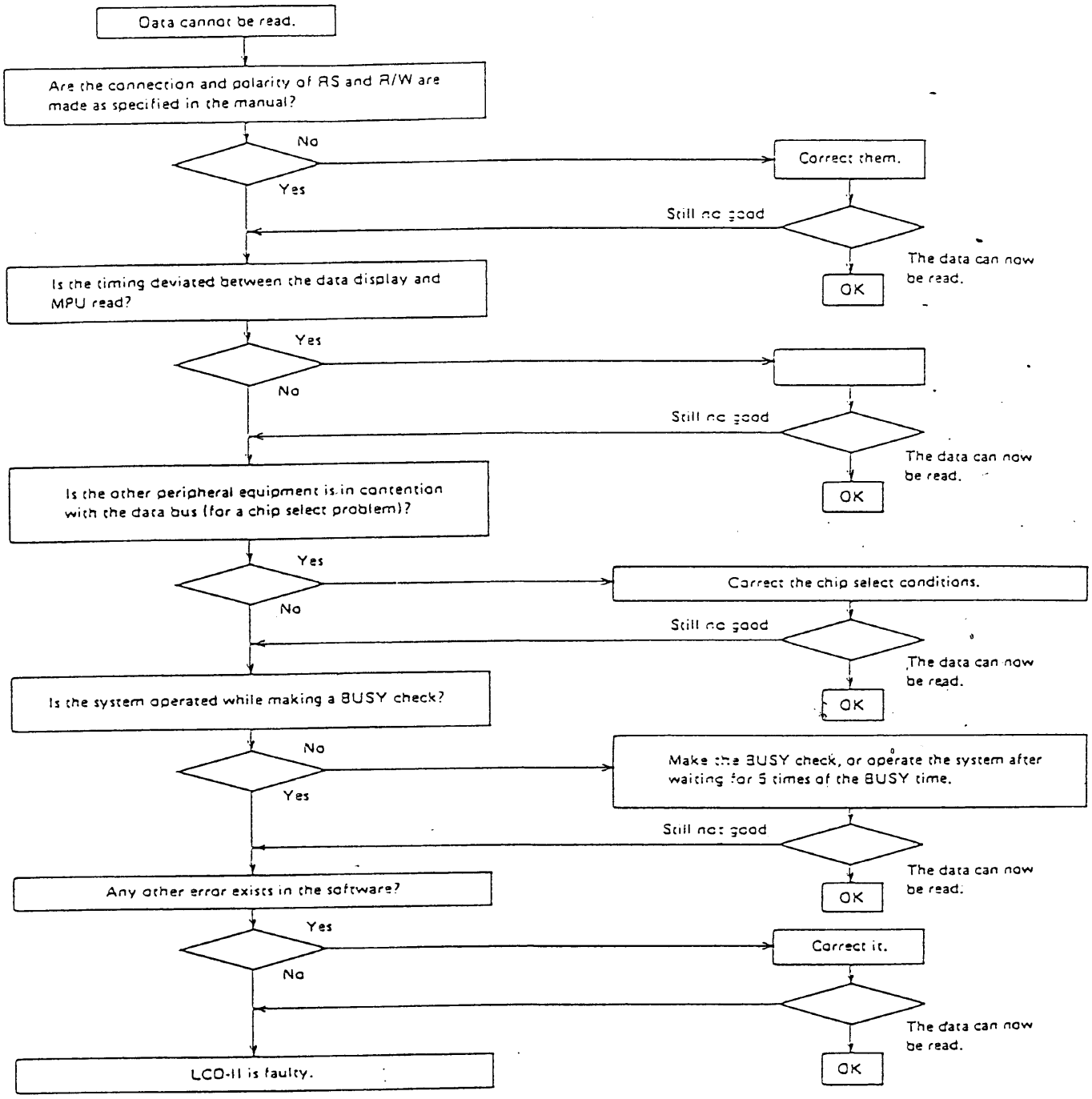
(3-9)

If no error exists in the software, the IC is faulty.

(3-10)

Contact our agent for any other erroneous event.

7.4 Data cannot be read



7.5 Others

Others

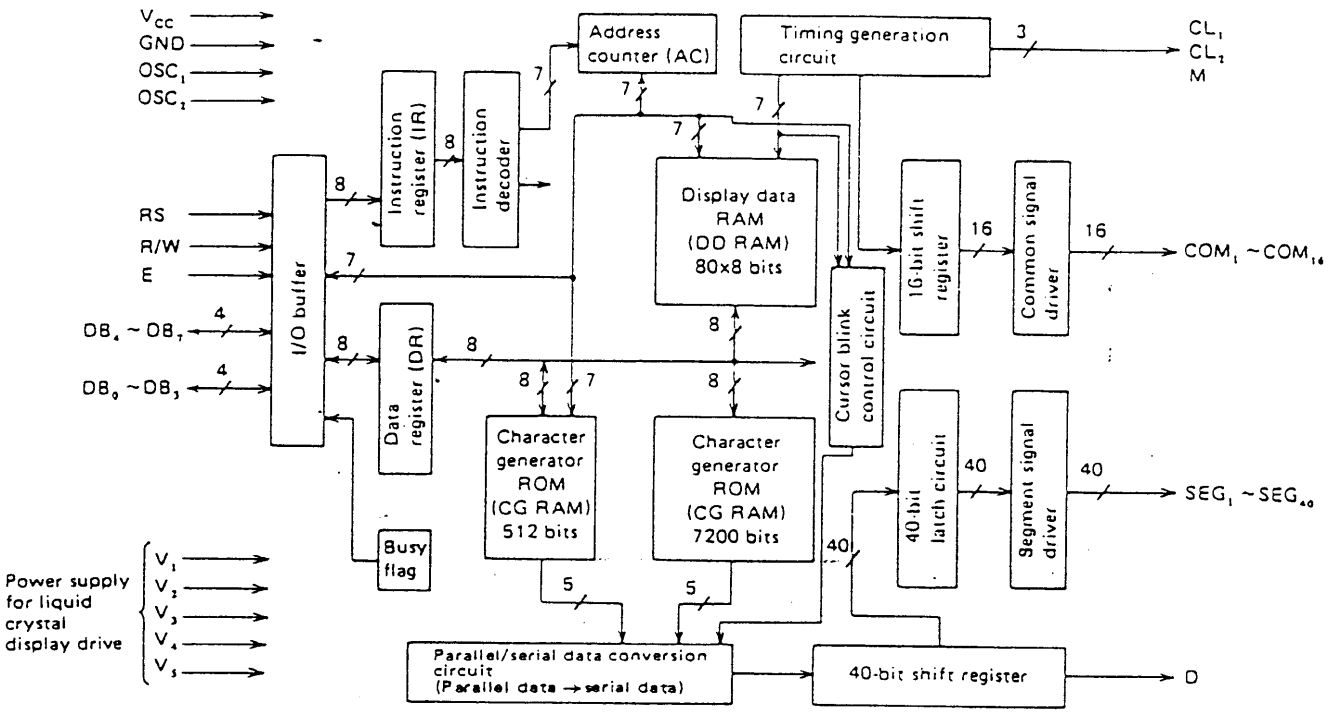
↓

Check the following:

- Use conditions
- Erroneous events
- Contents of operation before and after the error event occurrence
- Flowchart, if possible. (The program, if given, can not be decoded.)

8. Block diagram and function of each block

8.1 Block diagram of HD44780 interior



8.2 Function of each block

(1) Register

The HD44780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Table 4 Register selection

RS	R/W	E	Operation
0	0	⎺_	IR write as internal operation (Display clear, etc.)
0	1	_/⎺_	Read busy flag (DB7) and address counter (DB_0 ~ DB_6)
1	0	⎺_	DR write as internal operation (DR to DD or CG RAM)
1	1	_/⎺_	DR read as internal operation (DD or CG RAM to DR)

(2) Busy flag (BF)

When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As Table 4 shows, the busy flag is output to DB_7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)

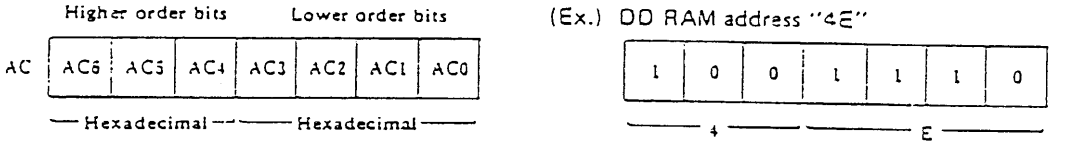
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by −1). AC contents are output DB_0 ~ DB_6 when RS = 0 and R/W = 1, as shown in Table 4.

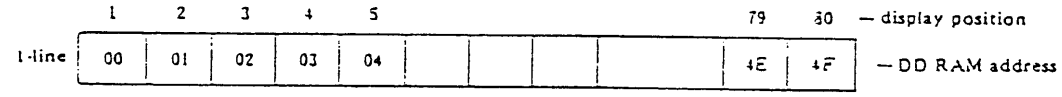
(4) Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 x 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

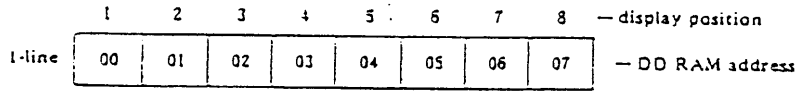
The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.



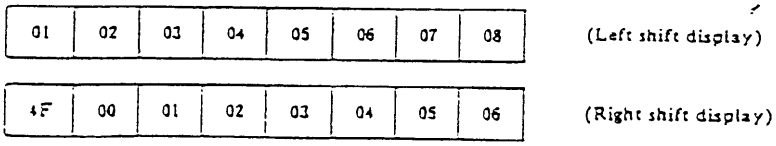
1-line display (N = 0)



(a) When the display characters are less than 80, the display begins at the head position. For example, 8 characters using one HD44780 are displayed as:



When the display shift operation is performed, the DD RAM address moves as:



(b) 16-character display using an HD44780 and an HD44100H is as shown below:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	— display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	— DD RAM address

HD44780 display — HD44100H display

When the display shift operation is performed, the DD RAM address moves as:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	(Left shift display)
4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	(Right shift display)

(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of (b).

Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	73	74	75	76	77	78	79	80	— display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	48	49	4A	4B	4C	4D	4E	4F	— DD RAM address

HD44780 display — HD44100H (1) display — HD44100H (2) ~ (8) display — HD44100H (9) display

2-line display (N = 1)

	1	2	3	4	5	.....	39	40	— display position
1-line	00	01	02	03	04	.....	26	27	— DD RAM address
2-line	40	41	42	43	44	.....	66	67	

(a) When the number of display characters is less than 40 x 2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters x 2 lines are displayed as:

	1	2	3	4	5	6	7	8	— display position
1-line	00	01	02	03	04	05	06	07	— DD RAM address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address move as:

01	02	03	04	05	06	07	08	(Left shift display)
41	42	43	44	45	46	47	48	

27	00	01	02	03	04	05	06	(Right shift display)
67	40	41	42	43	44	45	46	

(b) 16 character x 2 line are displayed when an HD44780 and an HD44100H are used.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	— display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	— DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

HD44780 display — HD44100H display

When display shift is performed, the DD RAM address moves as follows:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Left shift display)

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(Right shift display)

(c) The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of (b).

Since the increase can be 8 digits x 2 lines for each additional HD44100H, up to 40 digits x 2 lines can be displayed by connecting 4 HD44780's externally.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		33	34	35	36	37	38	39	40
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	·····	20	21	22	23	24	25	26	27
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	·····	60	61	62	63	64	65	66	67

— display position

— DD RAM address

— HD44780 display — — HD44100 (1) display — — HD44100H (2) (3) display — — HD44100H (4) —

(d) Display position and DD RAM address for LM020L.

Character NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM address	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

(Note) Shift display is as same as that of 8 char. x 2 line type.

(e) Display position and DD RAM address for LM041L.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
3-line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
4-line	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

— display position

— DD RAM address

(f) Display position and DD RAM address for LM044L.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
3-line	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
4-line	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

— display position

— DD RAM address

(Note) Shift display is as same as 2-line type.

(5) Character generator ROM (CG ROM)

The character generator ROM generates 5 x 7 dot or 5 x 10 dot character patterns from 8-bit character codes. It can generate 160 types of 5 x 7 dot character patterns and 32 types of 5 x 10 dot character patterns. Tables 5(1) and 5(2) show the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programming ROM. For details, see "The LCD-II (HD44780) Breadboard User's Manual"

(6) Character generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 x 7 dots, 8 types of character patterns can be written and with 5 x 10 dots 4 types can be written. Write the character codes in the left columns of Tables 6(1) and 6(2) to display character patterns stored in CG RAM.

Table 5 shows the relation between CG RAM addresses and data and display patterns.

As Table 5 shows, an area that is not used for display can be used as a general data RAM.

(7) Timing generation circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(8) Liquid crystal display driver circuit

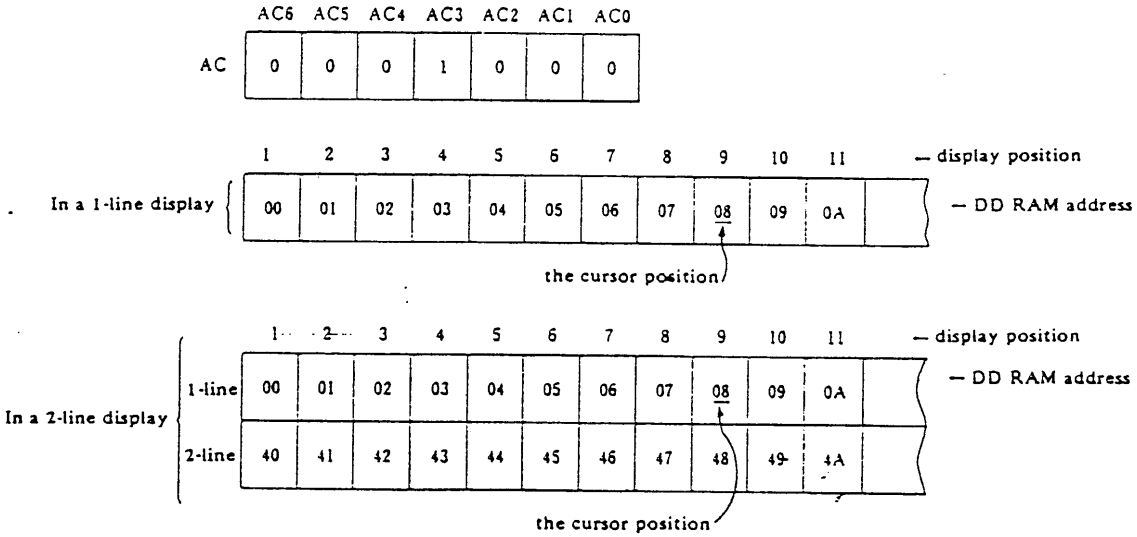
The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms. The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension. Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

(9) Cursor/Blink control circuit

This is the circuit that generates the cursor or blink. The cursor or the blink appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is $(08)_{16}$, a cursor position is:



(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

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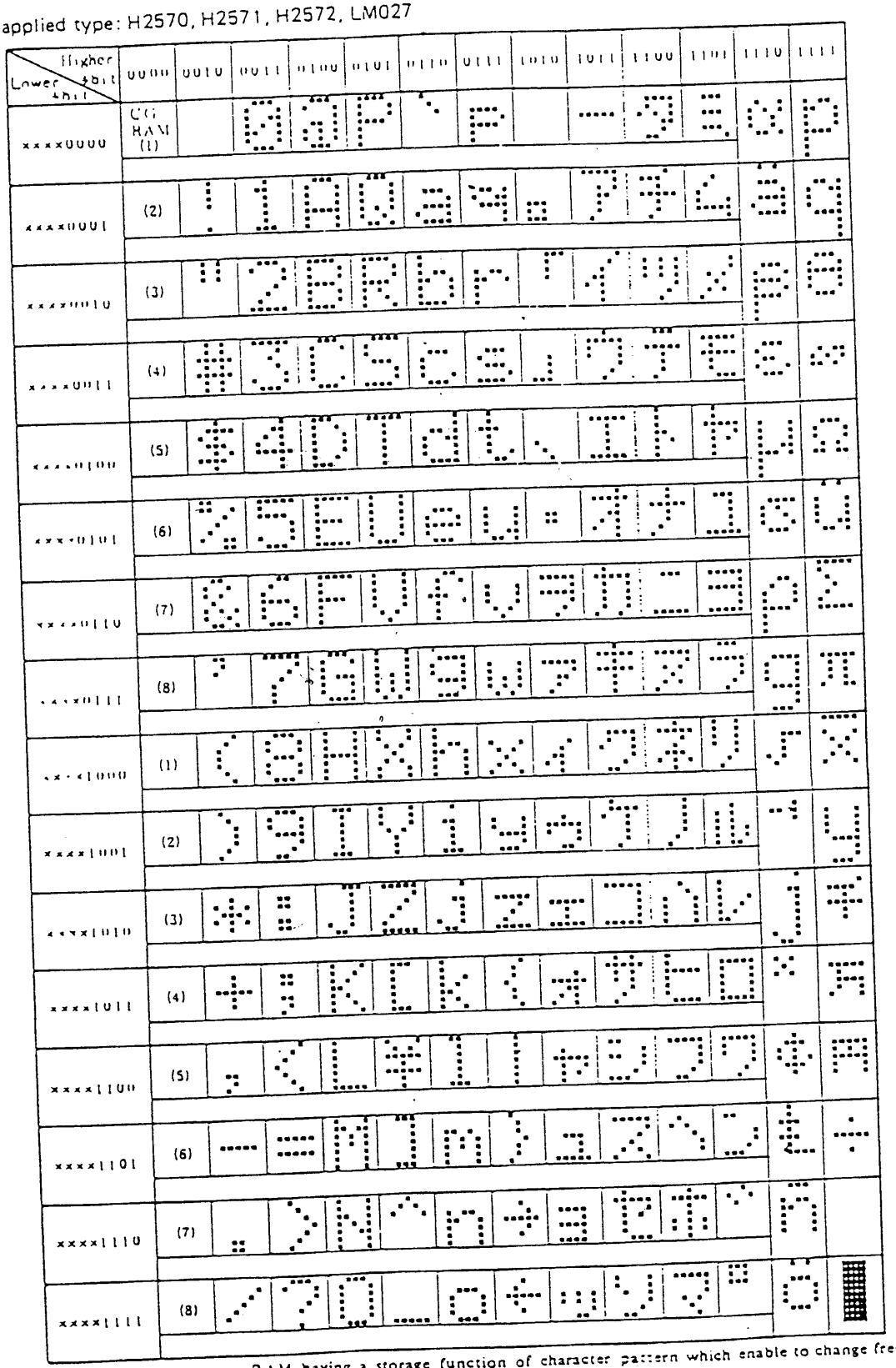
Table 5

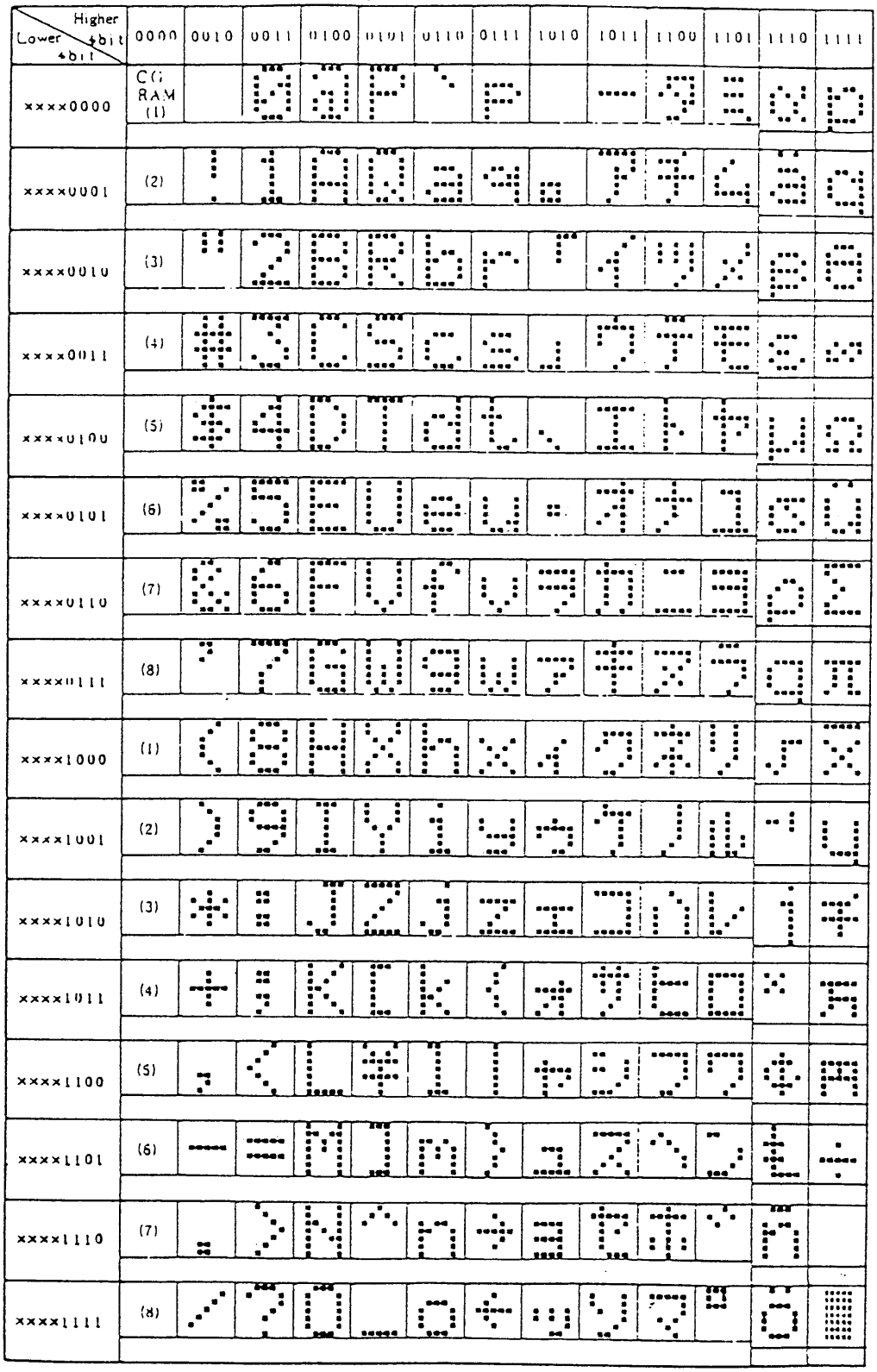
CORRESPONDENCE BETWEEN CHARACTER CODES AND CHARACTER PATTERN

(1) 5 x 10 dot, applied type: H2570, H2571, H2572, LM027



Note 1. CG RAM is a character generator RAM having a storage function of character pattern which enable to change freely by users program.
Note 2. When line setting at initialization is 2 lines (N = 1), pattern becomes 5 x 7 dot.

(2) 5 x 7 dot, applied type: Character display modules (including LED backlight versions)



Note: CG ROM is a character generator RAM having a storage function of character pattern which enable to change freely by users program.

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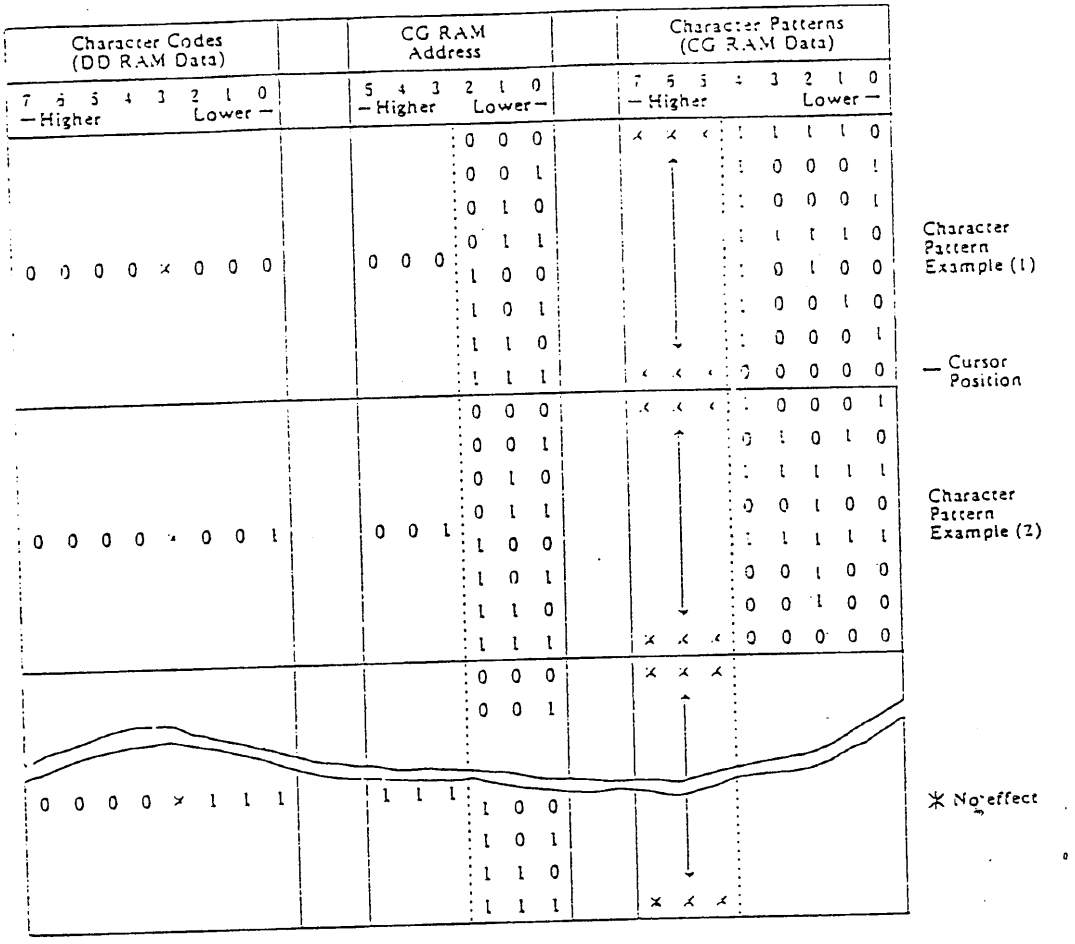
Table 6 Relation between CG RAM addresses and character code (DD RAM) and character pattern (CG RAM data).

(1) For 5 x 7 dot character pattern



(Note) 1: Character code bits 0 ~ 2 correspond to CG RAM address bits 3 ~ 5 (3 bits: 8 types).

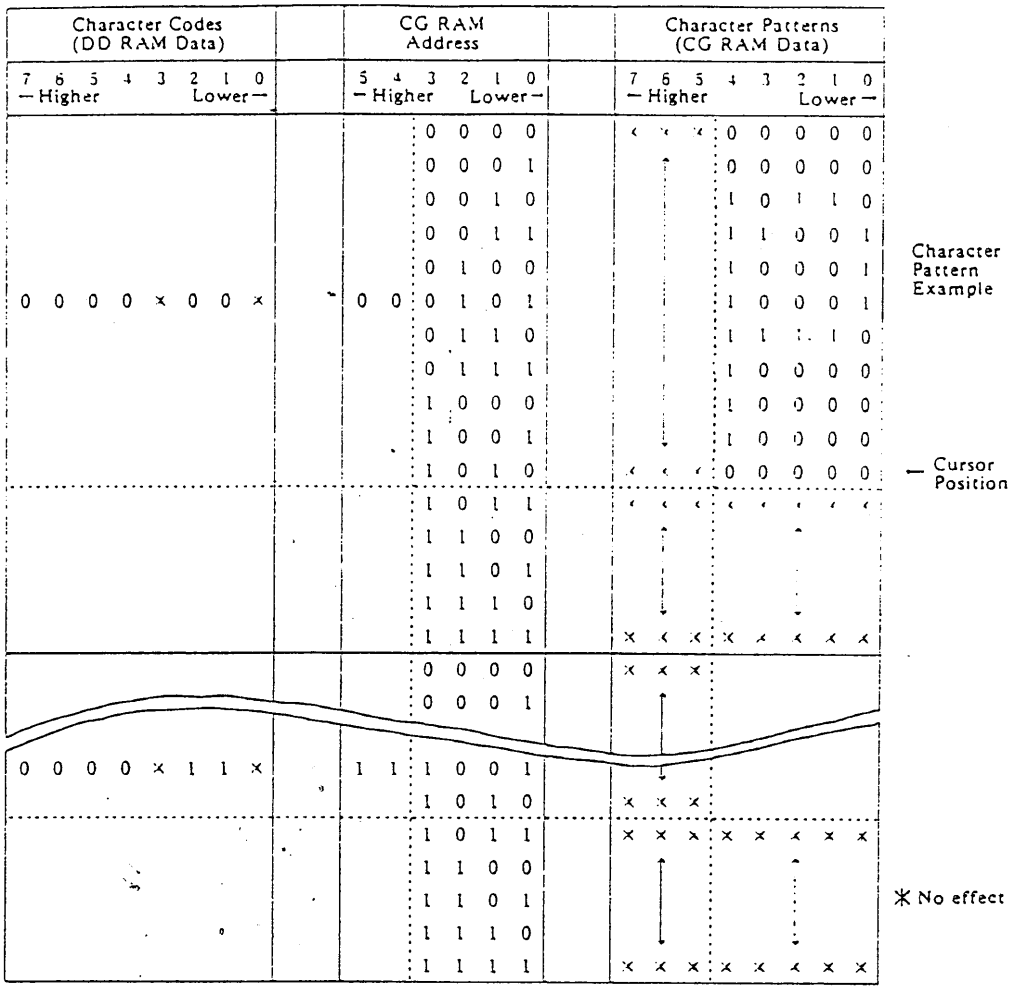
2: CG RAM address bits 0 ~ 2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR by the cursor.
Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.

3: Character pattern row positions correspond to CG RAM data bits 0 ~ 4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM.

4: As shown in Tables 3 and 4, CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 3 is a ineffective bit, the "R" display in the character pattern example, is selected by character code "00" (hexadecimal) or "08" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

For 5 x 10 dot character pattern



(Note) 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).

2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.
Maintain the 11th line data corresponding to the cursor display position in the "0" state for cursor display. When the 11th line data is "1", bit 1 lights up regardless of cursor existence. Since the 12th ~ 16th lines are not used for display, they can be used for the general data RAM.

3: Character pattern row positions are the same as 5 x 7 dot character pattern positions.

4: CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, "P" display in the character pattern example is selected by character code "00", "01", "08" and "09" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.