

- 24 Character x 1 line
- Built-in control LSI HD44780 type (see page 23)
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	126W x 36H x 12D (max) mm
Effective display area	100W x 13.8H mm
Character size (5 x 10 dots)	3.15W x 7.9H mm
Pitch	3.75 mm
Dot size	0.55W x 0.7H mm
Weight	about 40 g

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (V_i)	V_{SS}	V_{DD} V
Operating temperature (T_a)	0	50°C
Storage temperature (T_{stg})	-20	70°C

ELECTRICAL CHARACTERISTICS

$$T_a = 25^\circ\text{C}, V_{DD} = 5.0\text{ V} \pm 0.25\text{ V}$$

Input "high" voltage (V_{IH}) 2.2 V min.

Input "low" voltage (V_{IL}) 0.6 V max.

Output high voltage (V_{OH}) ($-I_{OH}=0.2$ mA) . . 2.4 V min.

Output low voltage (V_{OL}) ($I_{OL} = 1.2 \text{ mA}$) 0.4 V max.

Power supply current (I_{DD}) ($V_{DD} = 5.0\text{ V}$) . . . 0.5 mA typ.

2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

$$Du = 1/8 \quad Du = 1/11$$

at $T_a = 0^\circ\text{C}$	4.0	4.2 V typ.
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at $T_a = 25^\circ\text{C}$ 3.7 3.8 V typ.

at $T_a = 50^\circ\text{C}$ 3.3 3.3 V typ.

OPTICAL DATA..... See page 8

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V _{SS}	—	0V	Power supply
2	V _{DD}	—	+5V	
3	V _O	—	—	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Note:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

- (1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB_7$, and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$ when interface data is 8 bits long).
- (2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB_7$.

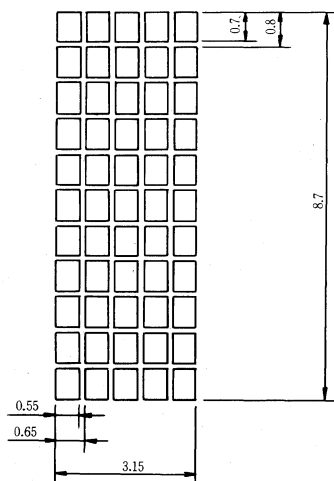


Fig. 1 Display pattern

Unit: mm

Technical drawing of a 12U rack with dimensions in mm. The drawing includes a front view and a side view.

Front View Dimensions:

- Overall width: 126.0 ± 0.5
- Overall height: 36.0 ± 0.5
- Top flange width: 2.5 ± 0.5
- Top flange height: 2.5 ± 0.5
- Top flange thickness: 2.54
- Top flange hole diameter: $14 - \phi 1.0 \pm 0.1$
- Top flange hole spacing: 12.6 ± 0.3
- Top flange hole offset: 121.0 ± 0.3
- Top flange hole diameter: 110.0 ± 0.3
- Top flange hole offset: 8.7 ± 0.2
- Top flange hole diameter: 2.55 ± 0.5
- Top flange hole offset: 6.6 ± 0.3
- Top flange hole diameter: 13.8 ± 0.3
- Top flange hole offset: 27.0 ± 0.3
- Top flange hole diameter: $4 - \phi 2.7 \pm 0.2$
- Top flange hole offset: 89.4 ± 0.2
- Top flange hole diameter: 100.0 ± 0.3
- Top flange hole offset: 5.5
- Top flange hole diameter: 5.3 ± 0.5
- Top flange hole offset: 10.5 ± 0.5
- Top flange hole diameter: 31.0 ± 0.2
- Top flange hole offset: 5.5
- Top flange hole diameter: $4.7 - 5.3$
- Top flange hole offset: 7.3 max

Side View Dimensions:

- Overall depth: 12.0 max
- Side flange width: 4.0 max
- Side flange height: 1.6 ± 0.2

* IC height

[illegible]

LCM

V_{DD} (+5V)

V_0

V_{SS}

$V_{DD} - V_0$

V_R

V_{DD}

$V_{DD}-V_0$: LCD driving voltage
 V_R : 10k Ω ~20k Ω

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TIMING CHARACTERISTICS

Item	Symbol	Test condition	min.	typ.	max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	—	—	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	—	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	—	—	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	—	—	ns
Data delay time	t_{DDR}	Fig. 6	—	—	320	ns
Data set up time	t_{DSW}	Fig. 5	195	—	—	ns
Hold time	t_H	Fig. 5, Fig. 6	20	—	—	ns

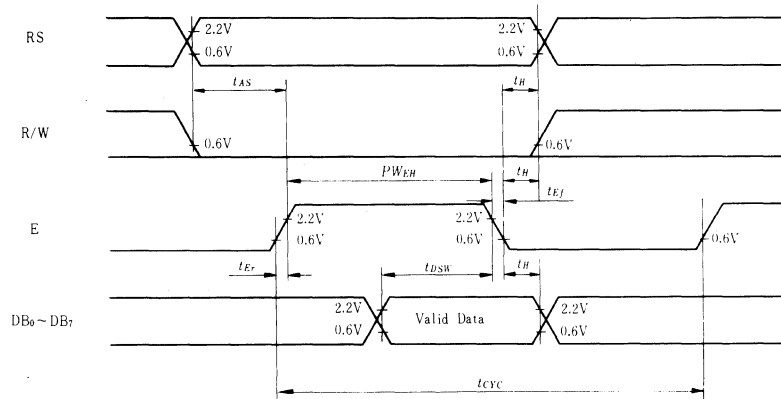


Fig. 5 Interface timing (data write)

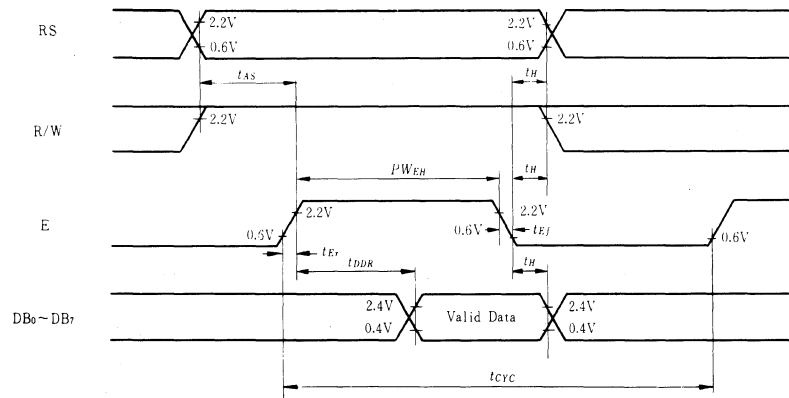


Fig. 6 Interface timing (data read)