LM041L

- 16 Character x 4 lines
- Built-in control LSI HD44780 type (see page 23)
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 87W x 60H x 12D (max.) mm
Effective display area . . . . . 61.8W x 25.2H mm
Character size (5 x 7 dots) . . . . . 2.95W x 4.15H mm
Pitch . . . . . 3.55 mm
Dot size . . . . . 0.55W x 0.55H mm
Weight . . . . . about 60g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V
Input "high" voltage (V_{iH}) . . . . . 2.2V min.
Input "low" voltage (V_{iL}) . . . . . 0.6V max.
Output high voltage (V_{OH}) ($-I_{OH}$=0.2mA) . . . 2.4V max.
Output low voltage (V_{OL}) (I_{OL}=1.2mA) . . . . . 0.4V max.
Power supply current (I_{DD}) (V_{DD}=5.0V) . . . 1.0 mA typ.
3.0mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Du=1/16
at Ta=0°C . . . . . 4.6 V typ.
at Ta=25°C . . . . . 4.4 V typ.
at Ta=50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 8

Unit: mm

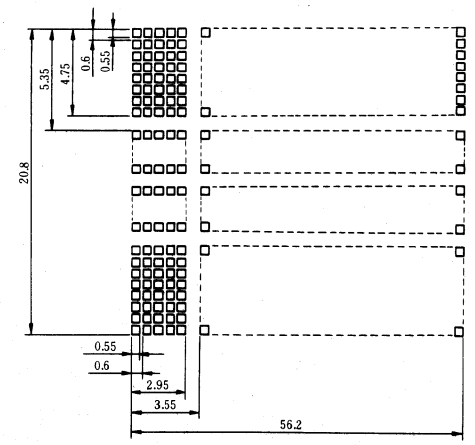

Fig. 1 Display pattern

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Note:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

DISPLAY POSITION AND DD RAM ADDRESS

Character No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
2nd line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF
3rd line	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
4th line	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF

Note:
(1) 80 ~ DF are described in hexidecimal for DD RAM address.
(2) The set to HD44780 are "N = "1", F = "0" (2 lines 5 x 7 + cursol)."
(3) DD RAM address is no series in line. Address set is necessary to change the lines.
(4) Circuit is equal to 32 characters by 2 lines type.
(5) In case of executing shift, first line and third line are shifted continuously, also second line and fourth line. Therefore it happens that display of third line is transfered to first line.

Unit: mm

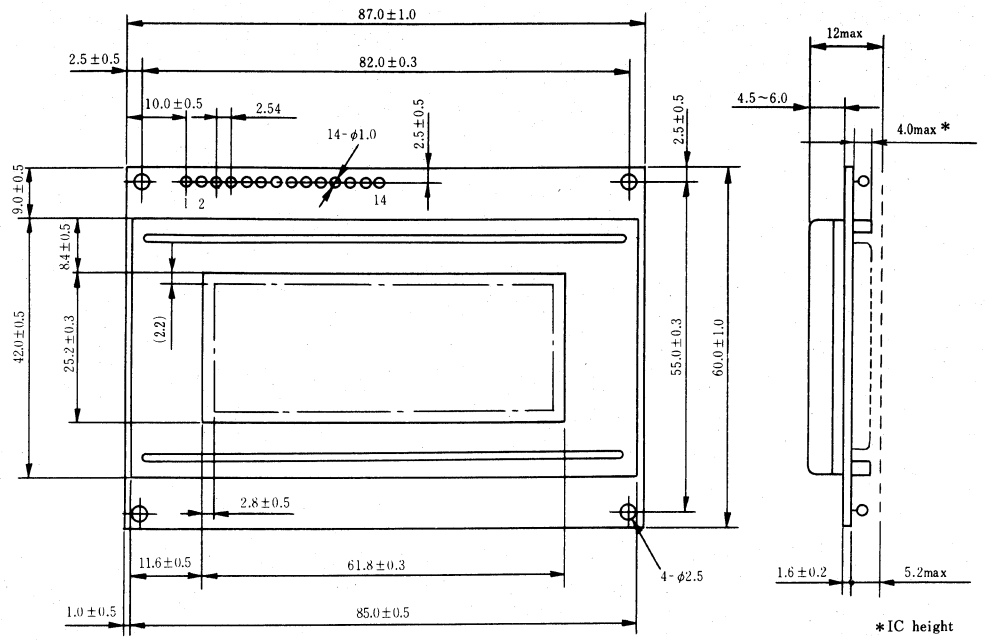

Fig. 2 External dimensions

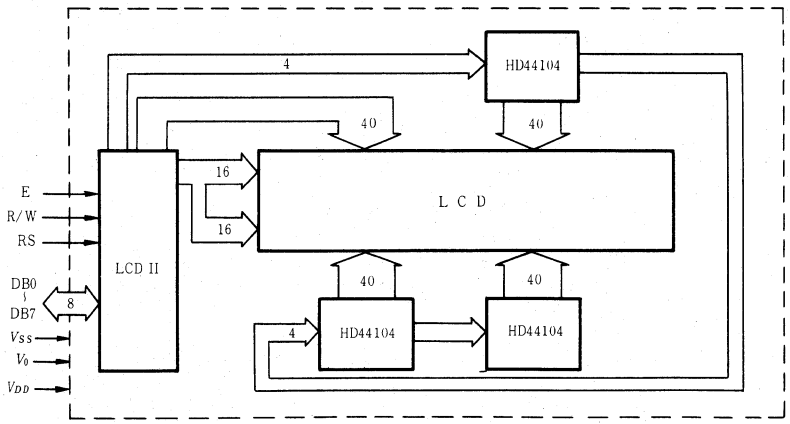

Fig. 3 Block diagram

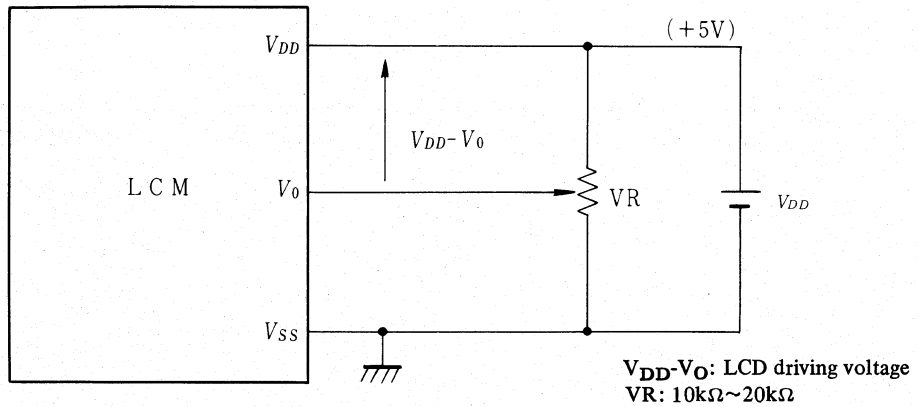

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	min.	typ.	max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

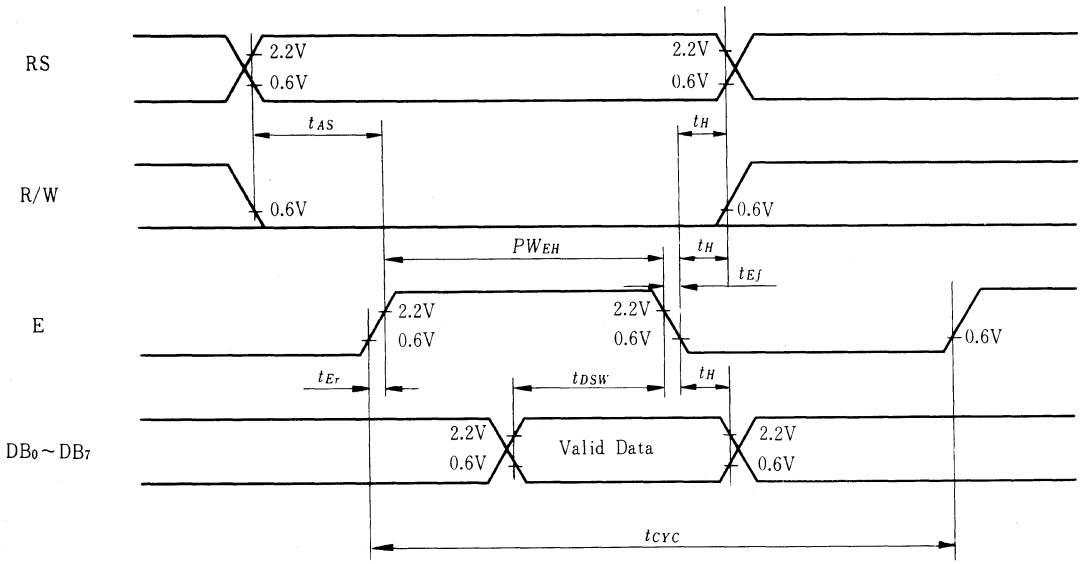

Fig. 5 Interface timing (data write)

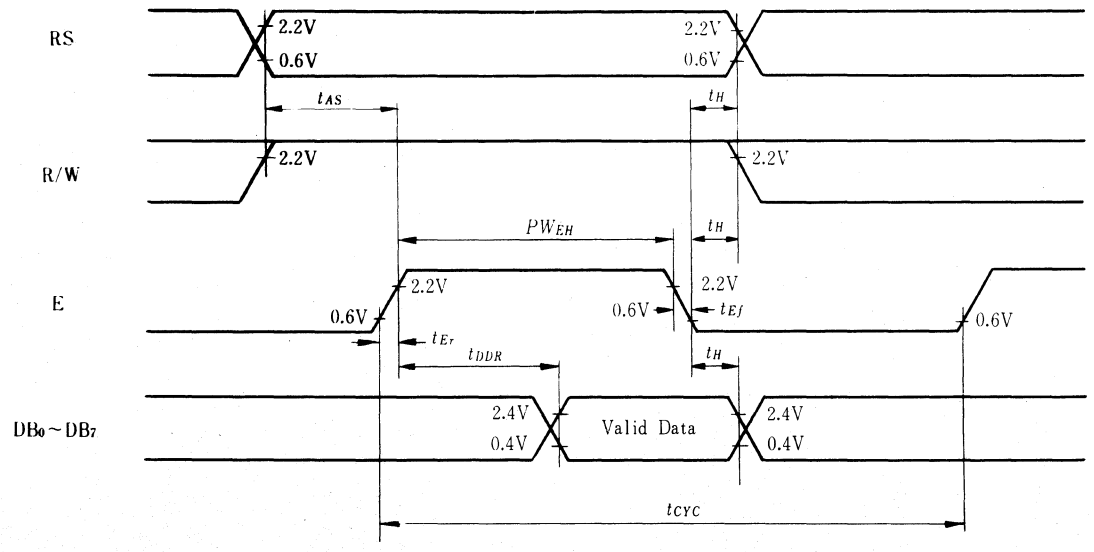

Fig. 6 Interface timing (data read)