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SHARP

TECHNICAL LITERATURE

MODEL NO. **LM057QC1T01**

DOC. NO. LC98X57

DATE NOV.2.1998

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PRESENTED
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RECORDS OF REVISION	SPEC No. LC98X57	MODEL No. LM057QC1T01
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DATA	SPEC REVISED No.	REVISED No.	REF. PAGE	SUMMARY	CHECK & APPROVAL

SHARP

SPEC No.	MODEL No.	PAGE
LC98X57	LM057QC1T01	1

○Contents

1.Application

This data sheet is to introduce the specification of LM057QC1T01,negative Matrix type Color LCD module.

2.Construction and Outline

Construction: 320×RGB×240 dots color display module consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TCP(tape carrier package) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically. Signal ground(Vss) is connected with the metal bezel.

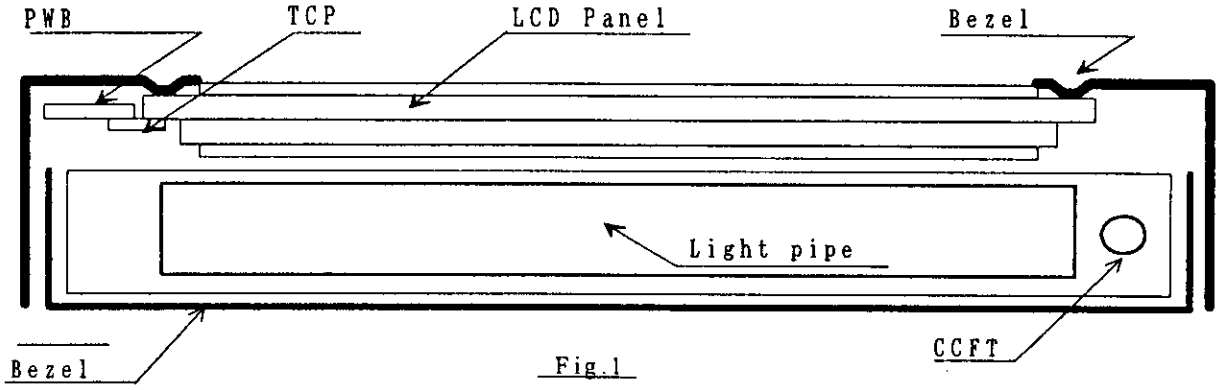


Fig.1

Outline :See Fig. 13

Connection :See Fig. 13 and Table 6

Application inspection standard

The LCD module shall meet the following inspection standard : S-U-014

3.Mechanical Specification

Table 1

Parameter	Specifications	Unit
Outline dimensions *1	154.6±0.5(W)×114.8±0.5(H)×8.3±0.5(D)	mm
Viewing area	118.2(W)×89.4(H)	
Active area	115.18(W)×86.38(H)	mm
Display format	320×RGB(W)×240(H)	mm
Dot size	0.1×RGB(W)×0.34(H)	-
Dot spacing	0.02	mm
Base color *2	Normally black *3	-
Weight	Approx. 200	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*2 Negative-type display

Display data "H" → Display ON = white

Display data "L" → Display OFF = black

5.Electrical Specifications

5-1.Electrical characteristics

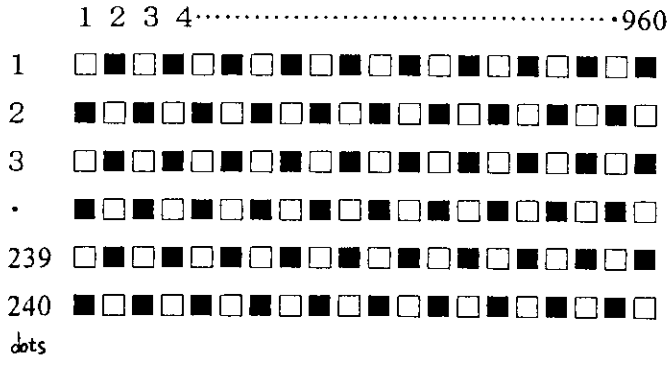
Table 5

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	Ta = 0~60 ℃		4.75	5.0	5.25	V
Supply voltage (LCD) Note 1)	V_{EE}-V_{SS}	Ta = 0 ℃		-	T.B.D.	T.B.D.	V
		Ta = 25 ℃			(21.8)		
		Ta = 60 ℃		T.B.D.	T.B.D.		
Input signal voltage	V_{IH}	"H" level	Ta = 0~60℃	0.8V_{DD}	-	V_{DD}	V
	V_{IL}	"L" level		0	-	0.2V_{DD}	V
Supply current	I_{DD}	Ta =25 ℃(Note 2)		-	(3.0)	(4.5)	mA
	I_{EE}			-	(6.5)	(10)	mA
Power consumption	Pd	Ta =25 ℃(Note 3,4)		-	(170)	(255)	mW

Note 1) Frame frequency = 75 Hz.

Note 2) Frame frequency = 75 Hz, V_{EE} - Vss = T.B.D. V, V_{DD} = 5 V

Display pattern = checker flag pattern



Note 3) Except Lamp power consumption. (*See Page 12)

5-2 Interface signals

○ LCD

Table 6 CN1 (LCD)

No.	Symbols	Description	Note
1	YD	scan start-up signal	"H"
2	LP	input latch singal	"H" → "L"
3	XCK	data input clock signal	"H" → "L"
4	DISP	display control signal	"H" display on , "L" display off
5	VDD	power supply for logic(+5V)	
6	VSS	ground potential	
7	VEE	power supply for LCD	
8	D7	disply data signal	"H" (ON) , "L"(OFF)
9	D6		
10	D5		
11	D4		
12	D3		
13	D2		
14	D1		
15	D0		

○ Inverter

Table 7 CN2 (CCFT)

No.	Symbols	Description	Note
1	VL1(GND)	ground line(from Inverter)	for back light
2	NC	-	
3	VL2(HV)	High voltage line(from Inverter)	

Used connector

CN1 : 53216-1510 (MOLEX)

CN2 : BHR-03VS-1 (JST)

Correspondable connector

CN1 : 51021-1500 (MOLEX)

CN2 : SM02-(8.0)B-BHS-1 (JST)

Except above connector shall be out of guaranty.

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5-3.Interface timing

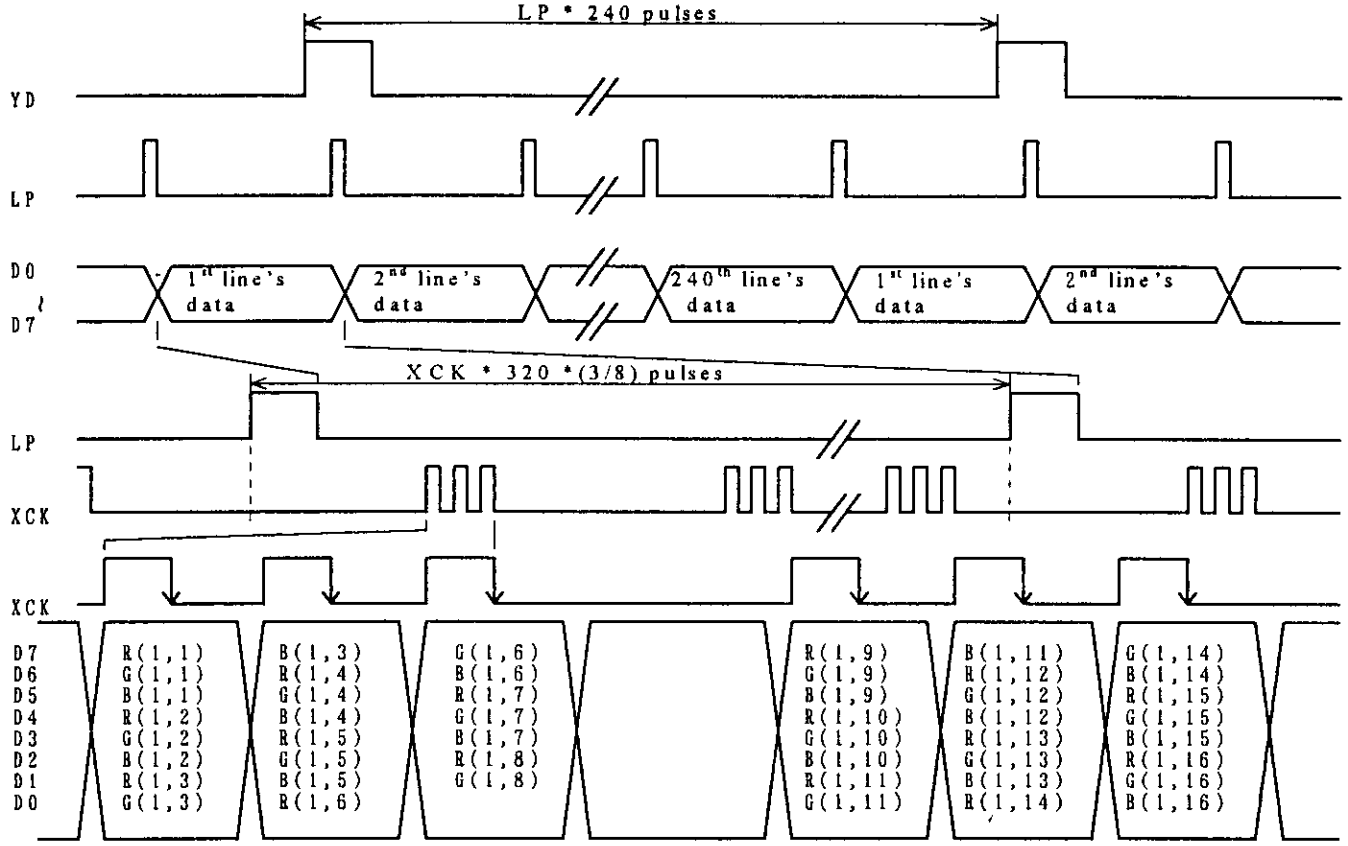


Fig.2 Interface timing

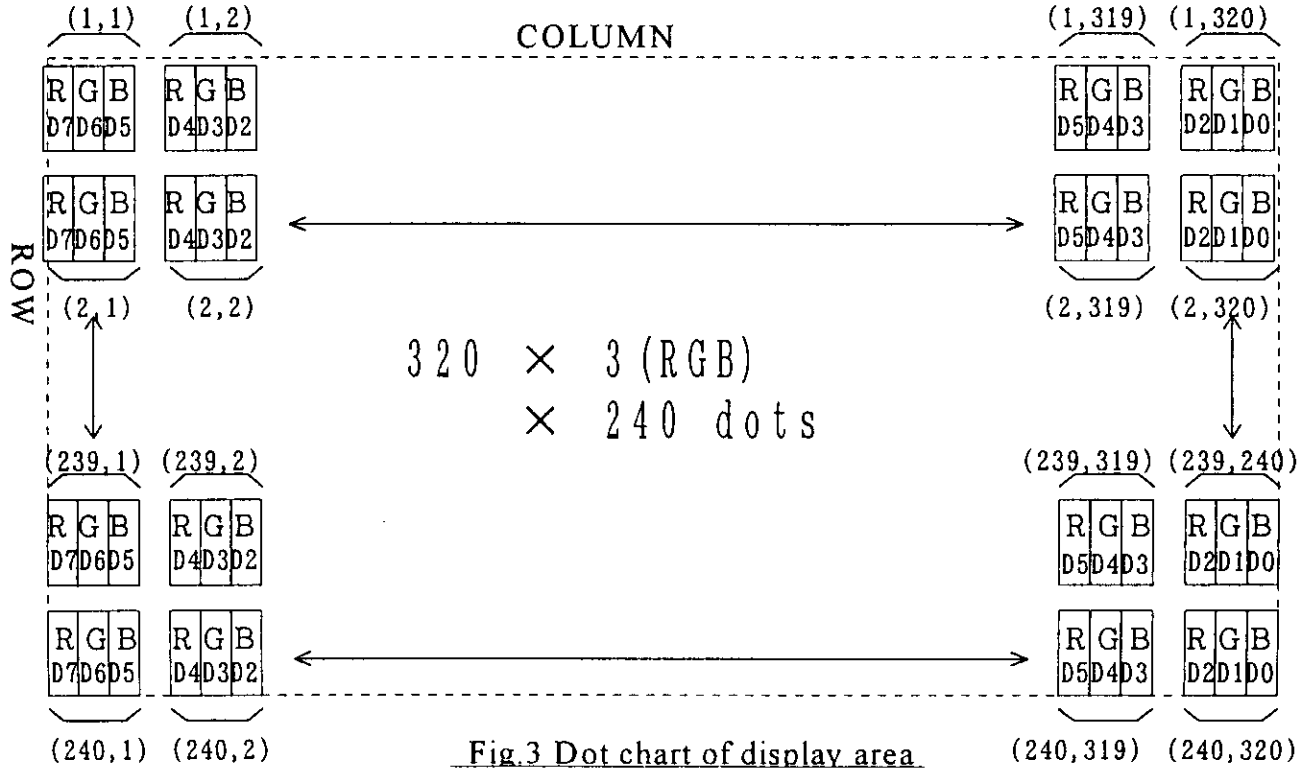


Fig.3 Dot chart of display area

Table 8 Interface timing ratings

Ta=25 ℃,VDD = 5.0 V±10 %

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Flame cycle Note 1)	t_{FRM}	(11)		(16)	ms
XCK clock cycle Note 2)	t_{CK}	81			ns
XCK "H" level width	t_{WCKH}	35			ns
XCK "L" level width	t_{WCKL}	35			ns
LP "H" level latch clock width	t_{WLPH}	200			ns
Data set up time	t_{DS}	35			ns
Data hold time	t_{DH}	35			ns
YD "H" level set up time	t_{HYS}	100			ns
YD "H" level hold time	t_{HYH}	100			ns
YD "L" level set up time	t_{LYS}	100			ns
YD "L" level hold time	t_{LYH}	100			ns
LP ↓ allowance time from XCK ↑	t_{LS}	200			ns
XCK ↓ allowance time from LP ↑	t_{LH}	200			
Input signal rise/fall time*1	t_r,t_f	-		13	ns

Note 1) Owing to the characteristics of this LCD module, "shadowing" will become more eminent as frame frequency goes up, contrast ratio will be down and flicker will become more eminent as flame frequency goes down. So it is recommended that the module should be driven according to he specified limit.

It is recommended that frequency range is 70 Hz～ 80 Hz.

Note 2)The intervals of one LP fall and the next must be always the same, and LPs must be input continuously. The interval must be 70 μ s MAX.

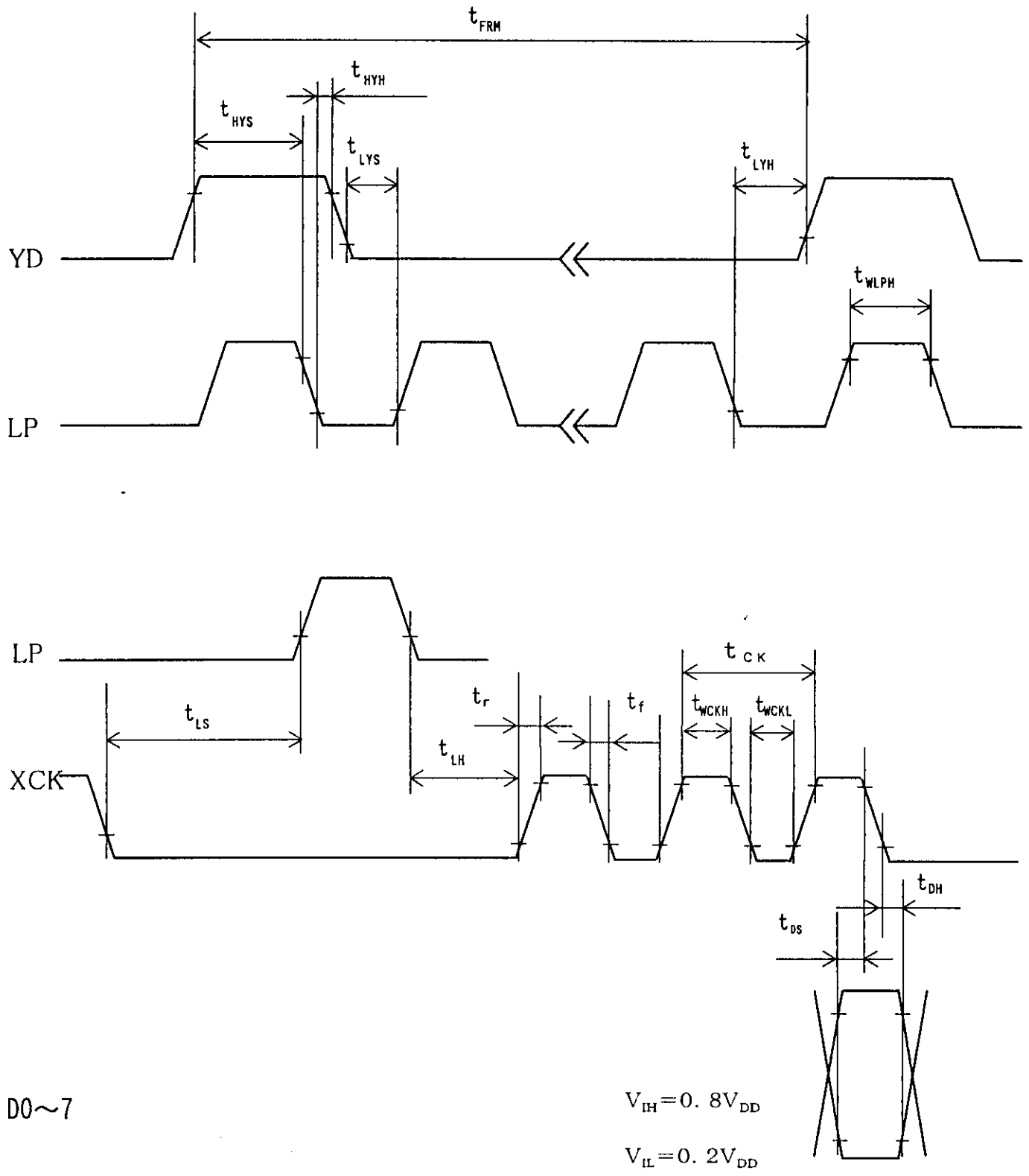


Fig.4 Interface timing chart

6. Module Driving Method

6-1. Input data and control signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (320×3 R,G,B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal (XCK).

When input of one row (320×3 R,G,B) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP) then, the corresponding drive signals will be transmitted to the 320×3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 320×3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 240th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method. Simultaneously the same scanning sequence occur at the lower panel. Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system of transferring 8 bit parallel data through the 8 lines of shift registers.
Thanks to this system the power consumption of the display module is minimized.

In this circuit configuration, 8 bit display data shall input to data input pins of D0-7.

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 240 dot (30XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. This process is followed simultaneously both at the top and bottom column drivers LSI's.

Thus data input will be made through 8 bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals are shown in fig. 4 and Table 8.

7. Optical Characteristics

Table 9 Ta = 25 ℃, V_{DD}= 5.0 V, V_{EE} = V_{CO} max

Parameter		Symbo	Condition			MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θ_x	Co>2.0	θ_y=0 °	$\theta_x \geqq 0$ °	(50)	-	-	°	Note1)
					$\theta_x < 0$ °	-	-	(-50)	°	
		θ_y		θ_x=0 °	$\theta_y \geqq 0$ °	(45)	-	-	°	
					$\theta_y < 0$°	-	-	(-60)	°	
Contrast ratio		Co	$\theta_x = \theta_y = 0$ °			T.B.D.	(40)	-	-	Note2)
Response time	Rise	τ r	$\theta_x = \theta_y = 0$ °			-	(220)	(320)	ms	Note3)
	Decay	τ d	$\theta_x = \theta_y = 0$ °			-	(110)	(210)	ms	
Brightness		B	$\theta_x = \theta_y = 0$ °	IL = 5.0 mA		T.B.D.	(200)		cd/m^2	Note4)
Module chromaticity	white	x	$\theta_x = \theta_y = 0$ °			-	(0.35)	-	-	
		y	$\theta_x = \theta_y = 0$ °			-	(0.36)	-	-	

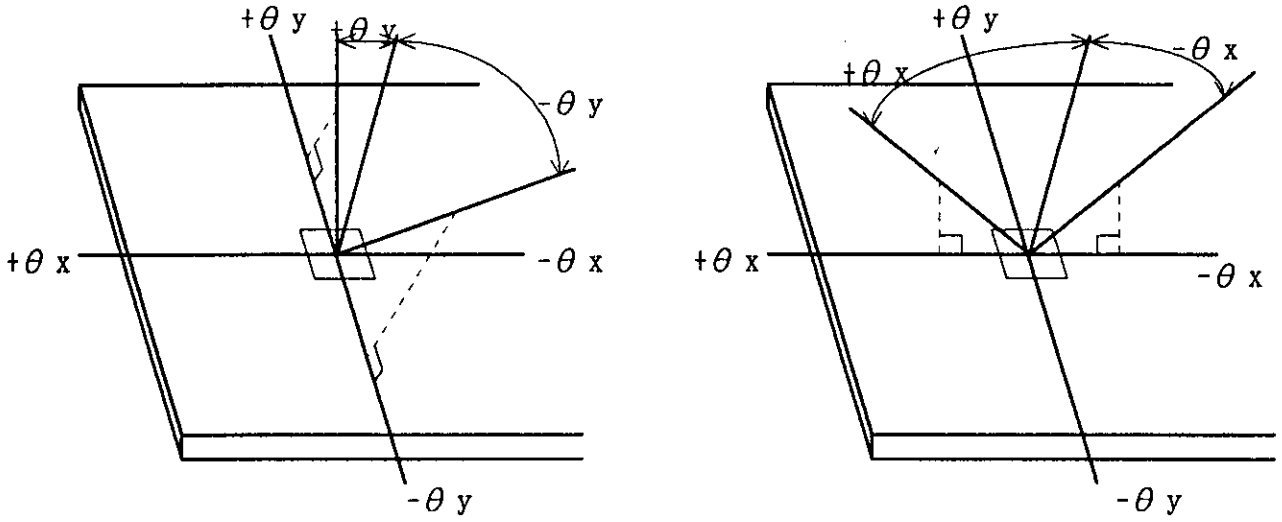


Fig.5 Definition of Viewing Angle

Note 1) The viewing angle range is defined as shown Fig.5

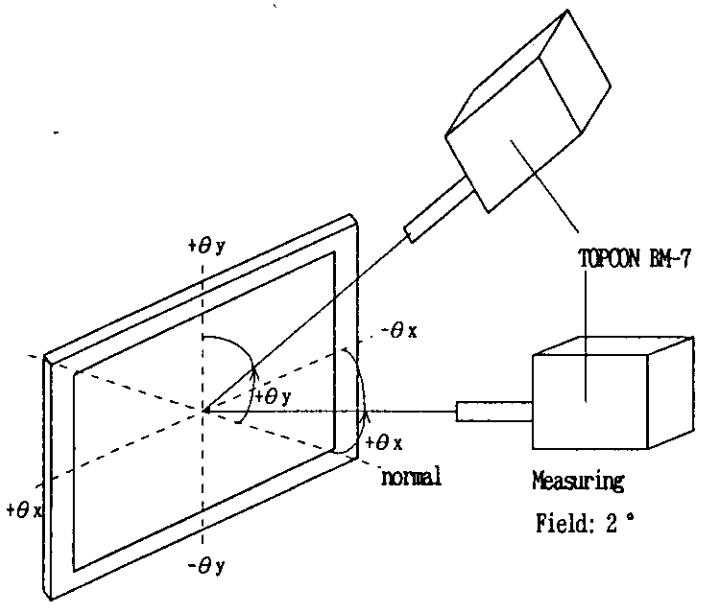
Note 2) Contrast ratio is defined as follows:

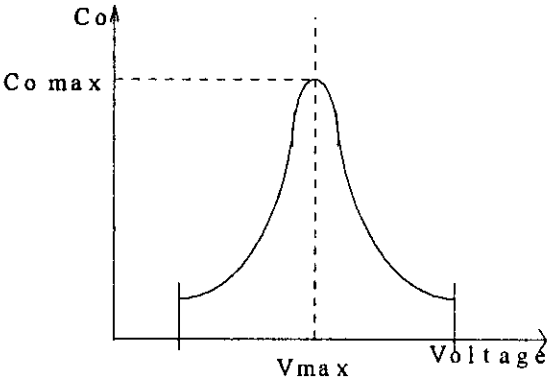
$$Co = \frac{\text{Luminance(brightness) all pixes "White" at Vmax}}{\text{Luminance(brightness) all pixes "dark " at Vmax}}$$

Vmax is defined in Fig.7.

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.8, assuming that input signals are applied so as to select and deselect the dot to be measured, in the optical characteristics test method shown in Fig.6

Note4) Brightness is defined as average luminance (brightness) of measuring points (①~⑤) at Vcmax. All pixels of LCD is "white"





Measuring Spot Size : ϕ 10 mm

θ x : Angle from "normal" to viewing surface rotated about the horizontal axis.

θ y : Angle from "normal" to viewing surface rotated about the vertical axis.

Fig.6 Optical Characteristics Test Method I

Fig.7 Definition of Vmax

(Response Measurement)

Ta = 25 ℃

In dark room

TOPCON BM7 + quartz fiber

(Measuring spot size : ϕ 10 mm, Measuring Field : 2 °)

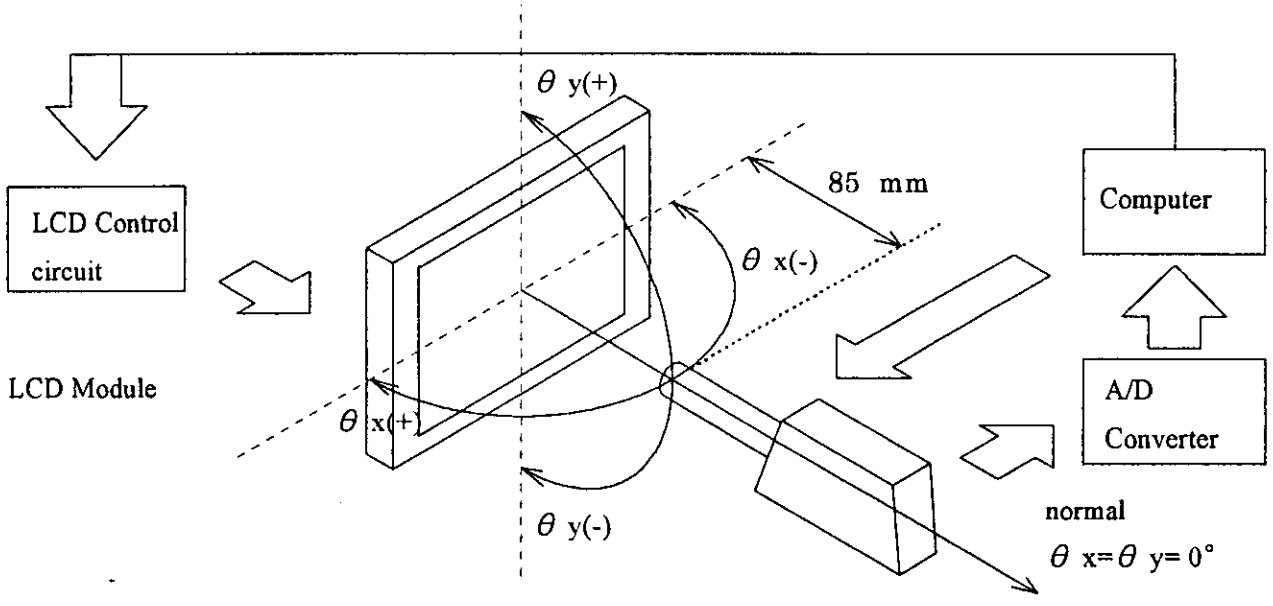
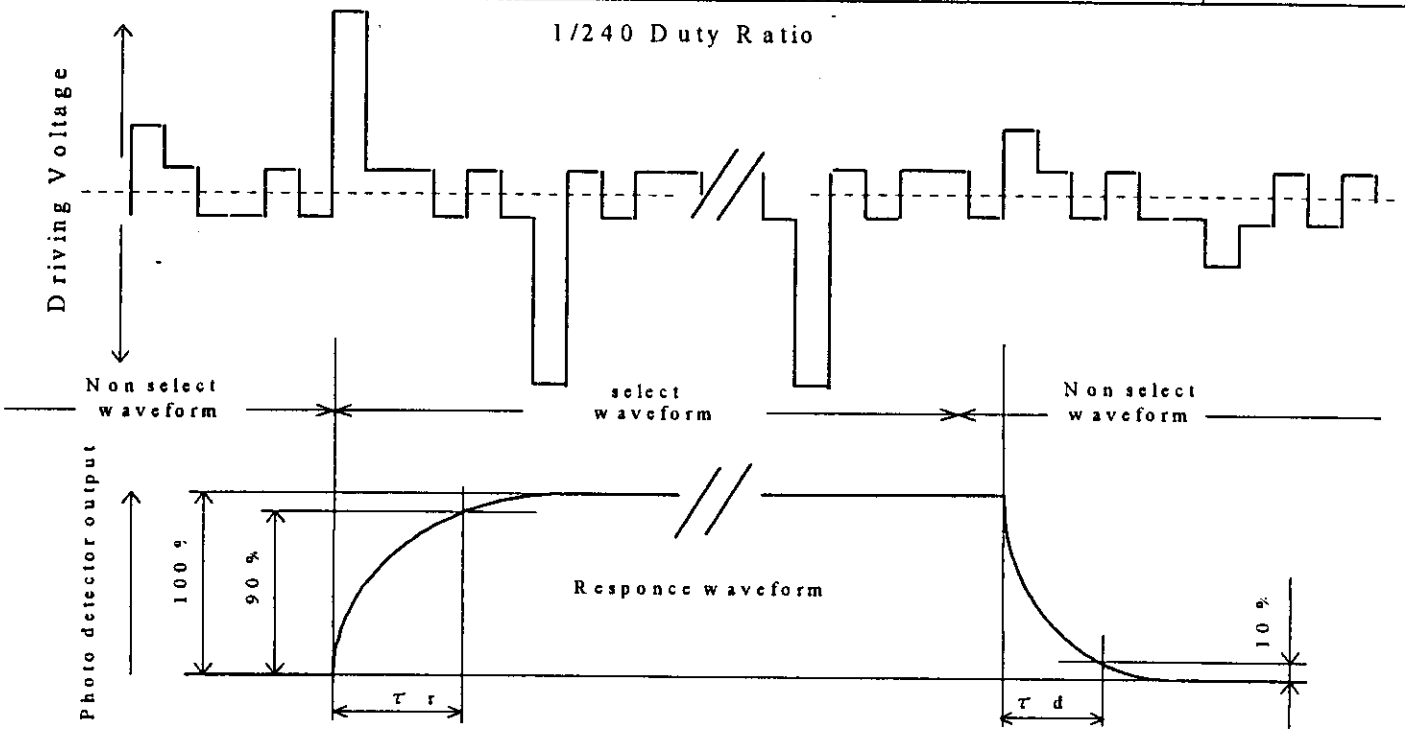


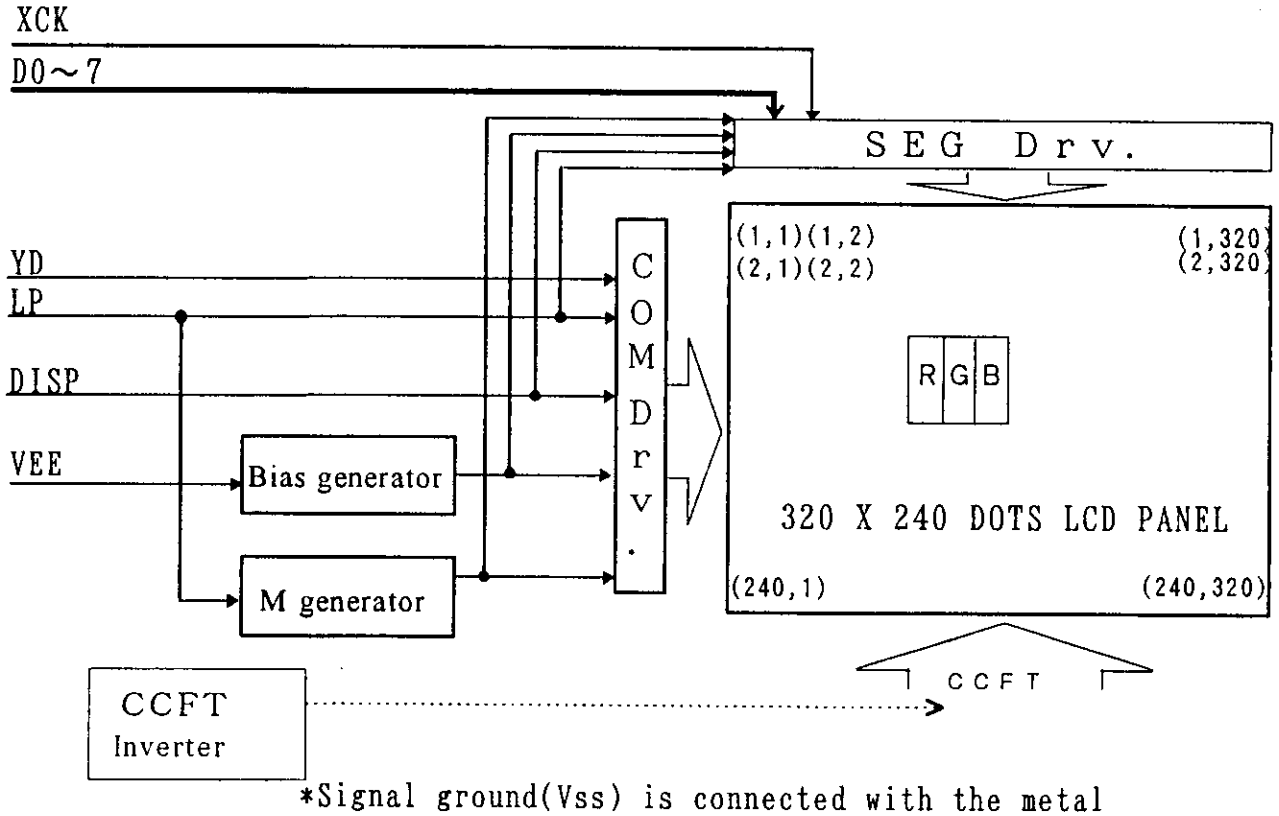
Fig. 8 Optical Characteristics Test Method II



τ r: Rise time

τ d: Decay time

Fig.9 Definition of Response time



*Signal ground(Vss) is connected with the metal

Fig.10 Circuit block diagram

8.Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied.

1) Rating(Note)

Table 10

Parameter	MIN.	TYP.	MAX.	Unit
Brightness	-	(200)	-	cd/m^2

2) Measurement circuit : CXA-M10L(TDK) (at IL = 5.0 mArms)

3) Measurement equipment : BM-7 (TOPCON Corporation)

4) Measurement conditions

4-1. Measurement circuit voltage : DC = 9.5 V, at primary side

4-2. LCD: All digits WHITE, V_{DD}= 5.0 V, V_{EE} = Vmax, D7～0 :"H"(White)
1/tFRM = 75 Hz

4-3. Ambient temperature : 25 ℃
Measurement shall be executed 30 minutes after turning on.

5)

5-1. Rating (1pc)

Table 11

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Lamp current	I_L	T.B.D.	5	T.B.D.	mArms	*1
Lamp voltage	V_L	-	400	-	Vrms	
Lamp power consumption	P_L	-	2	-	W	*2
Lamp frequency	F_L	30	-	100	kHz	
Kick-off voltage	V_S	-	-	650	Vrms	Ta=25 ℃
		-	-	770	Vrms	Ta= 0 ℃, *3
Lamp life time	L_L	-	25 000-	-	h	*4

*1 It is recommended that I_L be not more than T.B.D. mArms so that heat radiation of CCFT backlight may least affect the display quality.

*2 Power consumption excluded inverter loss.

*3 The circuit voltage(VS) of the inverter should be designed to have some margin, because VS may be increased due to the leak current in case of the LCD module.

*4 Average life time of CCFT will be decreased when LCD is operating at lower temperature.

6) Operating life

The operating life time is 25 000 hours or more at 5 mArms, 25 ±1℃

(Operating life with CXA-M10L or equivalent.)

The inverter should meet the following conditions to keep the specified life time of used lamp;

-Since, symmetric waveform without spike in positive and negative

-Output frequency range: 30 kHz-100 kHz

Make sure the operating conditions by executing the burn-in enough time.

The operating life time is defined as having ended when any of the following conditions occur;

-When the illuminance or quantity of light has decreased to 60 % of the initials value.

-When the kick-off voltage has reached Maximum value.

(NOTE) Rating are defined as the average brightness inside the viewing area specified in Fig.11.

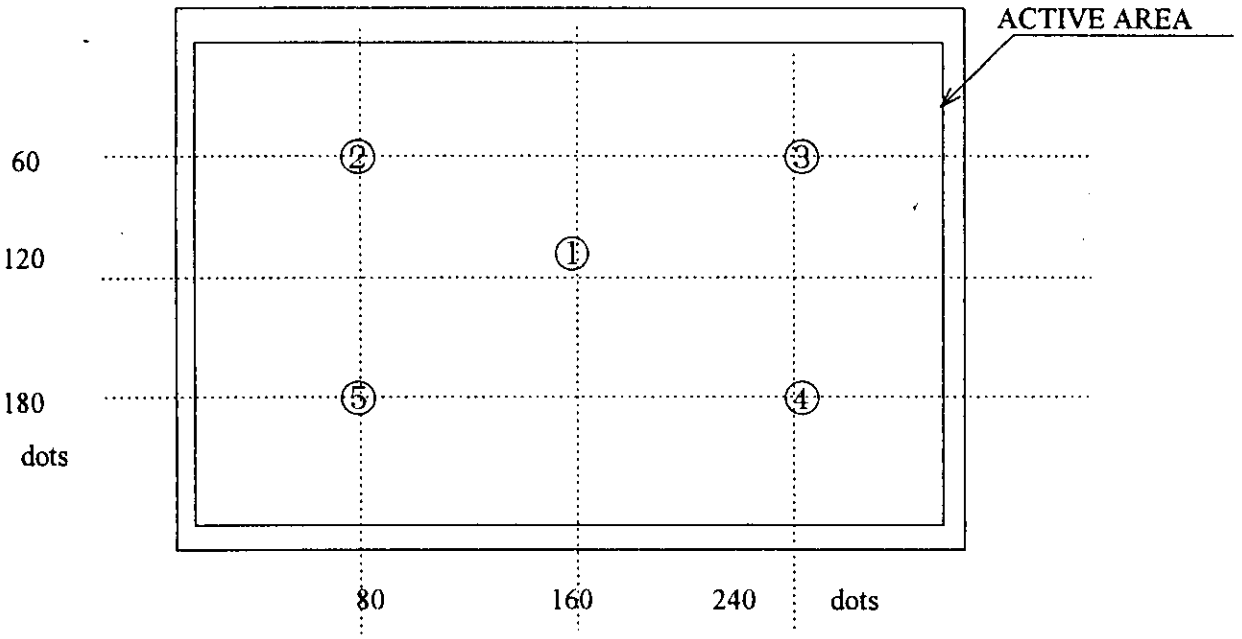


Fig.11 Measuring points (1-5)

9. Supply voltage sequence condition

The power ON/OFF sequence shown on Fig.12 shall be followed to avoid latch-up of drive LSIs and application of DC voltage to LCD panel.

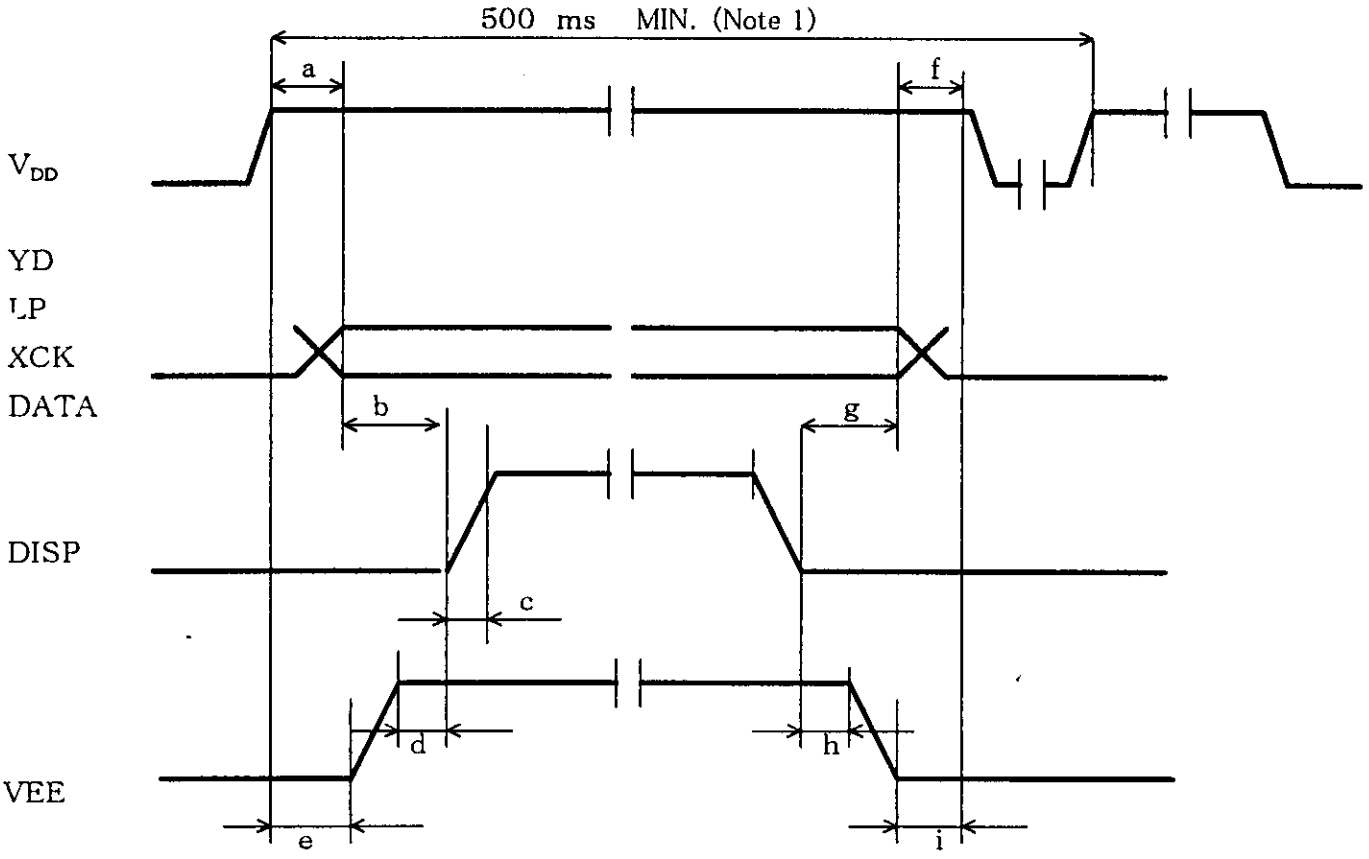
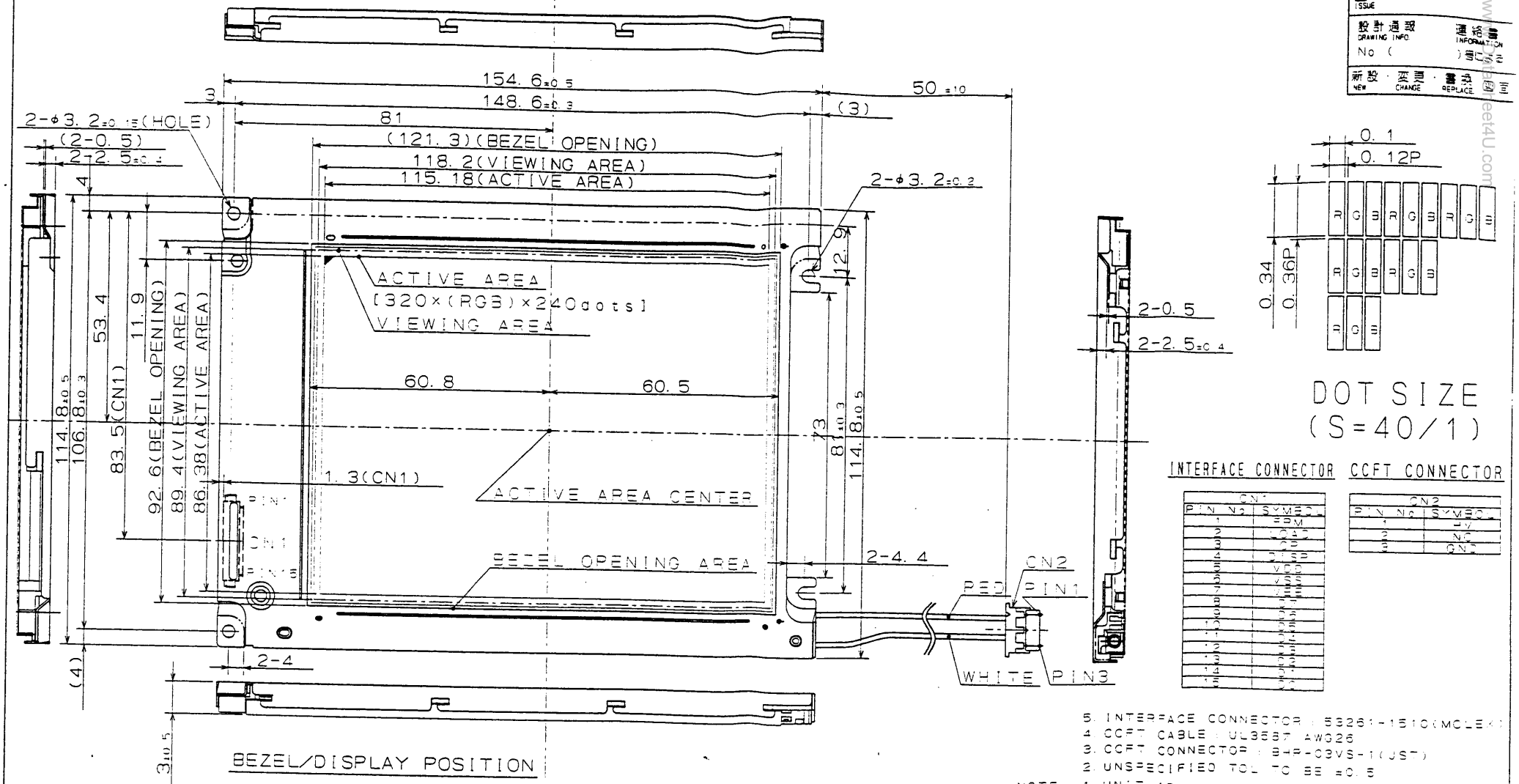


Fig.12 Sequence condition

	POWER ON	
Symbol	Allowable value	
a	0 ms MIN.	1 s MAX.
b	20 ms MIN.	-
c	-	100 ns MAX.
d	0 ms MIN.	-
e	0 ms MIN.	-

	POWER OFF	
Symbol	Allowable value	
d	0 ms MIN.	1 s MAX.
e	20 ms MIN.	-
	20 ms MIN.	-
f	0 ms MIN.	-

Note 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.



DOT SIZE
(S=40/1)

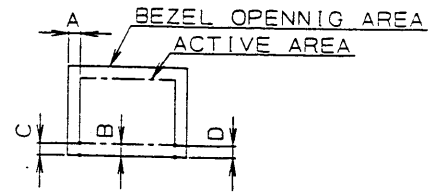
INTERFACE CONNECTOR

CN1	
PIN No.	SYMBOL
1	EDM
2	LCCAS
3	LCCAS
4	DISP
5	VDD
6	VDD
7	R0
8	R1
9	R2
10	R3
11	R4
12	R5
13	G0
14	G1
15	G2
16	G3
17	G4
18	G5
19	B0
20	B1
21	B2
22	B3
23	B4
24	B5
25	GND
26	GND
27	GND
28	GND
29	GND
30	GND

CCFT CONNECTOR

CN2	
PIN No.	SYMBOL
1	HV
2	NC
3	GND

BEZEL/DISPLAY POSITION



1) TOLERANCE X-DIRECTION A:3.21±0.5
2) TOLERANCE Y-DIRECTION B:3.11±0.5
3) OBLIQUITY OF DISPLAY AREA IC-DI<0.5

5. INTERFACE CONNECTOR : 53261-1510(MOLEX)
4. CCFT CABLE : UL3587 AWG26
3. CCFT CONNECTOR : BHR-03VS-1(JST)
2. UNSPECIFIED TOL. TO BE ±0.5
NOTE : 1. UNIT IS mm

/3					LM057QC1T01	NAME	LCD MODULE OUTLINE DIMENSIONS
/2							
/1							
DATE	REVISE			PREP'A	MODEL		
MATERIAL	THICKNESS	FINISH			SCALE 1/1	ASSEMBLY	320×3×240 DOTS
						PARTS CODE	
DESIGN	TRACE	CHECK	CHECK	APPROVE	SHARP CORPORATION	DATE	1998 10 8
					Mobile LCD Development P.T. Duty Panel Development Center Duty LCD Group	DRAWING No.	

10. Precautions

1) Industrial(Mechanical) design of the product in which this LCD module will be incorporated must be made so that the viewing angle characteristics of the LCD may be optimized.
This module's viewing angle is illustrated in Fig.1.
θ y MIN. < viewing angle < θ y MAX.
(For the specific values of θ y MIN., and θ y MAX., refer to the table)
Please consider the optimum viewing conditions according to the purpose when installing the module.

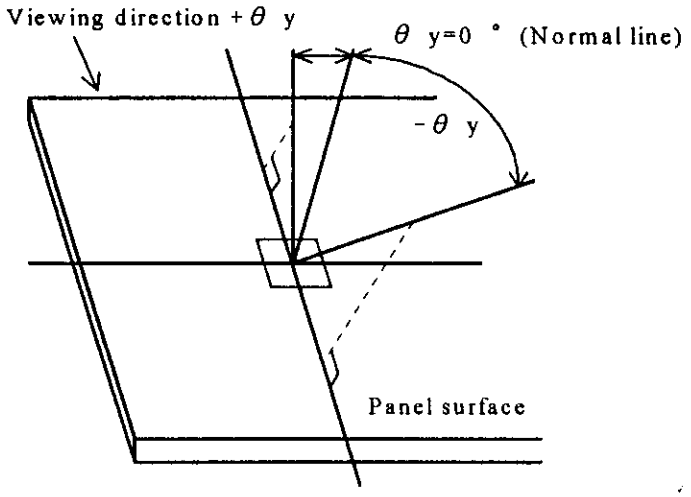


Fig.14 Definition of viewing angle

2) This module should be installed using mounting holes of metal bezel.
When installing the module, pay attention and handle carefully not to allow any undue stress such as twist or bend.

3) Since the front polarizer is easily damaged. Please pay attention not to scratch on its face.
It is recommended to use a transparent acrylic resin board or other type of protective panel on the surface of the LCD module to protect the polarizer, LCD panel, etc..

4) If the surface of the LCD panel is required to be cleaned, wipe it swiftly with cotton or other soft cloth. If it is not still clear completely, blow on and wipe it.

5) Water droplets, etc. must be wiped off immediately since they may cause color changes, staining, etc., if it remained for a long time.

6) Since LCD is made of glass substrate, dropping the module or banging it against hard objects may cause cracking or fragmentation.

7) Since CMOS LSIs are equipped in this module, following countermeasures must be taken to avoid electrostatics charge.

1. Operator

Electrostatic shielding clothes shall be had because it is feared that the static electricity is electrified to human body in case that operator have a insulating garment.

2. Equipment

There is a possibility that the static electricity is charged to equipment which have a function of peeling or mechanism of friction(EX: Conveyer, soldering iron, working table), so the countermeasure(electrostatic earth: 1×10^8 Ω) should be made.

3. Floor

Floor is a important part to leak static electricity which is generated from human body or equipment. There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure(electrostatic earth: 1×10^8 Ω) should be made.

4. Humidity

Humidity of working room may lower electrostatics generating material's resistance and have something to prevent electrifying. So, humidity should be kept over 50% because humidity less than 50 % may increase material's electrostatic earth resistance and it become easy to electrify.

5. Transportation/storage

The measure should be made for storage materials because there is a possibility that the static electricity, which electrify to human body or storage materials like container by friction or peeling, cause the dielectric charge.

6. Others

The laminator is attached on the surface of LCD module to prevent from scratches, fouling and dust. It should be peeled off unhurriedly with using static eliminator.

And also, static eliminator should be installed to prevent LCD module from electrifying at assembling line.

8) Don't use any materials which emit gas from epoxy resin(amines' hardener) and silicon adhesive agent(dealcohol or deoxym) to prevent change polorizer color owing to gas.

9) Since leakage current, which may be caused by routing of CCFT cables, etc., may affect the brightness of display, the inverter has to be designed taking the leakage current into consideration. Thorough evaluation of the LCD module/inverter built into its host equipment shall be conducted, therefore, to ensure the specified brightness.

10) Avoid to expose the module to the direct sun-light, strong ultraviolet light, etc. for a long time.

11) If stored at temperatures under specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state. Therefore, the module should be always stored at normal room temperature.

12) Disassembling the LCD module can cause permanent damage and should be strictly avoided.

13) Procedure insert mating connector

When the mating connector is inserted, it should be parallel to the used connector of LCD module and it should be inserted horizontally.

When the mating connector is attempted to be fixed to LCD connector, it should be inserted properly in order not to create a gap.

Please insert the connector as both edge is placed to the connect position of LCD connector.

14) The module should be driven according to the specified ratings to avoid permanent damage.

DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Especially the power ON/OFF sequence shown on Page 16 should be kept to avoid latch-up of drive LSIs and application of DC voltage to LCD panel.

15) It is a characteristic of LCD to maintain the displaying pattern when the pattern is a applied for long time. (Image retention)

To prevent image retention, please do not apply the fixed pattern for along time by pre-installing such programs at your side.

16) This phenomena (image retention) is not deterioration of LCD. It if happens, you can remove it by applying different patterns.

17) CCFT backlight should be kept OFF during VDD is "L" level.